# Analysis of a power MOSFET switching process

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***Abstract***. *This paper considers the switching dynamics of a power MOSFET using fourth order equivalent circuit for the different regions of operation. In contrast to the standard approach, reducing the investigated circuit to second order is not made, which helps to keep the detailed dynamics in the final waveforms. The governing equations for the different stages during turn on and off are written in state space form. Using this approach, the obtained waveforms are plotted for both the turn on and turn off process. Finally, a discussion is made about the way to implement some of the more obvious discrepancies between the used MOSFET equivalent circuits and the physical device.*

***Анализ на превключването при силови МОС транзистори (Владимир Димитров).*** *В статията са разгледани етапите на превключване на силов МОС транзистор в схема с два източника на енергия. На базата на еквивалентни схеми за всеки епап са записани описващите процеса диференциални уравниея, като за разлика от съществуващи изследвания не са пренебрегнати ефектите свеждащи динамиката до втори ред. Получените времедиаграми са показани, и са отбелязани основните разлики между времедиаграмите и реално наблюдаваните процеси.*

## I. Introduction

Power conversion inevitably involves the use of nonlinear elements as an integral part of a power circuit topology. The constraints imposed by real elements limit the achievable efficiency of the power converter. As a consequence the need for good models is more apparent, the tighter the design requirements are. Every model of a physical device must be a compromise between the depth of the modeled effects and simulation speed. The possibility of analytic solution is also a great concern, which allows the use of different parameters, without the need to adjust the simulation parameters for each run.

The power MOSFET is one of the primary devices used in power electronics for controlled energy conversion, and as such its dynamic behavior has received much interest from both academica [1], [2], [3], and industry [4], [5]. However, all of these publications describe the full equivalent circuit during the different stages of switching, and then reduce it to second or first order, which is the basis for the obtained waveforms. The underlying reason for this kind of modeling is the widespread engineering paradigm that second order ordinary differential equations (ODE) are the limit of analytic solvability. The possibility of analytically solving ODE`s up to fourth-order brings the question what will be the benefit of the additional burden to obtain and solve them. This is part of the motivation for this paper.

The paper investigates the switching dynamics of a power MOSFET based on its full equivalent circuit, bringing the dynamics to forth order with one exception. Its organization is as follows: in the next section the full equivalent circuits of the power MOSFET during the turn off, active and linear operation mode are presented along with the investigated circuit topology, also the assumed simplifications in the used equivalent circuits are discussed. Next in Section III the different stages during its turn on and turn off are discussed, the equivalent circuits for each of them are presented and the governing differential equations are obtained in state space form in combination with their initial

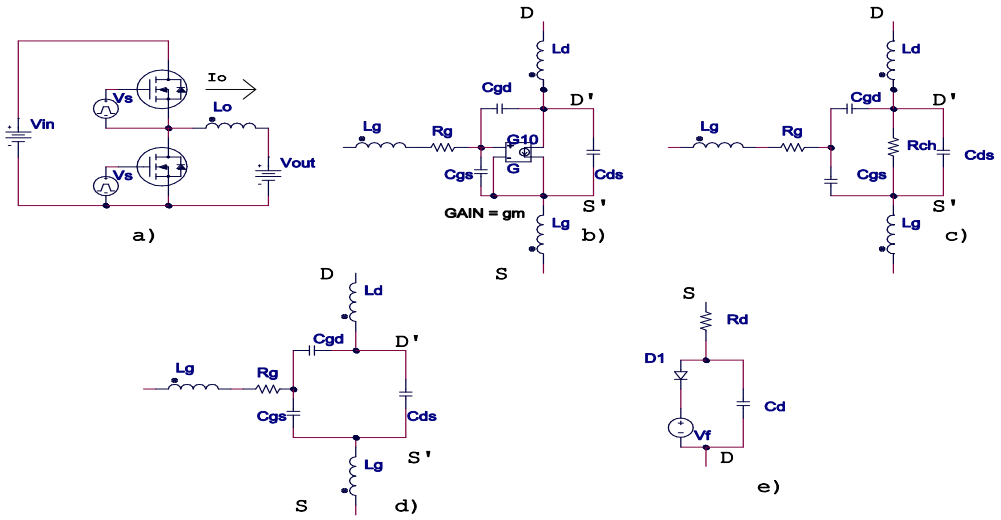



*Figure 1 a) Circuit for investigation, Equivalent circuits used in b) Active region, c) Linear reagion, d) Off state, e) Reverse diode*

conditions and the conditions for the end of the period. In Section IV waveforms for both the turn on and turn off dynamics are plotted using MATLAB for typical parameters. Finally, in section V a discussion is made about the possible modifications to account for some of the assumed simplifications.

## II. MOSFET equivalent circuits and assumptions

The MOSFET models used in the analysis of its switching behavior are shown in Figure ***1*** along with the studied circuit topology. The main idea behind the assumptions made is to obtain an ordinary differential equation which can be easily solved using specialized software for obtaining the switching dynamics. These are:

- The MOSFET is only modeled in its linear, active and off regions.
- The internal diode is modeled only during its reverse recovery, due to its higher influence over the overall losses, and also due to better documentation in datasheets.
- All L, R and C elements in its equivalent circuit are assumed linear and time-invariant.
- The load inductance Lo is assumed large enough, so during the switching process the output current Io is constant.

Although the assumptions of linear transistor capacitors are not realistic for real transistors at the end of the paper a method is discussed to rectify the problem.

## III. Switching Dynamics

The power MOSFET switching dynamics can be separated and analyzed independently during turn off and turn on. However, as it will be seen some of the resulting equivalent circuits and as a result the describing ODE are equivalent. A flowchart of the analyzed switching dynamics of a power MOSFET is shown in figure 2.

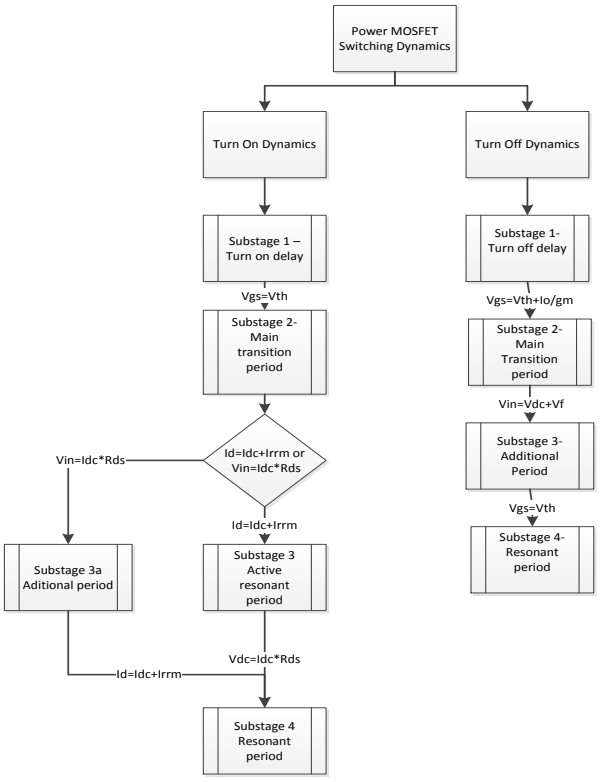



*figure 2 - A general flowchart of the power MOSFET dynamics*

### a. Turn on

**Stage 1**

The equivalent circuit to be analyzed is shown in figure 3.

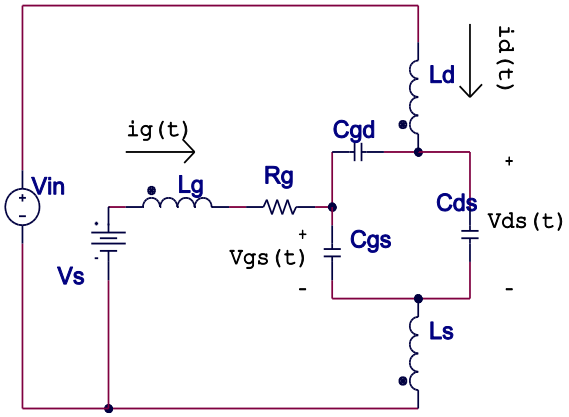



*figure 3 – Equivalent circuit during the first stage in transistor turn on dynamics*

At the start of this stage the gate driver applies a sufficient voltage to turn on the transistor and make it work in its linear region. However, this cannot happen instantaneously, and during this stage the transistor is off until the Vgs voltage reaches the threshold voltage.

The resulting circuit is of the fourth order, having one capacitor loop and one inductor cutset, so defining the state vector as $x = [i_g \quad V_{gs} \quad i_d \quad V_{ds}]$ the state space equation has the form,

$$\frac{dx}{dt} = Ax + Bu,$$

$$A = \begin{bmatrix} -\frac{R_g(L_s+L_d)}{L_{eq}^2} & -\frac{(L_s+L_d)}{L_{eq}^2} & 0 & \frac{L_s}{L_{eq}^2} \\ \frac{C_{ds}+C_{dg}}{C_{eq}^2} & 0 & \frac{C_{dg}}{C_{eq}^2} & 0 \\ \frac{R_g L_s}{L_{eq}^2} & \frac{L_s}{L_{eq}^2} & 0 & -\frac{L_s+L_g}{L_{eq}^2} \\ \frac{C_{dg}}{C_{eq}^2} & 0 & \frac{C_{gs}+C_{dg}}{C_{eq}^2} & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} -\frac{L_s}{L_{eq}^2} & \frac{L_s+L_d}{L_{eq}^2} \\ 0 & 0 \\ \frac{L_s+L_g}{L_{eq}^2} & -\frac{L_s}{L_{eq}^2} \\ 0 & 0 \end{bmatrix}, u = [V_{in} \quad V_s]$$

$$C_{eq}^2 = \sqrt{C_{ds}C_{gs} + C_{ds}C_{gd} + C_{gd}C_{gs}}$$

$$L_{eq}^2 = \sqrt{L_d L_g + L_d L_s + L_s L_g}$$

The initial conditions for this period are:

$$i_g = i_d = v_{gs} = 0, v_{ds} = V_{in}$$

**Stage 2**

This stage occurs when Vgs reaches the threshold voltage. The transistor turns on and during this time period operates in active region, and the resulting equivalent circuit is shown in figure 4.

It is characterized with combined rising of the drain current and Vds drop, with the size of Ld determining which process is evolving faster.

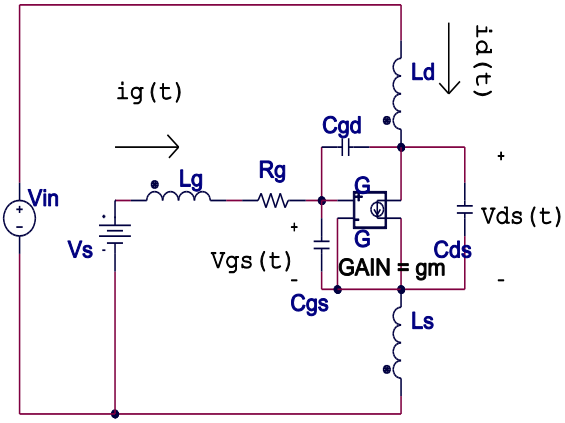



*figure 4 – Equivalent circuit during the second stage in transistor turn on dynamics*

Using the same state variables as in the previous stage:

$$\frac{dx}{dt} = Ax + Bu,$$

$$A = \begin{bmatrix} -\frac{R_g(L_s+L_d)}{L_{eq}^2} & -\frac{(L_s+L_d)}{L_{eq}^2} & 0 & \frac{L_s}{L_{eq}^2} \\ \frac{C_{ds}+C_{dg}}{C_{eq}^2} & -\frac{g_m C_{dg}}{C_{eq}^2} & \frac{C_{dg}}{C_{eq}^2} & 0 \\ \frac{R_g L_s}{L_{eq}^2} & \frac{L_s}{L_{eq}^2} & 0 & -\frac{L_s+L_g}{L_{eq}^2} \\ \frac{C_{dg}}{C_{eq}^2} & -\frac{g_m(C_{gs}+C_{dg})}{C_{eq}^2} & \frac{C_{gs}+C_{dg}}{C_{eq}^2} & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} -\frac{L_s}{L_{eq}^2} & \frac{L_s+L_d}{L_{eq}^2} \\ 0 & 0 \\ \frac{L_s+L_g}{L_{eq}^2} & -\frac{L_s}{L_{eq}^2} \\ 0 & 0 \end{bmatrix}, u = [V_{in} \quad V_s]$$

$$C_{eq}^2 = \sqrt{C_{ds}C_{gs} + C_{ds}C_{gd} + C_{gd}C_{gs}}$$

$$L_{eq}^2 = \sqrt{L_d L_g + L_d L_s + L_s L_g}$$

The initial conditions are:

$$i_g = I_{g0}, i_d = I_{d0}, V_{gs} = V_{th}, v_{ds} = V_{ds0}$$

There are two possible events the can lead to the end of this stage. In the more realistic one the drain voltage drops faster than the drain current. In this case the drain-source voltage drops until the transistor enters its linear region. For this reason the analyses only

for this period will be shown due to size considerations.

**Stage 3a**

If Vds reaches a value that ensures operation of the transistor in its linear region before the drain current reaches the load current an addition period must be analyzed shown in figure 5. This stage continues until the drain current reaches the output current in case of inductive load plus the reverse recovery current of the inverse diode of the upper transistor.

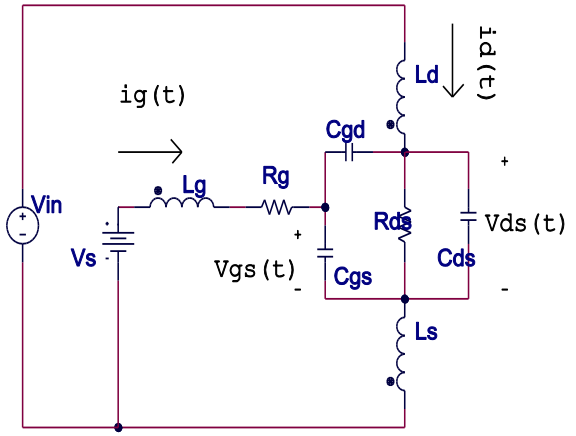



*figure 5 - Equivalent circuit during the third stage in transistor turn on dynamics*

Again the same state variables are used, leading to:

$$\frac{dx}{dt} = Ax + Bu,$$

$$A = \begin{bmatrix} -\frac{R_g(L_s+L_d)}{L_{eq}^2} & -\frac{(L_s+L_d)}{L_{eq}^2} & 0 & \frac{L_s}{L_{eq}^2} \\ \frac{C_{ds}+C_{dg}}{C_{eq}^2} & 0 & \frac{C_{dg}}{C_{eq}^2} & -\frac{C_{dg}}{R_{ds}C_{eq}^2} \\ \frac{R_g L_s}{L_{eq}^2} & \frac{L_s}{L_{eq}^2} & 0 & -\frac{L_s+L_g}{L_{eq}^2} \\ \frac{C_{dg}}{C_{eq}^2} & 0 & \frac{C_{gs}+C_{dg}}{C_{eq}^2} & -\frac{(C_{gs}+C_{dg})}{R_{ds}C_{eq}^2} \end{bmatrix}$$

$$B = \begin{bmatrix} -\frac{L_s}{L_{eq}^2} & \frac{L_s+L_d}{L_{eq}^2} \\ 0 & 0 \\ \frac{L_s+L_g}{L_{eq}^2} & -\frac{L_s}{L_{eq}^2} \\ 0 & 0 \end{bmatrix}, u = \begin{bmatrix} V_{in} & V_s \end{bmatrix}$$

$$C_{eq}^2 = \sqrt{C_{ds}C_{gs} + C_{ds}C_{gd} + C_{gd}C_{gs}}$$

$$L_{eq}^2 = \sqrt{L_d L_g + L_d L_s + L_s L_g}$$

The initial conditions are:

$$i_g = I_{g1}, i_d = I_{d1}, V_{gs} = V_{gs1}, v_{ds} = I_0 R_{ds}$$

**b. Turn off**

The turn off dynamics can be divided in four stages, where the analysis in every one is very similar to one of the stages during turn on, with the difference being the initial conditions and the stimulus. For this reason only the differences will be noted.

**Stage 1**

In this first stage at the turn off process the gate driver drops its voltage to –Vs and the equivalent circuit is shown in figure 6. As can be seen from it the analysis is very similar to stage 3a during turn on, so the same equations apply, the only difference being that the voltage Vs is negated, and Ld is replaced with Ld+Lo.

This stage ends when Vgs reaches a value forcing the transistor to operate in its active region. This value is dependent on its transconductance (gm) and load current according to $V_{gs} = \frac{I_o}{g_m} + V_{th}$. Also the initial conditions are $i_g = 0, i_d = I_o, V_{gs} = V_s, v_{ds} = I_o R_{ds}$

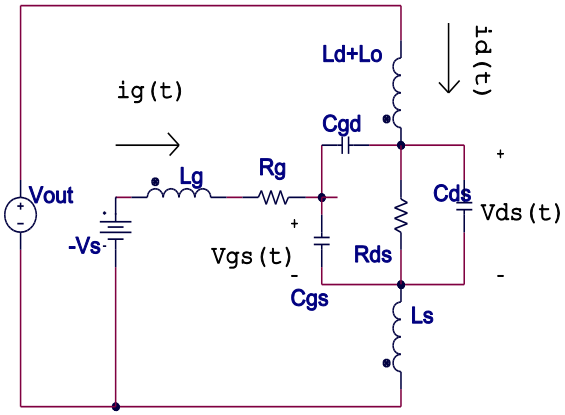



*figure 6 - Equivalent circuit during the first stage in transistor turn off dynamics*

**Stage 2**

During this stage the transistor operates in active region. Again as in stage 2 during turn on there is simultaneous change in the drain current and drain source voltage. The stage ends when Vds rises to a value sufficient to turn on the reverse diode of the other transistor, so Vds=Vin+Vf.

The equivalent circuit is shown in figure 7, and as the analysis is equivalent to stage 2 during turn on, it will not be repeated, the difference being the sign of Vs. The initial conditions are

$$i_g = I_{g1}, i_d = I_{d1}, V_{gs} = \frac{I_o}{g_m} + V_{th}, v_{ds} = V_{ds1}.$$

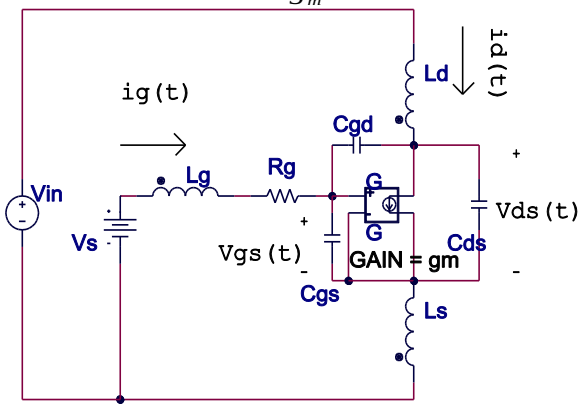
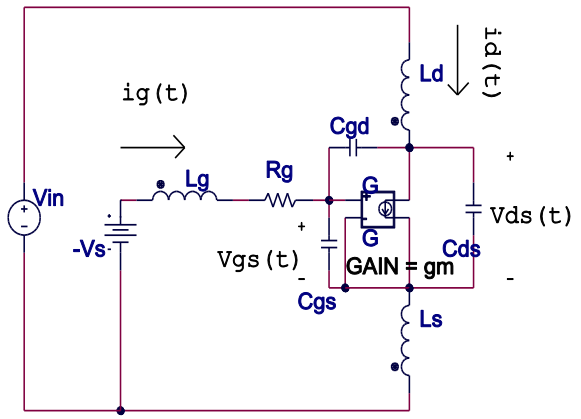



*figure 7 - Equivalent circuit during the second stage in transistor turn off dynamics*

**Stage 3**

When Vds reaches a value allowing the reverse diode of the other transistor to turn the resulting equivalent circuit is shown in figure 8 (note that forward recovery of the diode is not modeled).

The resulting circuit is very similar to stage 2 of the turn on dynamics with negative value of Vs. The initial conditions are




$i_g = 0, i_d = I_o, V_{gs} = V_s, v_{ds} = I_o R_{ds}$. This stage ends when the Vgs voltage reaches the threshold resulting in the transistor turning off.

*figure 8 - Equivalent circuit during the third stage in transistor turn off dynamics*

## IV. Simulation Results

Using the parameters shown in the appendix the waveforms for turn on and turn off are shown in figure 9 and figure 10.

## V. Conclusion

This paper considered the switching dynamics of a power MOSFET without making the common approximations to the used equivalent circuits. There are two main differences between the real device and the analyzed equivalent, and each of them will be discussed in turn.

The first one is the nonlinear dependence of the transistor capacitors on the voltages, and most notably Cds, as is also discussed in [1]. However, their dependence can easily be accounted for by using different values for different voltage values, in simple case one for high Vds and one for low.

The second problem is the idealization of the gate driver to an ideal voltage source, which is capable in instant transitions between high and low value. This is unrealistic in real situations, which can lead to substantial prolongation of the first and second stages in the associated turn on or off process. This problem is also easily fixed by using the Laplace transform of the obtained differential equations and substituting its constant value with a typical exponential or linear ramp.

Finally, in a future paper the comparison between the proposed model and the cited models for calculating switching losses will be presented.

## VI. Appendix

The simulation values used for the generation of figure 10 and figure 9 are: Vin=24V, Vs=15V, Lg=5,5nH, Ls=7.5nH, Ld=4,5nH, Vth=2V, gm=400, Rds=2mOhm, Ciss=4nF, Crss=1,1nF, Coss=3,65nF.

## VII. Acknowledgements

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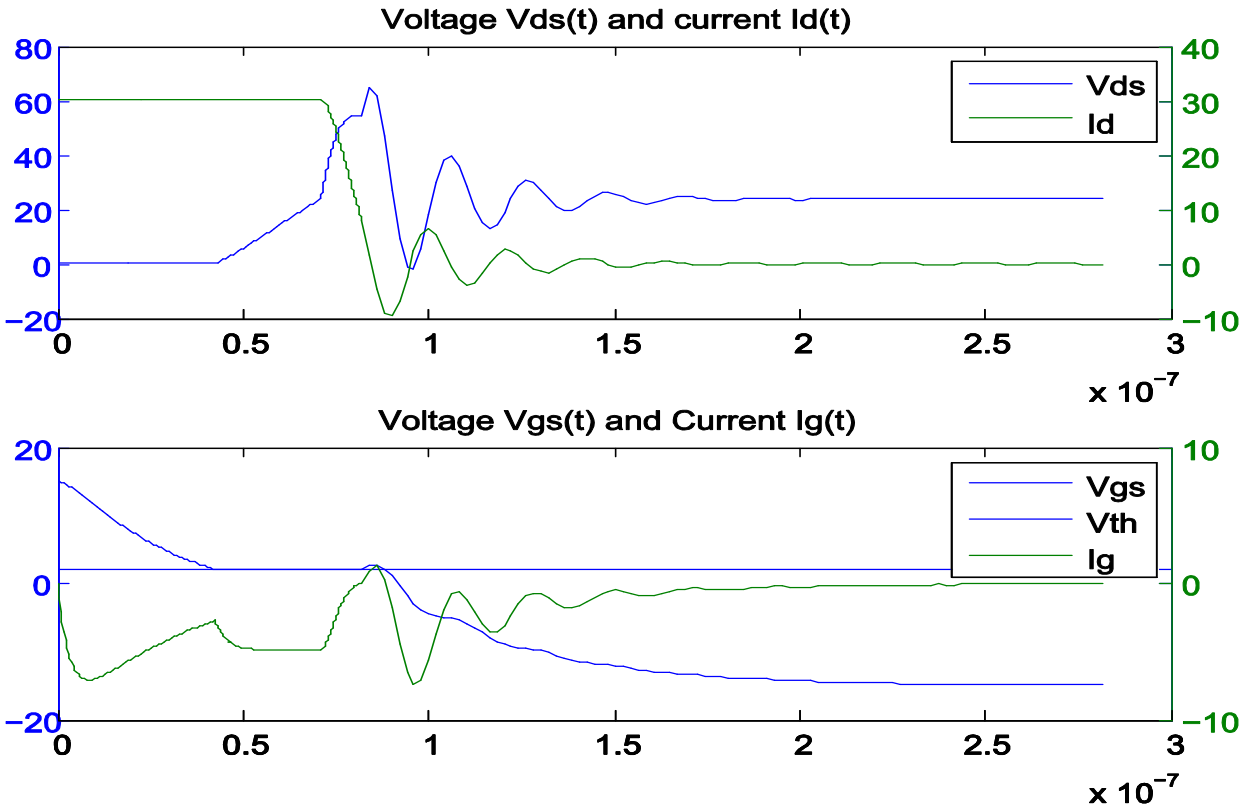


*figure 10 – Model Turn On Dynamics*

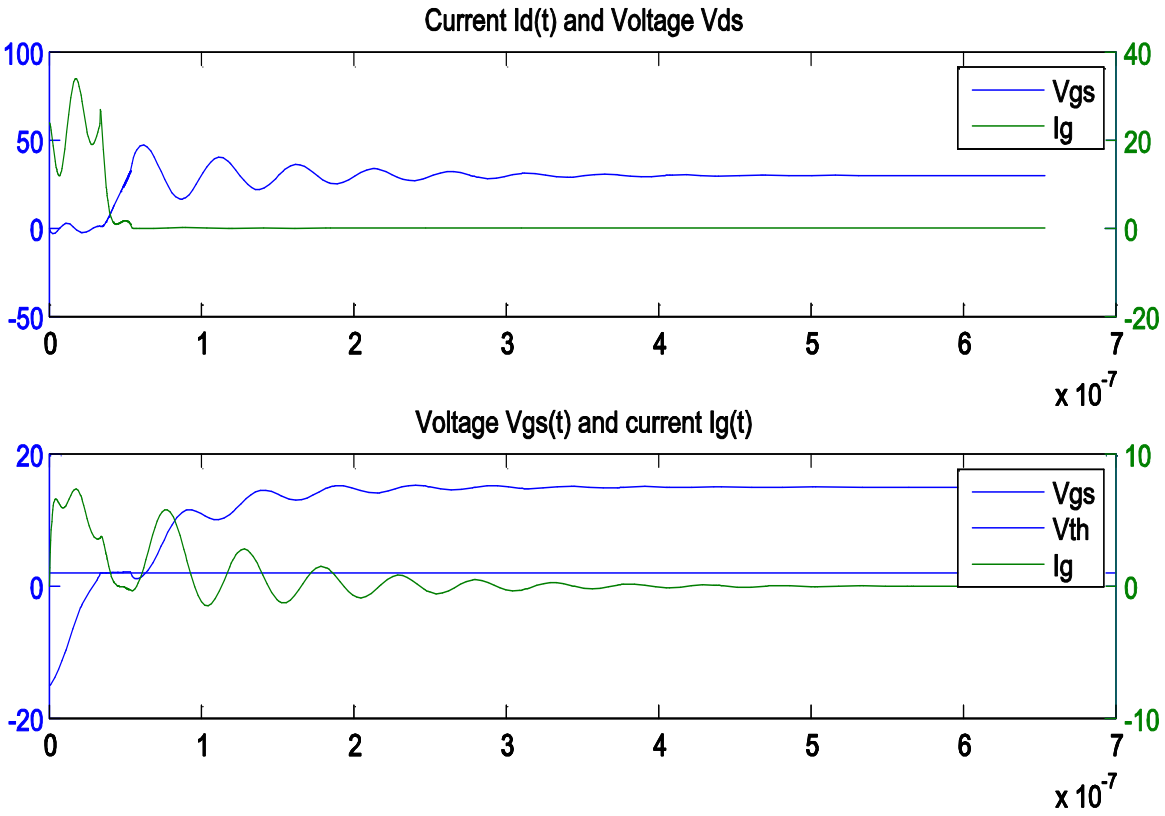


*figure 9 Model Turn Off Dynamics*