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COMPUTER INVESTIGATION OF THREE PHASE CLARKE-MAXIMUM (MAXIMUM p, q) TRIGONOMETRICAL PLL FOR GRID CONNECTED POWER CONVERTERS

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ABSTRACT

This paper focuses on three-phase Clarke-maximum (Maximum p, q) trigonometrical PLL. An advantage of the proposed implementation is the improved performance at an initial difference in phase angles greater than 90º, and the presence of one equilibrium point – coincidence of the input and output signals phases. A block diagram for the implementation of the PLL and a PSIM computer simulation model are presented as well as computer simulation results of the research.

KEYWORDS: Phase Locked Loop, Clarke Transformation, Grid Connected Power Converters.

1. INTRODUCTION

The operation of the control systems of on-grid inverters and active power filters needs a reference signal, by which it continuously monitors the grid voltage frequency and phase [1], [2], [3]. Such a signal is used also in other types of power electronic converters [4]. Various methods of synchronization exist, the most frequently used one is based on various PLL schematics. Reference [5] contains an overview of the historical development of the phased-locked loops, general information about their operation as well as a more detailed review of the three major blocks building the general block-diagram of a single-phase PLL. Classification and explanation of the basic operation of the most commonly used types of control and synchronization methods are presented in [2]. Increasingly, one can find separate approaches in the implementation of the PLL in three-phase and single-phase applications in recently published researches. In grid connected three-phase applications the synchronous-reference frame is very commonly used [6], [7]. The main idea of the synchronous-reference frame PLL is the transformation of the input signals in *dq*-frame by means of the well-known Park and Clark transformations. A design of such a PLL is proposed in [6]. In case

of operation of the grid-inverter in polluted utility grid to improve the quality of the energy, an adaptive synchronous reference frame PLL is presented in [8]. Specificity of this PLL is the rejection of disturbances even in case of variable fundamental frequency which is obtained by the use of several in number and type filters, such as notch filters and others. In the science literature, there are also some three-phase PLLs which fulfill the standard *pq*- theory and with simple addition of feedforward action a higher performance is easily reached at the start-up stage [9]. There are also single-phase phase-locked loops, based on modified *pq* theory [10]. A new approach for three-phase systems is presented in [11] and [10]. It is based on a preliminary estimation of the main parameters of the input signal – frequency, phase, magnitude, etc. It uses three different enhanced PLLs for each of the three phases of the input signals which are in the *abc*-frame. One of the major advantages of this method is its simplicity and introduction of parameter independency which can be applied to the other PLL methods, too. A similar approach for single-phase applications is presented in [12]. Other PLLs for frequency variable signals are proposed in [13], [14]. In order to decrease phase error problems in some PLLs for grid applications, methods with Selective Harmonics Elimination (SHE) operating in single- and three-phase systems have been developed [15]. A harmonics approach is also used in the digital phase-locked loop (DPPL) [16]. It consists of even harmonics elimination and thus the grid fundamental harmonic is extracted which is used as unity reference signal. As it happens that the utility grid operates under distorted conditions and its voltage is not always balanced, some PLL techniques for this kind of operation have been also researched [17], [18], [19], [20], [21]. The common for the first four quoted methods is that all of them use estimation of positive and negative sequences of the input signal at an uncertain frequency value. Such a method is used also in the fixed reference frame phase-locked loop (FRF-PLL) [22], [10] but the sequences are in stationary coordinates. There is also a research proving by mathematical analysis that the SOGI-PLL [17], [23] and the Park-PLL are equivalent in terms of control [24]. Another topology of PLL, based on the FPGA implementation [25], can also separate the components and detect harmonic components in three-phase signals. The last one uses lead compensators cascaded with a PI controller in order to reject some harmonics of the synchronous-reference-frame without reducing the bandwidth of the PLL. A novel hardware-based all-digital PLL presented in [26] has a zero-crossing detection function of the PD block. Philosophy of its operation is similar to the one of [9] in terms of the added feedforward loop due to which the frequency can vary and the PLL performance in terms of speed increase. In [26] a PLL is described with a phase-detector which rejects a ripple noise of the second order harmonics, without using any classical loop-filters, which can decrease the PLL performance in terms of response to dynamic changes, as well as it can decrease of about 50% of the settling time of the PLL. Reference [28] presents a modified power based PLL for single-phase systems, which is based on a so called double-frequency and amplitude compensation (DFAC) method in order to overcome some of the disadvantages of the standard PLL, such as sensitivity to grid frequency variation, double-frequency, etc. In [29] three PLL algorithms are presented, namely, pPLL, parkPLL and EPLL. In [30] an open-looped structure is described that processes the input signal and as a result the frequency and amplitude of its first-order harmonic and the higher-order harmonics are obtained. The scheme is characterized by an increased number of processing blocks – 4 multipliers and 3 integrators. The quality of the transient response is characterized by two additional parameters when compared to conventional methods. The way to define these two parameters is not clarified. In [31] a new detection method to find the phase and amplitude of the first-order and higher-order harmonics is described. The method is based on anticonjugate harmonic decomposition and cascaded delayed signal cancelation. A single-phase PLL proposed in [32] uses a phase detector multiplier and a phase shifter to obtain cosine from a sine function. Thus the PLL contains a low pass filter that decreases its response. The same filter is in the structure of the described PLL in [33], where the output signal is generated from a post-processor. In [34], [35] are presented researches on qPLL. A comparative analysis of q-PLL and feedforward loop (FFqPLL),

type2-PLL and type3-PLL is done in [36]. Single-phase PLL with such a q-PLL structure has been researched in [37], [38]. Its advantages are the decreased response time and independence from variations of the value of the input signal after the beginning of the synchronization.

The operation of q-PLL and p-PLL requires further analysis. Let the difference between the phases of the input and output signals is $\left(\vartheta-\hat{\vartheta}\right)$. Then the error signals in the control system of q-PLL and p-PLL are $U_M \sin\left(\vartheta-\hat{\vartheta}\right)$ and $U_M\left[1-\cos\left(\vartheta-\hat{\vartheta}\right)\right]$. Fig.1. shows the graphs of the two functions assuming that $U_M=1$. From those graphs the advantages and disadvantages of both PLLs can be seen, assuming that the parameters of the controller (usually PI-controller) are the same. A disadvantage of q-PLL is the presence of two equilibrium points – in phase and displaced to 180º to the input and output signals. Therefore, if the input signal is exactly displaced to 180º to the output signal and there are no disturbances, then theoretically the system reacts as if the synchronization in phase is reached and the signals would remain displaced to 180º. Actually, as a result of disturbances, warping from the second equilibrium point π, the phase synchronization starts with a time delay [37], [38]. The disadvantage of p-PLL using $\left[1-\cos\left(\vartheta-\hat{\vartheta}\right)\right]$ version is smaller values at phase angles smaller than 90° at and lower rate of change in this interval. This leads to a longer duration of the transient process and increased settlement time. The presented PLLis based on the idea that at any time should be used the bigger value if one of those two functions -"maximum trigonometrical" or "maximum p, q". Therefore, the input parameter for the PI- controller would run on the curves marked with arrows in Fig.1. If the initial phase difference $\left(\vartheta-\hat{\vartheta}\right)$ is less than 90°, then the system would respond $\sin\left(\vartheta-\hat{\vartheta}\right)$ as q-PLL. However, if the initial phase difference $\left(\vartheta-\hat{\vartheta}\right)$ is bigger than 90°, at the beginning the control system will respond $\left[1-\cos\left(\vartheta-\hat{\vartheta}\right)\right]$, i.e., as p -PLL, then it will go on $\sin\left(\vartheta-\hat{\vartheta}\right)$ as q-PLL. Therefore, in this system the advantages are the following: 1. It has only one equilibrium point – $\left(\vartheta-\hat{\vartheta}=0\right)$ the point $\left(\vartheta-\hat{\vartheta}=\pi\right)$ is missing. 2. In case of an initial difference exceeding 90° system response time is decreased, as it starts working with bigger error signal then passes along the curve, which corresponds also to this bigger error signal.

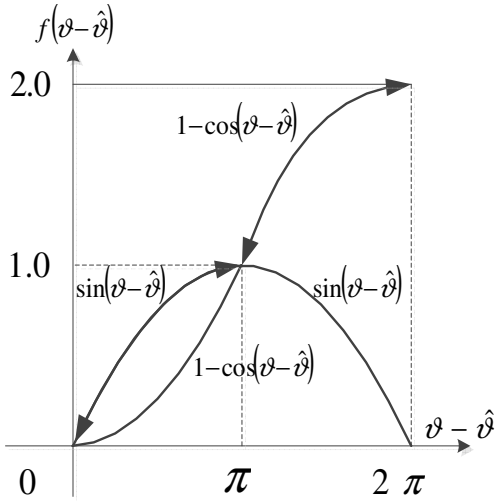

Fig.1. Functions comparison (error signals)

Part II presents a block diagram for the implementation of the proposed PLL, and Part III – computer simulation model. Part IV presents the results of the computer simulation.

2. BLOCK DIAGRAM

Fig.2 shows the block diagram for the implementation of three-phase Clarke-maximum trigonometrical PLL (3P Clarke-MaxTr PLL). It is based on the single-phase PLL described in [37], [38]. On this basis was carried Phase Detector1. Through this, component q which is one of the signals for the regulator – $U_M \sin(\vartheta - \hat{\vartheta})$ is obtained by means of the Park transformation. Compared to the single-phase PLL, in the block diagram of the 3P Clarke-MaxTr PLL, the Phase detector phase shift block is missing as the signal $(-U_M \cos\vartheta)$ is obtained from Clarke transformation, also, in VCO there is an additional block in order to obtain $(-1.\cos\hat{\vartheta})$, required for Clarke inverse transformation. Through the blocks of Phase Detector 2 component p is obtained by means of Park transformation – $U_M \cos(\vartheta - \hat{\vartheta})$. The block for maximum value is required for the comparison device, which output signal is the controller second signal – $U_M [1 - \cos(\vartheta - \hat{\vartheta})]$. The determination of the bigger error signal is in the Max Value Block. Thus by the use of signals U_α, U_β the synchronization starts at any time and at the initial phase of the three-phase system voltage input, and then is recovered by $\hat{U}_\alpha, \hat{U}_\beta$ using a Clarke inverse transformation. The steady state is achieved when the PI-controller input signal is equal to 0, which is achieved by equality of the phases and at the end of the settlement process corresponds to $\sin(\vartheta - \hat{\vartheta}) = 0$, since at the end the controller works as q-PLL.

For small values of the phase difference, the output signal of the phase detector 1 that uses the controller is:

$$U_{FD} \approx U_M (\vartheta - \hat{\vartheta}) \tag{1}$$

The transfer functions are the following:

$$\frac{dU_{PD}}{dt} \approx (\vartheta - \hat{\vartheta}).\frac{dU_M}{dt} + U_M . \frac{d\vartheta}{dt} \tag{2}$$

With respect to the phase of the input signal transfer function of the phase detector is:

$$W_{PD}(p) = \frac{U_{PD}(p)}{\vartheta(p)} \approx U_M \tag{3}$$

The transfer function of the open system is equal to:

$$W_O(p) = W_{PD}(p).W_{PI}(p).W_{VCO}(p) = U_M . K_P . \left(1 + \frac{1}{T_I . p}\right).K_{VCO} . \frac{1}{p} = \frac{U_M . K_P . K_{VCO}\left(p + \frac{1}{T_I}\right)}{p^2} \tag{4}$$

In (4) K_P and T_I are the coefficient of proportionality and the integration time constant of the PI-controller, and K_{VCO} – the coefficient of transmission of the VCO. Therefore, the system is of type 2 and the error in steady-state is zero at: step change of the input signal phase angle, linear phase change, step change of the input signal frequency.

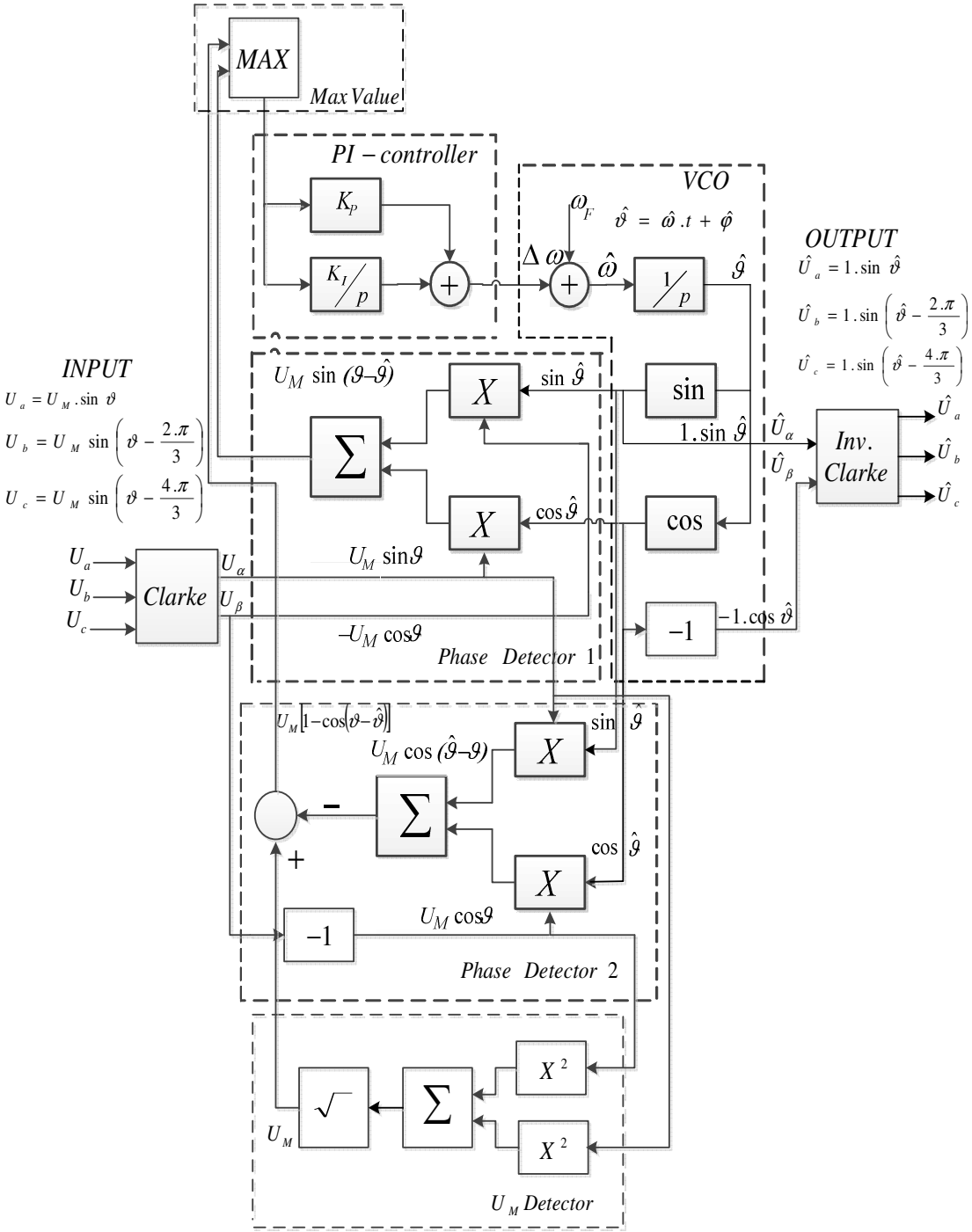

Fig.2. 3P Clarke-Max Tr PLL block diagram

3. COMPUTER SIMULATION MODEL

The software product PSIM is used for the research. The computer simulation model is presented in Fig.3. It is constituted by the above-described block diagram of Fig.2. The input signals of the whole system are denoted by Va, Vb, Vc, and the output – with Vao, Vbo, Vco. Blocks from the library of the software are used for Clarke direct and inverse transformations. The obtaining of

$U_M \sin(\vartheta - \hat{\vartheta})$ is achieved by the presented in [37] method and its output signal is denoted by Vq. Blocks to obtain $U_M \left[1 - \cos(\vartheta - \hat{\vartheta})\right]$ are added and marked in Fig.3 by Vp. To obtain this multiplier, the maximum value of the input voltage U_M is needed. It is obtained by U_α and U_β (denoted by Valfa and Vbeta) by the square root of the sum of their squared values. Then the signal $U_M \cos(\vartheta - \hat{\vartheta})$, marked as Vm in Fig.3, is subtracted from it. At the block Max is determined the maximum value of the signals Vp and Vq, which acts as Verror at the input of the PI-controller, the output signal of which is denoted by Vcontr.

4. COMPUTER SIMULATION RESULTS

The computer simulation is done at an effective value of the input voltage equal to 1V. PI-controller parameters are: $K_P = 10, T_I = 1ms$. The input signal frequency is 50Hz.

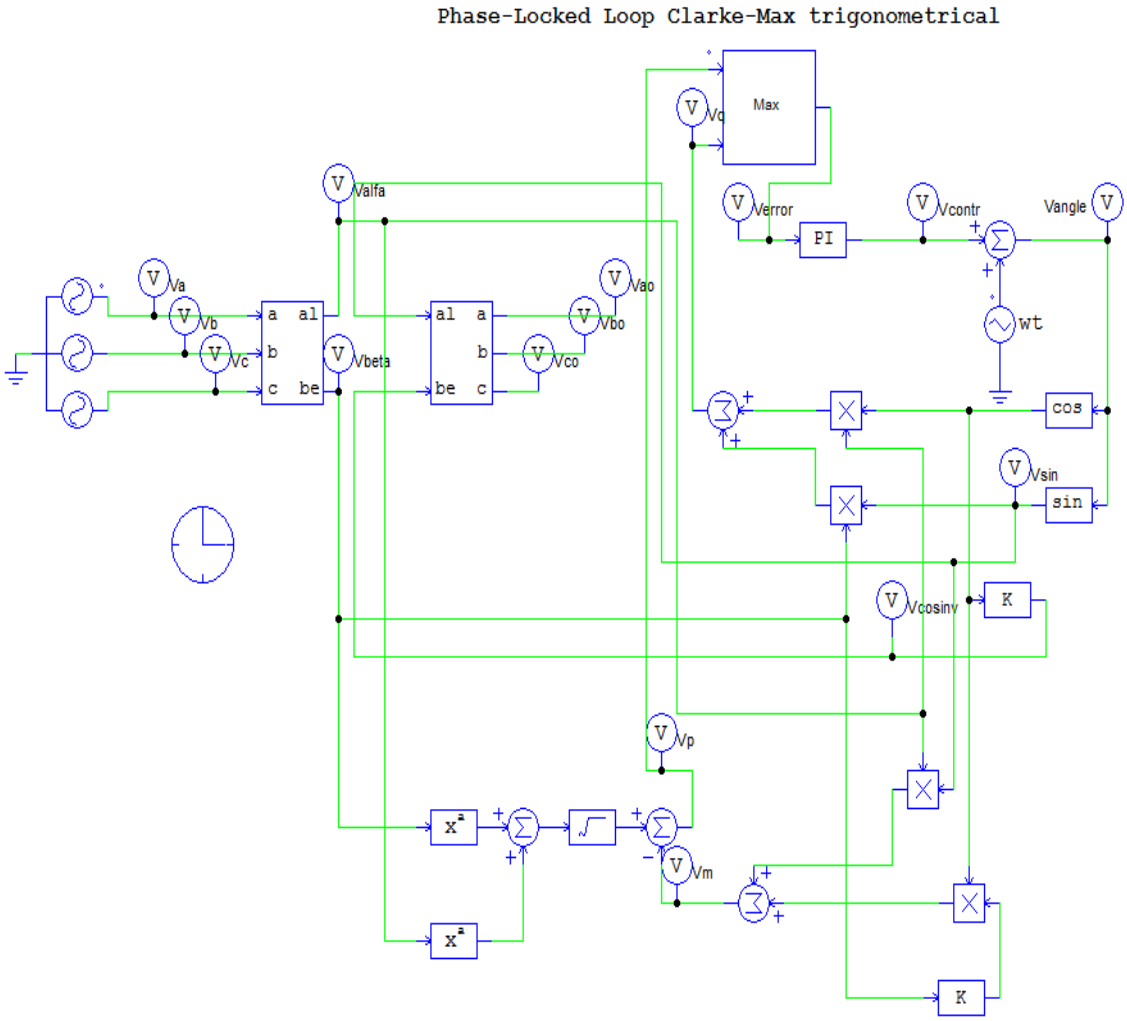

Fig.3. Computer simulation model

In Fig.4, Fig.5, Fig.6 and Fig.7 are presented computer simulation results for different initial phase angles from top to bottom: Va, Vb, Vc, Vao, Vbo, Vco; Verror and Vq; Verror and Vp.

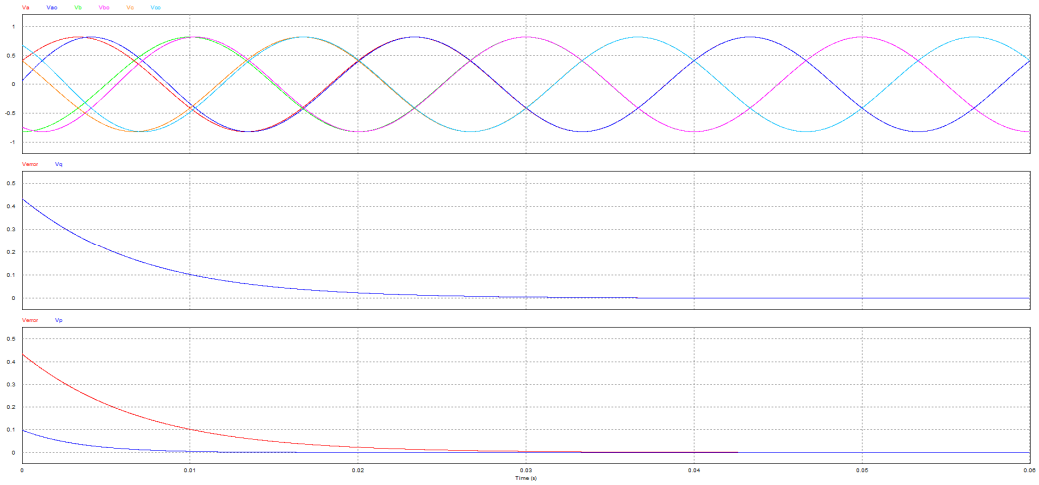

Fig.4. Initial phase angle 30° ; time span (0;60 ms)

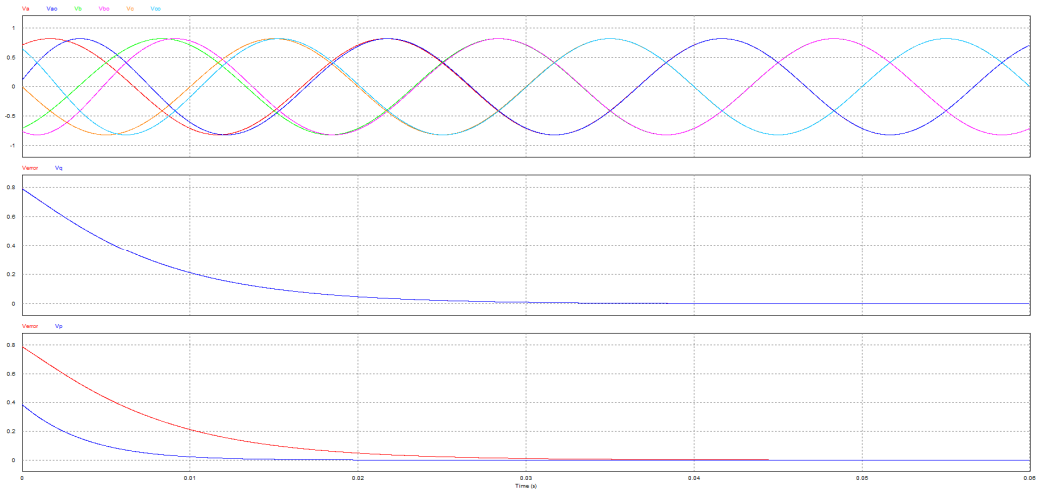

Fig.5. Initial phase angle 60° ; time span (0;60 ms)

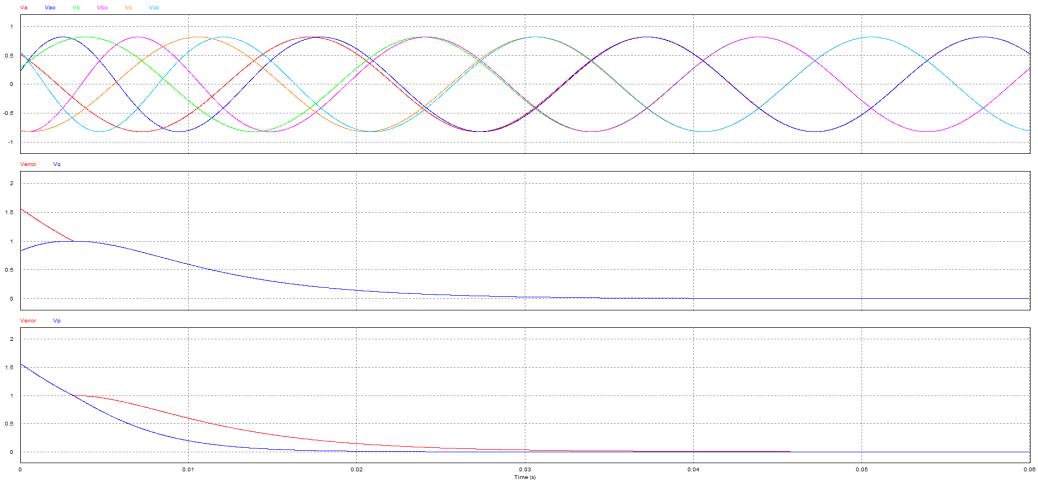

Fig.6. Initial phase angle 140° ; time span (0;60 ms)

According to the results of the computer simulation, the settling time at initial start is above 30ms, but the bigger the initial phase angle is, the longer the settling time is.

Then a simulation of the operation with only the component $U_M \sin\left(\vartheta - \hat{\vartheta}\right)$ and initial phase angle of 180° is done. PI-controller parameters are not modified. The result is presented in Fig.8. Input and output signals are in phase after 160ms with an important deformation around 115ms. However, a complete synchronization is obtained as the deviations around the second balance point π are due to the limited number of digits after the digital point of the values during the computer simulation.

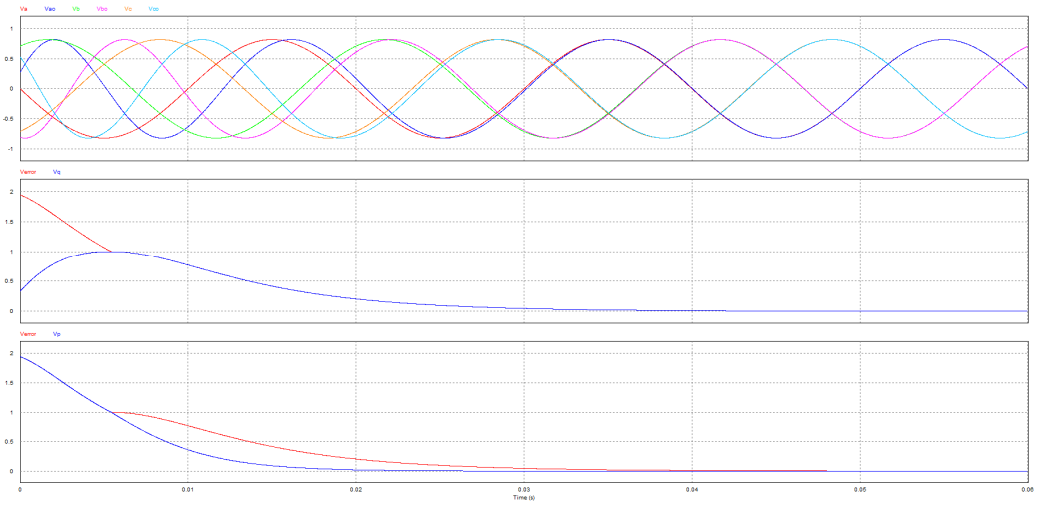

Fig.7. Initial phase angle 180° ; time span (0; 60ms)

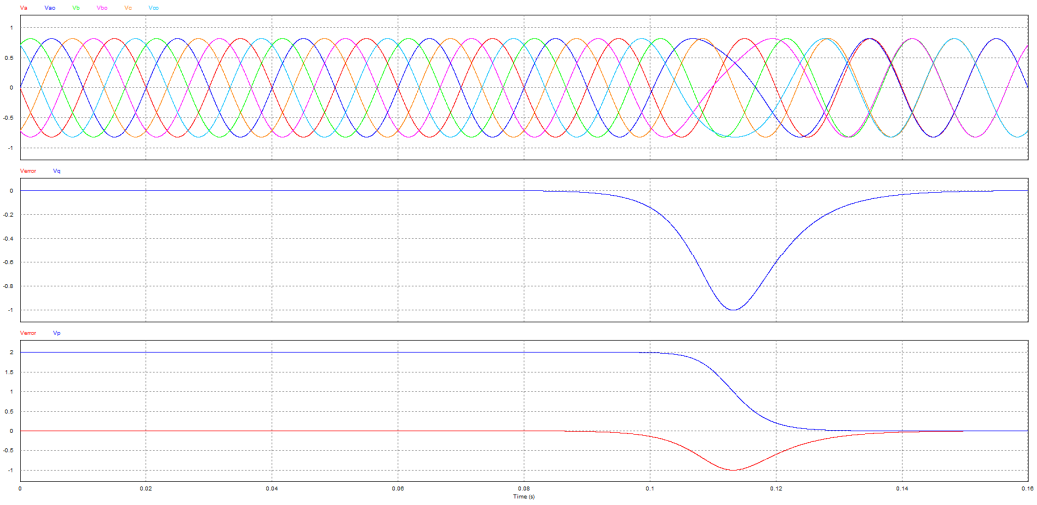

Fig.8. Initial phase angle 180° . Operation only with Vq – $V_{error} \equiv V_q$; time span (0; 160ms)

Then a simulation of the operation with only the component $U_M \left[1 - \cos\left(\vartheta - \hat{\vartheta}\right)\right]$ and initial phase angle of 180° is done. PI-controller parameters are not modified. The result is presented in Fig.9.

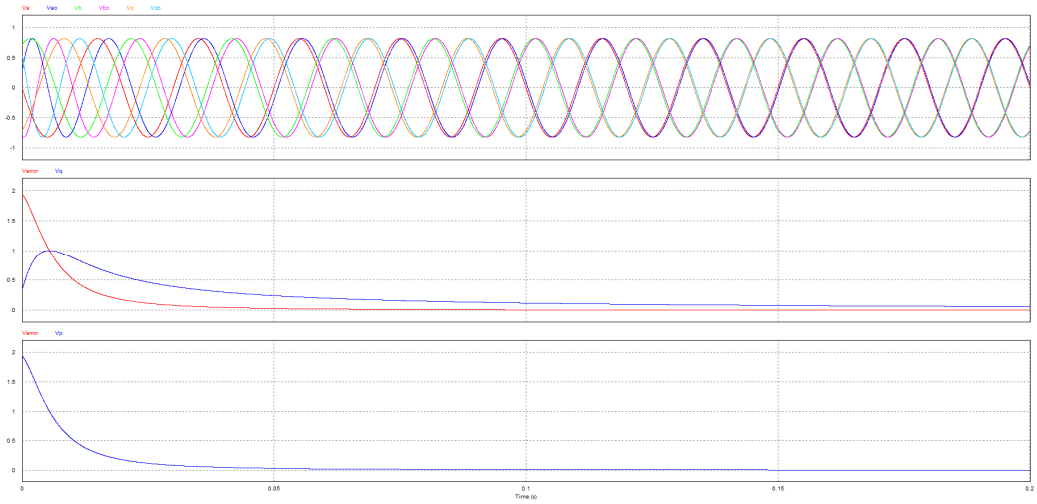

Fig.9. Initial phase angle 180°. Operation only with Vp – $V_{error} \equiv V_p$; time span (0; 200 ms)

Steady state is established for 200ms, as for long time – from 100 to 200ms, there are small deviations in the phases due to the slope of the curve $\left[1-\cos\left(\vartheta-\hat{\vartheta}\right)\right]$ close to 0.

5. CONCLUSION

From theoretical consideration and results of the computer simulation the main advantages of the proposed 3P Clarke-Max Tr PLL (3P Clarke-Max p, q PLL) are: 1. In case of initial difference bigger than 90º system response time is improved, as it starts to operate with bigger error signal then passes along the curve, which corresponds also to the bigger error signal. 2. Secure grip during initial phase angle also at increased performance.

The block diagram of Fig.3 shows the complex structure of the proposed PLL, which requires a more complicated implementation which is a kind of disadvantage. The implementation is possible for example on the basis of "System on Chip" (SoC).

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