Interconnect Parasitics and Reliability – Modeling and Analysis

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GLOBALFOUNDRIES
Agenda

Parasitic Extraction Overview

Parasitic Extraction Topic – RF/MMW Devices

Electromigration Overview

Electromigration Topic – Mission Profile

Electromigration Topic – Self Heat Analysis
Parasitic Extraction
Interconnect Parasitics

Interconnect RLC parasitics *strongly* contribute to the performance and reliability of integrated circuits.

Understanding parasitic RLC is crucial for predicting silicon circuit performance.
Parasitic Extraction

Parasitic extraction is the extraction of on-chip parasitic capacitances, resistances, and inductances from layout

Known as PEX or LPE (Layout Parasitic Extraction)

For device level extraction:

LVS (Layout Vs. Schematic) tool feeds connectivity, layer, and device details to PEX

PEX calculates and netlists parasitic RLC along with device information to a Spice Netlist or Extracted View
PEX – RLC Extraction

PEX tools use a pre-calibrated file to “look up” parasitic values based on the geometries in a design.

The pre-calibrated file, or deck, is part of a Foundry’s Process Design Kit (PDK).

PEX RLC calculation is fast and uses little memory as compared to an electromagnetic field solver.
PEX – Technology Description

Each PEX tool has a proprietary input file to describe the process

Includes information required to realize 3D on-silicon cross-section

Metal/via thickness, silicon width vs. drawn width/space/density
Dielectrics, resistivity
Ground rules to set calibration points
PEX – Conductor Example

Liners ($l_s$ and $l_b$) subtracted from drawn dimension for resistance calculation.

Sidewall angle included in determining parasitics.

Several additional factors influence silicon dimensions and conductor properties:

- Etch, OPC, **Retargeting**, Density, Cheesing, Scattering, etc.

Resistance = \( \frac{\rho \times \text{Length}}{\text{Cu Width} \times \text{Cu Height}} \)
PEX – Retargeting

Retargeting changes drawn design layers to new target dimensions

Performed post design submission to manufacturing

Must be accurately predicted in PEX to properly realize circuit performance
PEX – Multi-Patterning

Techniques like pitch splitting enable the reduction of metal feature sizes while extending the life of optical lithography.

Example: Single metal layer decomposed into 2 masks

PEX predicts the parasitic impacts due to these techniques, such as mask misalignment.
PEX – Deck Generation

PEX technology description files are fed to software that predetermines RLC based on potential layout structures

This technique includes thousands of field solver simulations to define rules or tables of parasitics vs. design scenario

Rules or tables are compiled into binary file(s) that are the input to PEX tools (decks)

Deck generation is a one-time CPU and memory intensive task performed by the Foundry

Includes predicting parasitics in and around FET devices
PEX – Accuracy Validation

Proven alignment of PEX, Independent Field Solver, and Silicon

Covering simple interconnect structures, devices, and circuits
PEX – RF/MMW Modeling

A parameterized cell (PCell) represents a device in layout.

For RF/MMW applications, the entire contents of the cell are characterized into a single compact model, including all conductor RC parasitics.

Critical to realize the correct boundary between PEX and compact model, and to extract parasitic coupling from outside the cell to inside the cell.
PEX – RF/MMW Modeling

Three techniques for proper handling of RF/MMW device parasitics

- Pcell Based
- Marker Layer Based
- Conductor Layer Based

Ignore Capacitance: $M1_{momcap} M2_{momcap}$
# PEX – RF/MMW Modeling

<table>
<thead>
<tr>
<th>Technique</th>
<th>PDK collateral complexity</th>
<th>Design hierarchy req’d</th>
<th>Compact model parasitic content equals PCell conductors</th>
<th>Different lateral and vertical coupling cap treatment</th>
<th>Device to device coupling cap</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conductor Layer Based</td>
<td>HIGH</td>
<td>NO</td>
<td>NO</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Marker Layer Based</td>
<td>MEDIUM</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td>Pcell Based</td>
<td>LOW</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
<td>YES</td>
</tr>
</tbody>
</table>
Electromigration
Electromigration

- "Electron wind" causes movement of metal atoms along wires
- Excessive electromigration (EM) leads to open & short circuits
- Most significant for unidirectional (DC) current.
- Black's equation on **Median Time to Failure** of a metal segment due to electromigration

\[
MTTF = \frac{A}{J^n} \cdot \exp\left(\frac{E_a}{k \cdot T}\right)
\]
EM – Analysis

EM is the gradual displacement of metal atoms when the current density is high enough to cause the drift of metal ions in the direction of the electron flow.

This density depends on the magnitude of forces that tend to hold the ions in place, i.e., the nature of the conductor, crystal size, interface and grain-boundary chemistry, and the magnitude of forces that tend to dislodge them, including the current density, temperature and mechanical stresses.

EM analysis solutions calculate current and compare with current limits.

Current is calculated for each metal segment / via and compared to limits set by Foundry.

Limits depend on circuit characteristics such as temperature and expected lifetime.
EM – Analysis Flow

PDK Components
- LVS
- PEX Techfiles
- Spice Models
- EMIR Techfiles
- Library

Analysis
- Layout vs Schematic
- Parasitic Extraction
- Post Layout Simulation
- EMIR/IR Drop Analysis & Results
- Visualization and Reporting

User Inputs
- Layout & Schematic
- Design Simulation Testbench
- EMIR Configuration File
- Library

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# EM – Current Types

## DC Current

<table>
<thead>
<tr>
<th>DC Current</th>
<th>Lifetimes</th>
<th>MTTF (Mean time to failure)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{dc}$ (Pulsed DC current)</td>
<td>Equivalent average dc current ($I_{avg}$)</td>
<td></td>
</tr>
</tbody>
</table>
| DC current stress induced failure | \[
\frac{S}{T_{sw}} \int_{0}^{T_{sw}} i(t) dt
\]

For the case of a pure ac current, $I_{dc}$ is zero.

$\frac{t}{T_{sw}} (\text{ShortLength}) = I_{dc} (\text{Calculated}) \times \left( \frac{L}{\text{Length}} \right)$

## AC Currents

### $I_{avg}$ (Average Current)

- **Lifetime**
- **MTTF (Mean time to failure)**

### $I_{rms}$ (Root mean square current)

- **Joule heating Impact**
- **Thermally induced EM failure**

### $I_{peak}$ (Peak Current)

- **Localized metal failure**

\[
I_{avg} (\text{falling}) = \frac{S}{T_{sw}} \int_{0}^{T_{sw}} I_{avg}(t) dt
\]

\[
I_{avg} (\text{rising}) = \frac{S}{T_{sw}} \int_{0}^{T_{sw}} I_{avg}(t) dt
\]

where, $S$ = Switching Factor

$T_{sw}$ = Period of one switching cycle (rising + falling)

$s / T_{sw} = \text{Feff}$, which means the effective frequency

\[
I_{rms} = \sqrt{\frac{S}{T_{sw}} \int_{0}^{T_{sw}} I^2(t) dt}
\]

Where, $S$ = Switching Factor

$T_{sw}$ = Period of one switching cycle (rising + falling)

$s / T_{sw} = \text{Feff}$, which means the effective frequency.

$T_d = \frac{\int_{0}^{T_{sw}} |I(t)| dt}{I_{peak, measured}}$

Where, $T_d$ = Period of one switching cycle

$I_{peak, measured} = I_{peak, limit} = \frac{I_{peak, dc, limit}}{\sqrt{r}}$

Where, $r$ is the duty ratio.
EM – Derating

Idc current limits depend on temperature (temp), product lifetime (EOL), and probability of failure (CDF)

Temp, EOL, CDF are known as derating factors

Product requirements determine appropriate temp/time/CDF

Traditionally, EM analysis is done at fixed value(s) of these derating factors
EM – Mission Profile

Reality – A product will run at various temperatures, for different time intervals, across their lifetime
Example: Automotive ICs

Optimal EM limits will account for varying temperature

Assuming highest temperature across timeline is too pessimistic

The temperature/time profile of a product is called its mission profile

Recent enhancements to EM solutions allow for a user to directly input a mission profile to the EM tool for checking their design against the exact Idc limits for their mission profile

<table>
<thead>
<tr>
<th>Temp(C)</th>
<th>Time(H)</th>
</tr>
</thead>
<tbody>
<tr>
<td>150</td>
<td>3600</td>
</tr>
<tr>
<td>145</td>
<td>4250</td>
</tr>
<tr>
<td>100</td>
<td>11430</td>
</tr>
<tr>
<td>60</td>
<td>5000</td>
</tr>
<tr>
<td>0</td>
<td>2000</td>
</tr>
</tbody>
</table>

Example User Input
EM – Self Heat Analysis

Temperature is not constant across wafer

Calculating Idc limits based on highest temperature across wafer can be too pessimistic

Especially true for applications with devices that produce significant heat such as photonics and MMW
EM – Self Heat Analysis

Local temperature influence on EM realized through a flow that couples localized device heating with metal/via Idc limit calculation

Define the increase in temperature for a given metal/via versus the increase in temperature for a device

Define the extent of the region around the device where a metal/via will experience an increase in temperature due to the device

For each metal segment/via, calculate the actual temperature and apply the associated Idc limit
Questions?

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And many more