Interconnect Parasitics and Reliability – Modeling and Analysis

Cole Zemke

GlobalFoundries, USA

Interconnect is a critical component of an integrated circuit, and accurately realizing the electrical characteristics and ensuring the reliability of interconnect is a necessity for a successful design.

This presentation will delve into Electronic Design Automation (EDA) solutions for interconnect, and how a Foundry's Process Design Kit (PDK) enables these solutions. This includes investigating Layout Parasitic Extraction (LPE) software and techniques that model interconnect resistance, capacitance, and inductance like actual silicon. In addition, electromigration concerns and verification methodologies will be discussed. The importance of these topics to applications such as automotive, MMW, and photonics will be examined.