



ВИДОВЕ ТРАНЗИСТОРИ С НАНОРАЗМЕРЕН ПРОВОДЯЩ КАНАЛ

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Резюме: *Направен е анализ на типовете MOSFET транзистори с наноразмерен проводящ канал. Този тип транзистори имат голям потенциал за полупроводниковата индустрия и микроелектронните системи. Статията е фокусирана върху типове транзистори с наноразмерен проводящ канал от въглеродна нанотръба (CNT), силиций (Si), цинков оксид (ZnO), индиев арсенид (InAs), двуиндиев триоксид (In₂O₃), галиев антимонид (GaSb) и галиев нитрид (GaN). Разгледана е структурата и технологията на различните видове.*

Ключови думи: транзистор с въглеродна нанотръба, нанотръба, нанопроводник

OVERVIEW OF NANOWIRE FIELD-EFFECT TRANSISTORS

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Abstract: *An overview of the different types of nanowire MOSFETs which have large potential to semiconductor industry and microelectronic systems is presented. The present paper is focused on the type of nanowire FETs with carbon nanotube (CNT), Silicon (Si), Zinc Oxide (ZnO), Indium Arsenide (InAs), Indium Oxide (In₂O₃), Gallium Antimonide (GaSb), Gallium Nitride (GaN) channel. The current paper presents the structure and technology of the various types of Nano Wire MOSFET.*

Key words: CNTFET, nanotube, nanowire

1. Introduction

With their unique electrical and optical properties, semiconducting nanowires offer interesting perspectives for basic research as well as for technology. Device scaling is critical for continuing trend of more functionality in a chip. As the scaling of Si MOSFET approaches towards its limiting value, new alternatives are coming up to overcome these limitations. Many types of transistors with nanomaterials in the channel are studied so far, e.g. Carbon NanoTube Field-Effect Transistor, Silicon (Si) nanowire transistors, Gallium Antimonite (GaSb) nanowire transistors, Gallium Nitride (GN) nanowire transistors, Zinc

Oxide (ZnO) nanowire transistor, Indium Oxide (In₂O₃), Indium Arsenide (InAs), etc.

2. Carbon nanotube Field Effect Transistors - CNTFETs

The carbon nanotubes (CNT) are one of the most important new materials with excellent mechanical and electrical properties. The main advantage of a MOSFET with graphene channel is its high carrier mobility. CNTFET so far can be classified into: Back-gated CNTFET's [1], [5], Top-gate CNTFET's [11], [10], Wrap-around gate CNTFET's [2], Multi-Wall CNTFET [13], Vertical CNTFET [6], Local gated CNT FET devices [14],

[15], multichannel Carbon nanotube FET [3]. One device fabricated with CNTs that has been highly examined is the carbon nanotube field-effect transistor, comprised of single-wall CNTs (SWCNTs) as the active element between two metal source and drain contacts. There are many advantages to the CNTFET, such as size, high sub-threshold slope, and low power consumption. There are two main methods for CNT creation: CVD Growth и CNT Solution Deposition.

3. Silicon NanoWire Transistors

Type 1. Silicon nanowires can be prepared with single-crystal structures, diameters as small as several nanometers and controllable hole and electron doping, and thus represent powerful building blocks for nanoelectronics devices such as field effect transistors. Thermal annealing and passivation of oxide defects using chemical modification were found to increase the average transconductance from 45 to 800 ns and average mobility from 30 to 560 $\text{cm}^2/\text{V}\cdot\text{s}$ with peak values of 2000 ns and 1350 $\text{cm}^2/\text{V}\cdot\text{s}$, respectively. Figure 1 shows schematic of a SiNW FET showing metal source and drain electrodes with the NW and contacts on the surface of SiO_2/Si substrate. High-resolution transmission electron micrograph of a 5 nm diameter SiNW; the scale bar is 5 nm. Figure 1 (B) shows scanning electron micrograph of a SiNW FET device; the scale bar is 500 nm. Thermal annealing and passivation of oxide defects by chemical modification were found to increase the average transconductance from 45 to 800 ns and average mobility from 30 to 560 $\text{cm}^2/\text{V}\cdot\text{s}$ with peak values from 2000 ns and 1350 $\text{cm}^2/\text{V}\cdot\text{s}$, respectively. Comparison of these results and other key parameters with state-of-the-art planar silicon devices shows substantial advantages for the SiNWs as building blocks [4].

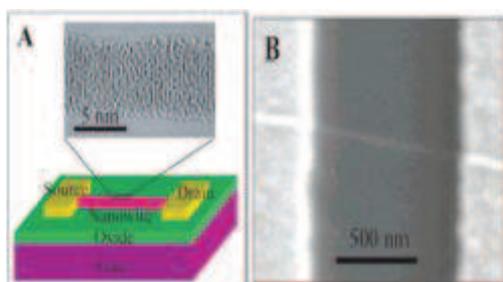


Fig. 1. Schematic of a SiNW FET [4].

Type 2. Here is demonstrated an atomic force microscopy lithography that enables the reproducible fabrication of complex single-crystalline silicon nanowire field-effect transistors with a high electrical performance. The nanowires have been carved from a silicon-on-insulator wafer by a combination of local oxidation processes with

a force microscope and etching steps. The silicon nanowire transistor is fabricated with a channel width of 4 nm. Fig. 2 shows images of a multiple-level SiNWs transistor. The device is formed by two perpendicular SiNW. Fig. 2 (a) shows amplitude modulation AFM image of the local oxide mask fabricated with the AFM. Fig. 2 (b) shows amplitude modulation AFM image of two perpendicular SiNWs (A-B and C-D) obtained after etching with KOH. Fig. 2 (c) shows optical image of the final device [12].

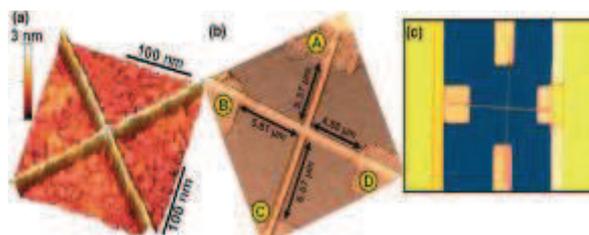


Fig 2. Images of a multiple-level SiNWs transistor[12].

Type 3. Here is demonstrated vertical surround-gate field-effect transistor VS-FET. Exemplarily, Si nanowires are used and present a first electrical characterization proving the feasibility of the process developed and the basic functionality of this device [17].

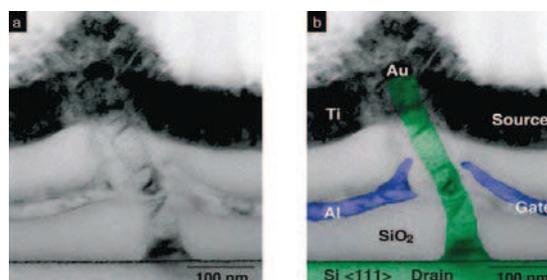


Fig. 3. a) TEM of a silicon nanowire VS-FET) . b) Colored TEM image (green: silicon, blue: aluminum)[17]

Type 4. This type presents the first attempt to fabricate two transistors on a single vertical silicon nanowire (Fig.4) realizing true 3-D integration. The fabricated device architecture, having two independently controlled MOSFETs connected in series, does not occupy any additional planar area except an extra gate contact. Consequently, compared with the single vertical nanowire transistor, the stacked MOSFETs provided the two input AND gate functionality with 50% area savings. The drain current I_D could be modulated by either of the gate biases without impacting the V_T of the other transistor in the stack. Furthermore, the tunability of the separation between the two gates, which is 7 nm in the current demonstration, makes the presented device

architecture promising for implementing electrically doped tunneling FET (TFET) and stacked SONOS memory cells [14].

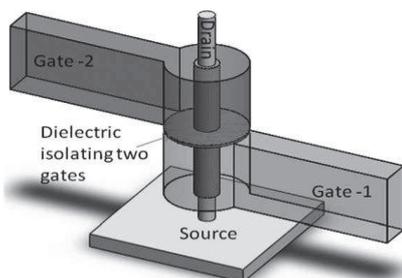


Fig. 4. Schematic showing the 3-D view of the stacked vertical twin-gate nanowire MOSFET [14].

4. ZnO Nano Wire Transistors

Type 1. This type demonstrates all solution processed, low-temperature ZnO NW transistor fabrication processes on polymer substrates by combining two different NP (Au and ZnO) based solution processes - Au NP direct nano imprinting and the ZnO NW synthesis on ZnO NP seeds. The ZnO NW network transistor (NWNT) fabrication process consists of two main steps: (1) source-drain electrode fabrication by the direct nanoimprinting of Au NPs and (2) hydrothermal ZnO NW growth from ZnO NP seeds in aqueous ZnO precursors. Both steps are low-temperature ($T_{max} < 140^{\circ}C$), NP based solution processes. These characteristics make this technique directly applicable to low-cost, solution processed electronics on inexpensive polymer substrates (Fig. 5) [16].

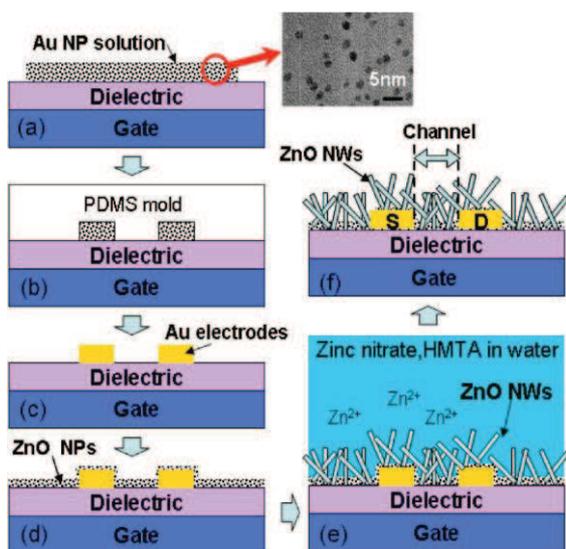


Fig. 5. Schematic illustration of the ZnO NW network FET fabrication process [16].

5. InAs Nano Wire Transistors

Type 1. InAs NWs are synthesized on Si/SiO₂ substrates by a physical vapor transport method using Ni nanoparticles as the catalyst. The

grown InAs NWs were over 10 μm long with a radius range of 7-20 nm. The NWs are single crystalline with a native oxide thickness of 2-2.5 nm. Energy dispersion spectrometry (EDS) indicates that the chemical composition of In:As is close to 1:1. Field-effect transistors in a back-gated configuration were fabricated, for the electrical transport measurements (Figure 6, panels a-b) [7].

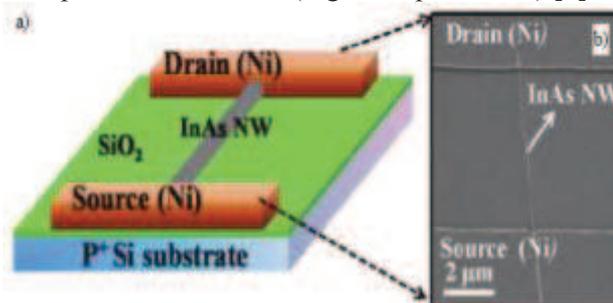


Fig. 6. (a) A top-view schematic of a global back-gated NW FET, used for the I-V characterization. (b) SEM image of a representative back-gated NW FET [7].

6. In₂O₃ Nano Wire Transistors

Type 1. In this study, the channel length was altered by placing a conducting atomic force microscopy (CAFM) tip at various positions along an In₂O₃ nanowire. The In₂O₃ nanowires were prepared by carbothermal reduction followed by a catalyst-mediated heteroepitaxial growth technique. A detailed description of the synthesis of In₂O₃ nanowires has been reported elsewhere. Fig. 7(a) shows a typical field-emission scanning electron microscopy (FE-SEM) image of In₂O₃ nanowires grown on the Si/SiO₂ substrate. Note that the high-resolution TEM (HRTEM) image shown in fig. 7(b) indicates that the In₂O₃ nanowire is a single crystalline material with an interplanar spacing of 0.5 nm in the (100) direction. The electron diffraction pattern was recorded along the (001) zone axis, as shown in the inset of fig. 7(b). Figure 7 (c) shows schematic of the CAFM setup for characterizing an In₂O₃ nanowire FET. The channel length of the In₂O₃ nanowire FET was varied from 1 μm to 20 nm. Figure 7(d) shows the AFM image of the In₂O₃ nanowire FET device with diameter of 25 nm. The CAFM tip was positioned on the nanowire at specific locations (a=1 μm , b=500 nm, c=200 nm, d=50 nm, and e=20 nm). Note that the AFM image (Fig. 7(d)) was obtained after the completion of the CAFM experiments in order to avoid potential damage to the nanowire by the CAFM tip [8].

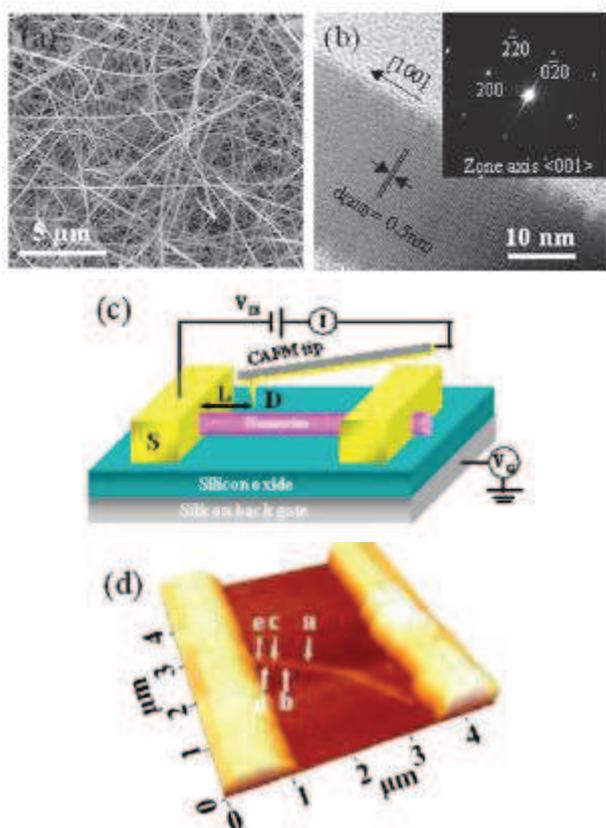


Fig. 7. (a) FE-SEM image of In_2O_3 nanowires. (b) HRTEM image of an In_2O_3 nanowire. (c) Schematic of the CAFM setup for characterizing an In_2O_3 nanowire FET. (d) AFM image of the In_2O_3 nanowire FET device characterized [8].

7. ZnO Nano Wire Transistors

Type 1. ZnO nanowire field-effect transistors (FETs) were fabricated and studied in vacuum. In air, these n-type nanowire transistors have some of the highest mobilities yet reported for ZnO FETs ($\mu_e = 13 \pm 5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$), with carrier concentrations averaging $5.2 \pm 2.5 \times 10^{17} \text{ cm}^{-3}$ and on-off current ratios ranging from 105 to 107. Four probe measurements show that the resistivity of the Ti/Au-ZnO contacts is $0.002\text{-}0.02 \Omega \cdot \text{cm}$. Figure 8 is a scanning electron microscope (SEM) image of a typical ZnO nanowire FET [9].

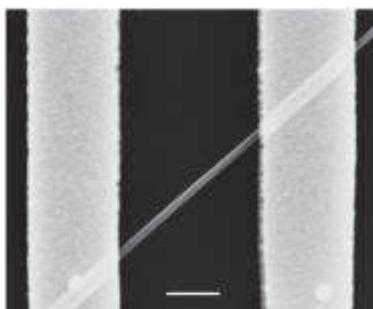


Fig. 8. SEM micrograph of a 101 nm diameter ZnO nanowire device [9].

8. GaSb Nano Wire Transistors

Type 1. Single GaSb Nanowire Field Effect Transistors (NWFETs) were fabricated (fig. 9). Among III-V compound semiconductors, GaSb has the potential to be a promising candidate for high speed electronic and photonic applications in the mid-infrared region. This is due to its high hole mobility of GaSb ($850 \text{ cm}^2/\text{Vs}$) and wide range of band gaps available for GaSb-based alloys with spectra range from ~ 0.3 to 1.58 eV ($0.8\text{-}4.3 \mu\text{m}$). The synthesis of GaSb nanowires has been studied and the one-dimensional (1D) geometry of nanowires is ideal building block for transistor devices [20].

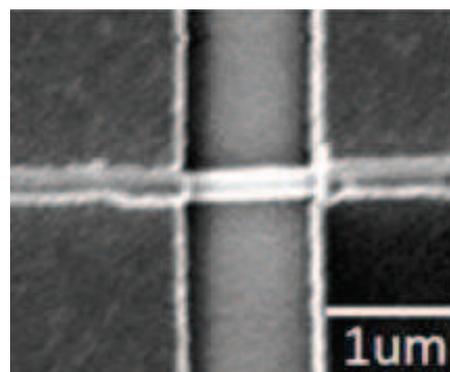


Fig. 9. Typical SEM image of one nanowire device. The gap between the electrodes is $1 \mu\text{m}$ [20].

The crystalline GaSb nanowires characterized in this work are synthesized using the self-catalyzed vapor-liquid-solid approach. Pools of gallium supported on amorphous quartz substrates are employed for this purpose. Antimony is supplied through the vapor phase from a solid antimony source by using 10% hydrogen in argon as the carrier gas. The dissolution and subsequent supersaturation of the molten gallium droplets formed on the substrate with antimony lead to the multiple nucleation and growth of GaSb nanowires. Following growth, the nanowires are removed from the growth substrates and suspended in isopropanol solution. The so grown GaSb nanowires were then drop cast from isopropanol dispersion onto an oxidized silicon substrate. 200 nm SiO_2 is thermally oxidized on top of a heavily p-doped silicon substrate, which serves as a global back gate. Cr/Au electrodes were patterned on top of each individual nanowire using JEOL 6000 FS Electron Beam Lithography to define the features in a 600 nm thick polymethylmethacrylate (PMMA) layer spun on the surface of the substrate. The patterned PMMA films were metalized by thermally evaporating 15 nm Cr and 200 nm Au . After lift-off procedure, the as-fabricated devices were annealed under forming gas environment (Nitrogen 95%, Hydrogen 5%) at 300°C for 30 minutes [20].

9. GaN Nano Wire Transistors

Type 1. The focus of this research was to demonstrate the use of gallium nitride (GaN) nanowires to fabricate a CMOSFET using the nanowire as the conducting channel (fig. 10.). Fabrication of the nanoFET was initiated with a low resistant, highly doped silicon (Si) wafer, which was cut into two one-inch-pieces. These Si wafers were then thermally oxidized in a quartz furnace at 1100°C to form a layer of silicon dioxide (SiO₂), which will be used as the gate dielectric. SiO₂ layers of thickness between 275-300 nm were used. To form the gate contact, a 150 nm thick aluminium (Al) ohmic contact layer was deposited onto the backside of the Si wafer by electron beam evaporation. To protect the layer during subsequent fabrication processes, a layer of photoresist was spun onto the surface and baked for 30 min. Employing photolithography, the source and drain electrodes for the nanoFET were defined atop the SiO₂ layer. We then evaporated 150 nm of Al, or gold (Au), over this surface. A liftoff process was then used to form the source drain contacts. The mask used in this work was specifically designed to maximize the probability of getting nanowires across the source and drain. The GaN nanowires used were grown in house and measured roughly 50 nm in diameter and 10-100 μm in length [18].

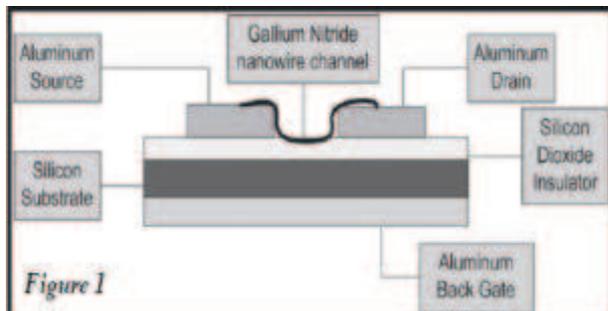


Figure 1
Fig. 10. GaN Nanowire Transistors [18].

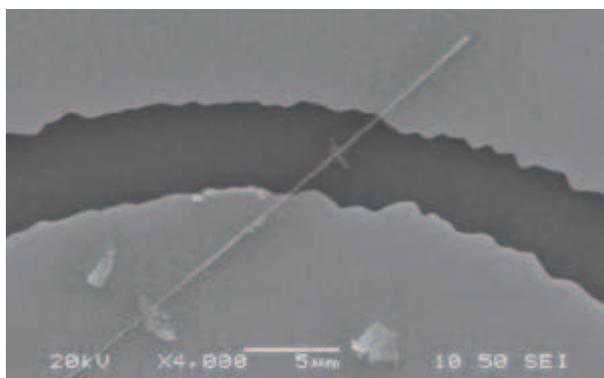


Fig. 11. Scanning electron microscope [18]

The solvent was allowed to evaporate, and the sample was then examined under an optical microscope and a scanning electron microscope to

confirm nanowire placement on the source-drain contacts (Fig. 11) [18].

10. Conclusion

This paper presented an overview of the Nanowire Field Effect Transistors structures depending on the type of nanowire and device architecture. The present study was focused on the type of nanowire FETs with Carbon Nanotube (CNT), Silicon (Si), Zinc Oxide (ZnO), Indium Arsenide (InAs), Indium Oxide (In₂O₃), Gallium Antimonide (GaSb), Gallium Nitride (GaN) channel. Nanowire MOSFETs are viewed as the most promising material for the upcoming nanoelectronic transistors. However, the Nanowire MOSFETs field is still in an early stage of development.

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REFERENCE

1. Aikawa, S., Einarsson, E., Inoue, T., Xiang, R., Chiashi, S., Shiomi, J., Nishikawa, E., Maruyama, S. "Simple Fabrication Technique for Field-Effect Transistor Array Using As-Grown Single-Walled Carbon Nanotubes", *Japanese Journal of Applied Physics* 50 (2011), pp.04DN08(1-4)
2. Chen, Z., Farmer, D., Xu, S., Gordon, R., Avouris, P., Appenzeller, J. "Externally Assembled Gate-All-Around Carbon Nanotube Field-Effect Transistor", *IEEE electron device letters*, VOL. 29, NO. 2, February 2008 pp. 183-185
3. Chen, C., Xu, D., Kong, E., Zhang, Y., "Multichannel Carbon-Nanotube FETs and Complementary Logic Gates With Nanowelded Contacts", *IEEE Electron Device Letters*, Vol. 27, No. 10, October 2006, pp. 852-855
4. Cui, Y. Z., Zhong, D., Wang, W., Wang, Ch. Lieber "High Performance silicon nanowire Field Effect Transistors" *Nano lett.*, Vol. 3, No. 2, pp. 149-153, 2003.
5. Derycke, V., Martel, R., Appenzeller, J., Avouris Ph. "Carbon Nanotube Inter- and Intramolecular Logic Gates" *American Chemical Society*, Vol. 1, Num. 9, pp 452-456, September 2001.
6. Franklin, A., Sayer, R., Sands, T., Fisher, T., Janes, D. "Toward surround gates on vertical single-walled carbon nanotube devices" *Mar/Apr 2009, American Vacuum Society*, DOI: 10.1116/1.3054266, pp 821-826

- 7. Ford A., Ho J., Y. Chuen, Y. Tseng, Z. Fan, J. Guo, J. Bokor, A. Javey,** „Diameter-dependent electron mobility of InAs Nanowires” American Chemical Society, Nano Letters, Vol. 9, No. 1, pp. 360-365, 2009
- 8. Gunho, J., Jongsun M., Tae-Wook K., H. Woong-Ki, J. Minseok, H. Hyunsang, L. Takhee** „Effects of channel-length scaling on In₂O₃ nanowire field effect transistors studied by conducting atomic force microscopy” American Institute of Physics, Applied physics letters 90, pp.173106-1 – 173106-3, 2007
- 9. Goldberger, J., Sirbuly D., Law M., Yang P., „ZnO Nanowire Transistors”** The journal of physical chemistry, B. Letters, pp. 9-14, 13 december 2004
- 10. Hu, Y., Yao, K., Wang, S., Zhang, Z., Liang, X., Chen, Q., Peng, L.** "Fabrication of high performance top-gate complementary inverter using a single carbon nanotube and via a simple process", *American Institute of Physics*, Applied Physics letters 90, 223116, 2007, pp. 223116 (1-3)
- 11. Lin, H., Park, Y., Tiwari, S.** "A Compact Single-Walled Carbon Nanotube Transistor Integrated with a Silicon MOSFET Using a Single Common Gate", *Materials Research Society* 2007, Vol. 963
- 12. Martinez, J., R.V. Martinez, R. Garcia** "Silicon Nanowire Transistors with a Channel Width of 4 nm Fabricated by Atomic Force Microscope Nanolithography" American Chemical Society, pp. 3636-3639, Vol. 8, No.11, 2008
- 13. Shun, M., Ganhua L., Kehan, Y., Junhong, Ch.,** "Specific biosensing using carbon nanotubes functionalized with gold nanoparticle-antibody conjugates" Elsevier Ltd. All rights reserved, September 26, 2009, pp. 479-486
- 14. Stokes, P., Khondaker, S.** "Local-gated single-walled carbon nanotube field effect transistors assembled by AC dielectrophoresis" University of Central Florida, Department of Physics, Orlando , USA
- 15. Svensson, P., Tarakanov, T., Lee, D., Kinaret, K., Park, Y. Campbell. B.,** "A carbon nanotube gated carbon nanotube transistor with 5 ps gate delay" IOP publishing, Online at stacks.iop.org/Nano/19/325201
- 16. Seung K., Inkyu P., P.Heng, M. Nipun, M. Rogers, C. Grigoropoulos, A. Pisano,** „ZnO nanowire network transistor fabrication on a polymer substrate by low-temperature, all-inorganic nanoparticle solution process”, Applied Physics Letters, Vol. 92, pp. 154102-1 - 154102-3, 2008
- 17. V. Schmidt, R. Heike, S. Senz, S. Karg, W. Riess, U. G3sele,** „Realization of a Silicon Nanowire Vertical Surround-Gate Field-Effecs Transistor” *Nano Small Micro*, Vol.2, No.1, pp. 85-88, 7 November, 2005.
- 18. Wingfield, A.** "Fabrication of a Gallium Nitride Nano-Field Effect Transistor" NNIN REU Research Accomplishments, pp.80-82, 2010
- 19. Xiang L., Ch. Chixian, Sh. Nansheng, D. Sarkar, N. Singh, K. Banerjee, G. Lo, D. Kwong** „Vertically Stacked and Independently Controlled Twin-Gate MOSFETs on a Single Si Nanowire”, IEEE Electron Device Letters, pp. 1492-1494, Vol.32, No.11, November 2011.
- 20. Xu, W., Chin A.,Y. Laura, N. Cun-Cheng, Y. Hongbin,** "Electrical and optical characterization of individual GaSb nanowires”, Proc. Of SPIE Vol. 7224, pp. 72240G-1 – 72240G-7, 2009

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