MODIFIED DRAM CELL DESIGN USING HIGH-K MOS CAPACITOR

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Abstract

In the present paper a modified 3T DRAM cell is simulated using a Verilog-A model of a high-k stack MOS capacitor from HfO_2-Ta_2O_5. The results showed better performance than the original circuit.

1. Introduction

Scaling of silicon dioxide dielectrics enabled the constant increasing of transistor performance in CMOS technologies as predicted by Moore's law [1]. The reduction of devices under 45 nm technology node, the effective oxide thickness (EOT) of the traditional silicon dioxide dielectrics are required to be smaller than 1 nm, which is approximately 3 monolayers and close to the physical limit. To continue the downward scaling, dielectrics with a higher dielectric constant (high-k) are considered as a solution to achieve the same transistor performance [2]. Hf-based oxides have been recently highlighted as the most suitable dielectric materials because of their comprehensive performance. In this paper we present a modified circuit schematic of a DRAM cell and applied a model developed in [MIXDES2011] to simulate its behavior. The model describes a high-k MOS stack structure from [3].

2. Schematic

We have implemented the capacitor model developed in Verilog-A code in a DRAM circuit consisting of two memory cells and a sense amplifier. The circuit is taken from US Patent No. US 6,426,905 B1, Jul. 30, 2002 [4].

The above described sensitive amplifier circuit uses one-transistor DRAM memory cells. We have modified the one-transistor DRAM memory cell (Fig.1) to a three-transistor memory cell (Fig.2).

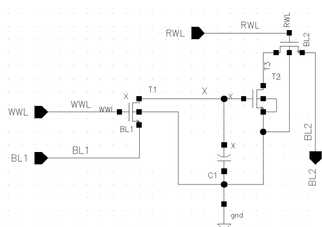


Fig. 1. 3T cell

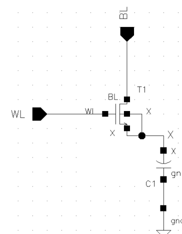
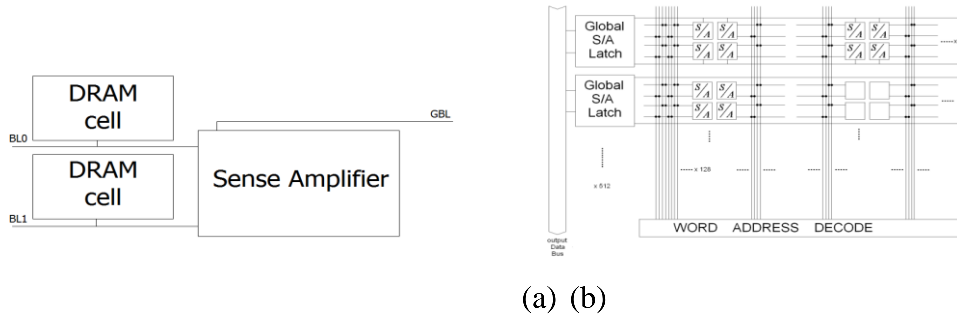


Fig. 2. 1T cell

The block diagram of the DRAM memory circuit includes memory cells connected to sensitive amplifiers via local bitlines and these sensitive amplifiers are in their turn connected to global bitlines (Fig.3) [4].



(a) (b)

Figure 3. (a) Block Diagram of the memory cell with sensitive amplifier; (b) A typical layout and construction of such a DRAM macro utilizing the High Speed DRAM Local Bit Line Sense Amplifier (Block Diagram of Word Address Decode).

Each of the Local Bit Line Sense Amps shown as box in Fig.3(b) denoted with “S/A” is connected to two local bitlines and one global bitline (as shown in Fig.3(a)) and is accessed by M wordlines. DRAM memory cell is accessed by selecting respective wordline and bitline [4].

In Fig.4 is shown the schematic of the local bitline sensitive amplifier of Fig.3. The schematics of the DRAM memory cell is shown in Fig.1.

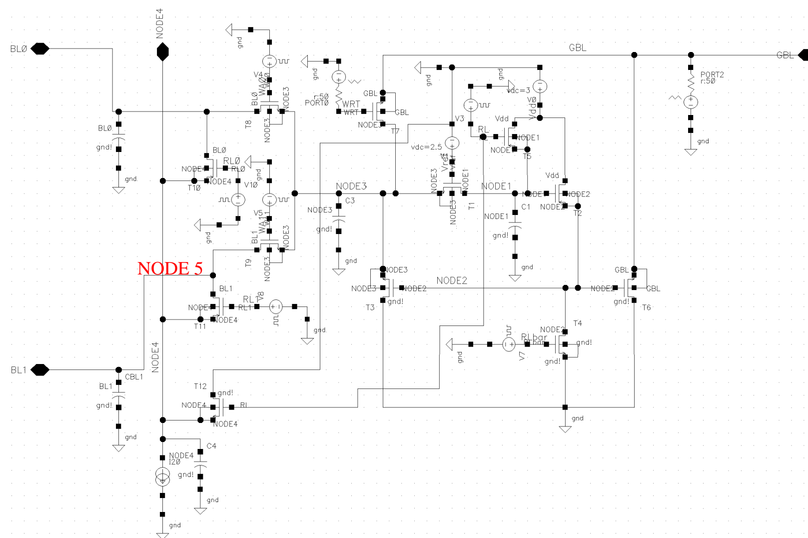


Figure 4.Local bitline sensitive amplifier schematic.

The local bitline sensitive amplifier is comprised of CMOS transistors T1 to T11. Connected to the local bitline sensitive amplifier are two DRAM memory cells.

3. Simulations

In order to demonstrate the applicability to real circuit simulations of the Verilog-A model of the high-k HfO_2-Ta_2O_5-based MOS capacitor this model is implemented in Cadence Spectre simulator as external code. The simulation results with this model are compared to the simulation results with standard Cpoly capacitor from the S35D3 technology of the 0.35-µm CMOS design kit of AMS. The HfO_2-Ta_2O_5-based MOS capacitor is modeled by modifying the standard BSIM3v3 model of the standard MOS capacitor within the 0.35-µm CMOS design kit of AMS in Verilog-A.

Transient characteristics of READ and WRITE cycles are given in Fig. 5(a) (b) (c) (d). They are obtained setting the geometry dimensions and capacitor values listed in Tables 1 and 2.

$C_{X0,1}$ (fF)	C4 (pF)	C3 (fF)	CBL0 (fF)	CBL1 (fF)
100	500	70	30	30
100	500	90	10	10
100	500	60	40	40

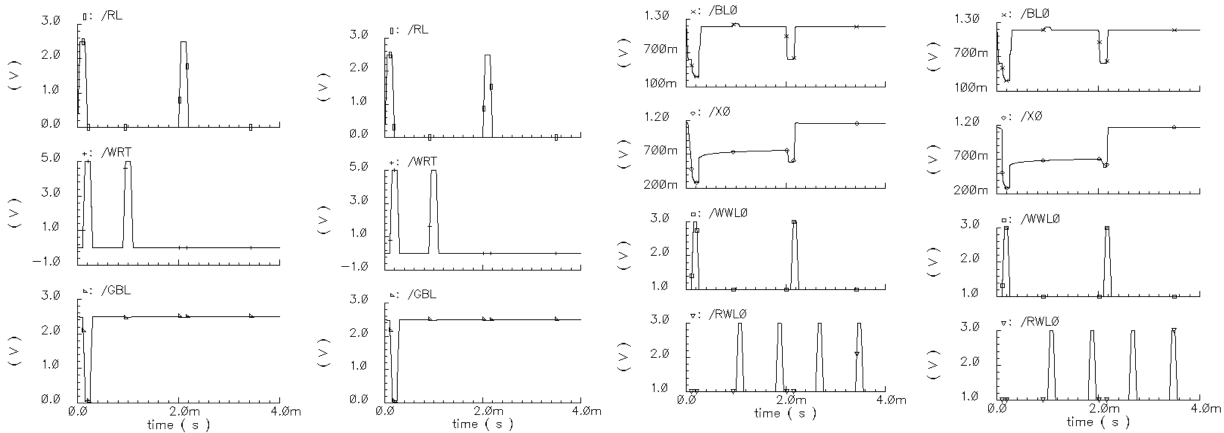
Table 1. Parameters of the storage capacitor Cploy (the standard capacitor of the 0.35 μm CMOS design kit)

L (μm)	W (μm)	$C_{X0,1}$ (fF)	C4 (pF)	C3 (fF)	CBL0 (fF)	CBL1 (fF)
100	100	111.2	500	70	30	30
200	200	444.3	500	70	30	30
300	300	994.8	500	70	30	30
100	100	111.2	500	90	10	10
200	200	444.3	500	60	40	40

Table 2.Parameters of the high-k MOS capacitor.

The value of

CBL0 (CBL1) + C3 = 100fF



a) Cpoly capacitor b) MOS capacitor c) Cpoly capacitor d) MOS capacitor

Figure 5. Comparison between Input signals RL (restore clock), WRT (write enable), and GBL (Global Bit Line) and between output signals from BL0 DRAM cell of Fig. 1 and Write Word Line 0 and Read Word Line 0 at the storage capacitor Cpoly (the standard capacitor of the 0.35 μm CMOS design kit) and the high-k storage MOS capacitor.

The read and write cycles of the Verilog-A modeled capacitor and the standard Cpoly capacitor are compared in Fig.5(a) (b). In write operation RL is at high, is submitted the clock for write WRT at the same time Global Bit Line - GBL is pulled to ground. After second clock of the WRT pass reading mode. In read operation RL again is at high, WRT is at low, and GBL is at high to the next write operation. In write operation WRT (WRT is the "write enable" clock signal) is at high level (Fig.5(a) (b)). The restore clock signal RL is high (it equals to Vdd). It turns OFF the T4 and T5 transistors in Fig. 4. At the same time Global Bit Line - GBL is pulled to ground (Fig.5(a) (b)). Additional decode signals are applied to T8 - T11 transistors in order to select one of the two neighbouring local bitlines for access and to clamp the other line at the fixed potential on Node 4 (Fig.4). The respective bitlines

are chosen by setting different signals to control transistors T8 - T11. When T8 and T11 turn ON via signals WA0 (high) and RL1 (low) while T9 and T10 are both kept OFF via their gate voltages WA1 (low) and RL0 (high) then BL0 is chosen. When T8 and T11 turn OFF via signals WA0 (low) and RL1 (high) while T9 and T10 are both kept ON via their gate voltages WA1 (high) and RL0 (low) then BL1 is chosen.

Cell write at the time of the value of BL0 and validate its Write Word Line (WWL = 1). Data is retained in the form of charge stored in capacitor C_{001} once at WWL = 0 Fig.5(c) (d). BL2.0 is recharged to Vdd and the read operation is confirmed by setting high level signal on Read Word Line RWL. To read the cell RWL must be equal to 1. T_{002} can be turned ON or OFF depending on the stored value. T_{002} and T_{003} BL2.0 are pulled low where X = 1, otherwise BL2.0 remains high (Fig.1).

On Fig.5(c) (d) are shown the output voltages at the BL0 (DRAM cell on Fig.1) and a comparison between the storage capacitor Cpoly and the high-k MOS capacitor is made. The capacitor playing the role of storage elements is characterized by very low capacity (30 - 100fF), which makes its measurement and must comply with the parasitic capacity buses, which is often bigger than the capacity of a storage capacitor.

Conclusion

Widely used SiO_2 for gates oxide film can no longer be used because they receive very large earth leakage currents. Starts the search and examination of other materials for gates oxides, which already belong to highdielectric materials (high-k). The past is in many materials such as Hf-based films are very widely studied in combination with Ta_2O_5 give very encouraging results. Created scheme to simulate the modes of reading and writing 3T DRAM cell.The scheme is designed with AMS 0.35 CMOS technology in Cadence. By replacing Si capacitor with the MOS capacitor from HfO_2- Ta_2O_5 film the cell consumes less power and take less area, in which the matrix effect will be increase total power and occupies an area of the DRAM memory.

Acknowledgement

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