Verilog-A Model of a High-k HfO_2-Ta_2O_5 Capacitor

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Abstract—**A circuit simulation model of a MOS capacitor using high-k HfO_2–Ta_2O_5 mixed layer structure is developed using Verilog-A hardware description language. Model equations are based on the BSIM3v3 model core. Capacitance-voltage (*C*–*V*) and current-voltage (*I*–*V*) characteristics are simulated in Spectre circuit simulator within Cadence CAD system and validated against measurements of stack structure.**

Index Terms—**Device modeling, compact models, circuit simulation, high-k gate dielectric, Verilog-A, Spectre.**

I. Introduction

Device modeling is a key milestone to efficiently achieving the analog design objectives. The demand for circuit simulation models is increasing due to two ongoing developments, namely, the technology scaling into nanoregime and system integration with many different functions on a single chip [1]. The scaling of classical bulk Si CMOS transistors approaches its physical limits. The SiO_2 gate dielectric thickness of a few atoms raises unwanted quantum mechanical effects such as electron tunneling and gate leakage currents that compromise the classic MOS transistor operation. A key challenge in order to maintain the historic Moore's law progress in microelectronic technologies [2] is the implementation of new materials with higher dielectric constant (high-k materials) to replace the conventional SiO_2. In addition to their physical thickness aspect the high-k gate dielectrics are also required for enabling high-performance and low-power CMOS applications in the 45 nm technology node and beyond [3]. The emerging nanoelectronic transistors will rely on non-silicon high-k materials with target effective oxide thickness (EOT) of less than 10 Å to advance beyond the sub-20 nm regime [2], [4].

Promising alternative high-k materials are the multicomponent gate dielectrics based on a variety of metal oxides. To date, Ta_2O_5 is one of the best high-k dielectric candidates for storage capacitors of nanoscale dynamic random access memories (DRAMs) while HfO_2 appears to be the respective candidate for nano-MOSFETs [4], [5], [6]. The electrical characteristics prove that the structure composed of HfO_2–Ta_2O_5 mixed layer on Si performs as a high-k layer in terms of permittivity, allowable level of leakage current, and appropriate oxide interface properties [7].

To assist in the technology development, the most important modeling issue is to ensure sufficient simulation accuracy and applicability for any technology. For achieving this task it is essential to maintain a physically correct modeling of the real technological origins of the effects that govern the new device structures.

Compact device models are usually coded in circuit simulators using general-purpose languages. Accordingly, they are targeted specifically to the interface and internal data structures of their host simulator, and hence are inherently non-portable. In this context modification and optimization of a given model becomes a time-consuming and error-prone task. An effective approach to overcome this gap between model development and its subsequent implementation in CAD tools is to formulate open source code models in analog hardware description languages (HDLs) such as Verilog-A/AMS or VHDL-AMS. In the recent years Verilog-A has become increasingly viewed as most promising candidate for compact modeling purposes [8].

A compact model for circuit simulation of the high-k MOS capacitor HfO_2–Ta_2O_5 mixed layer structure presented in [7] is developed in this paper. The model is coded in Verilog-A HDL based on the BSIM3v3 model equations. Capacitance–voltage (*C*–*V*) and current–voltage (*I*–*V*) characteristics are compared to the measurements to validate the model.

II. Device Fabrication and Characterization

MOS capacitor structures are fabricated on chemically cleaned p-type (100) 15 Xcm Si wafers used as substrates. The HfO_2 layer with two thicknesses of 5 and 7 nm is deposited by RF sputtering of Hf target in Ar + 10% O_2 atmosphere on top of RF sputtered Ta_2O_5 with the same thicknesses. The wafer temperature is maintained at 200 °C during the deposition of the two types of films; the working gas pressure is 0.33 Pa and RF power density is 3.6 W/cm^2; Ta and Hf targets both with a purity of 99.99 % are used. The total film thickness, *d* and the refractive index, *n* are measured by ellipsometry (k = 632.8 nm); the physical thickness of the stacked films is 10 and 15 nm. Relatively large layer thicknesses are intentionally used in order to minimize the very small thickness-related effects and to study the effect of layers intermixing itself. According to X-ray diffraction analysis both types of films the pure Ta_2O_5 and the HfO_2–Ta_2O_5 are amorphous [7].

The test structures for electrical measurements are MIS capacitors with a back side electrode of ~ 300 nm evaporated Al. The capacitors are electrically characterized by means of *C*–*V* (Fig. 1) and *I*–*V* (Fig. 2) curves. The effective dielectric

constant ε_{eff} of the films is determined from the capacitance C_0 at an accumulation using ellipsometrically measured values of d. The oxide charge Q_f is evaluated from the C–V curves. The I–V curves are recorded at both polarities with a voltage ramp rate of 0.1 V/s, using Keithley 236 source measurement unit. Temperature dependent (20 – 100 °C) I–V measurements are performed in order to obtain a deeper insight into the conduction mechanisms governing the current through the structures as well as the energy location of traps participating in these processes. All measurements are carried out in a dark chamber [7].

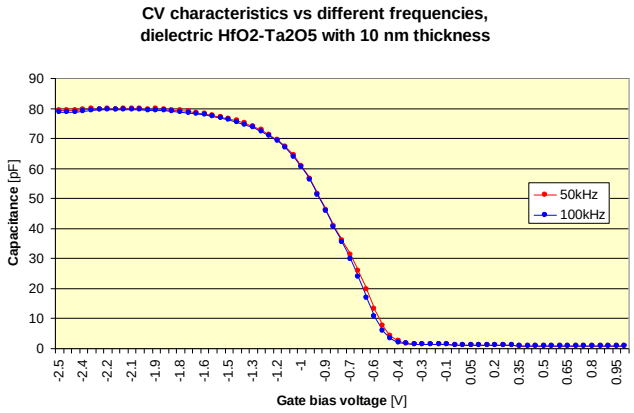

Figure 1. C–V characteristics measured by RLC meter versus two frequencies across 10 nm HfO_2-Ta_2O_5 capacitor stack.

The frequency range 50 kHz ÷ 100 kHz is selected in order to minimize the effects of the equivalent series-parallel circuit – at lower frequencies is increasing the role of the parallel shunting resistance while at higher frequencies the series substrate resistance is already an important factor [9].

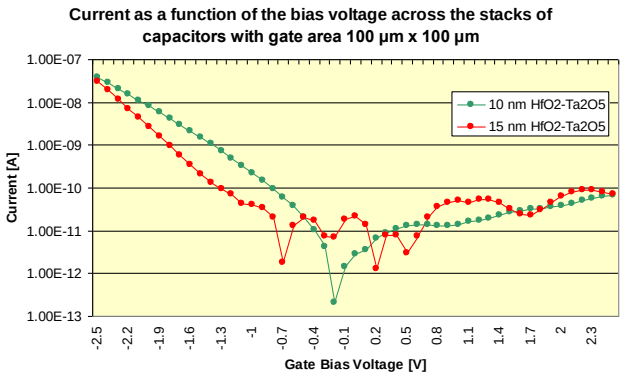

Figure 2. I-V characteristics measured with Keithley 236 across 10 nm and 15 nm HfO_2-Ta_2O_5 capacitor stacks.

III. Model Formulation

A. Modeling C–V Characteristics

Parameter extraction from the measurements. The designed model has typical capacitor input parameters – gate area, dielectric thickness, and substrate type of conductivity (P- or N-doped) which are further customized in the schematics. Other important parameters for the component performance are permittivity, substrate doping concentration, and flat band voltage. The effective permittivity is analyzed in [7] where it is extracted $\varepsilon_{eff} \approx 9$ from the 100 kHz C–V curve. The methodology, described in [10], provides an easy way for calculation of the doping concentration and the flat band voltage.

The substrate doping concentration (N_{sub}) is related to the slope of the $1/C^2$ curve versus the V_G bias voltage [10] which is shown on Fig. 3.

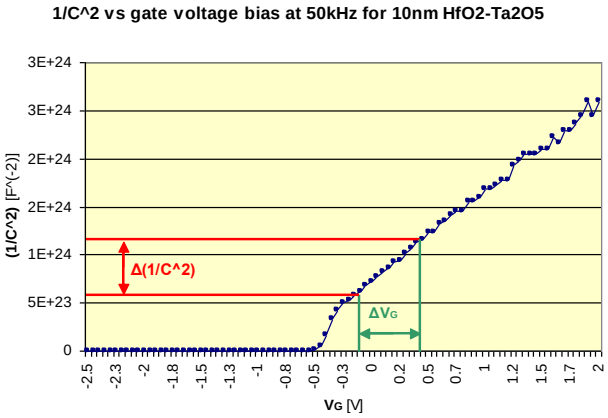

Figure 3. Curve of $1/C^2$ vs. V_G at 50 kHz. It is observed the typical increasing slope after the onset of depletion.

Therefore it can be directly extracted and calculated as follows [10]:

$$N_{SUB} = 2 \Big/ q\varepsilon_{Si} A^2 \left[\frac{\Delta\left(1/C^2\right)}{\Delta V_G} \right] \qquad (1)$$

where q – electron charge (1.60219×10^{-19} C), A – gate area (in cm^2), ε_{Si} – substrate permittivity (1.305×10^{-12} F/cm for Si).

Fig. 3 shows the roughly extraction of the slope after the onset of depletion based on which the substrate doping concentration was calculated on 1.25×10^{15} cm^{-3}.

The flat band voltage and the doping concentration profile were not directly extracted from the measurements due to the low accuracy of the method for bigger values of the interface trap density ($0.5\div1\times10^{12}$ $cm^{-2}eV^{-1}$ according to [7]). These parameters were fitted in the model according to the measurements.

B. Model creation

The modeled high-k dielectric structure is an upgrade to the state-of-the-art MOS technology for which the BSIM3v3 model provides one of the most advanced approximations to device physics. Therefore the equations for simulating C–V

characteristics can be based on the BSIM3v3 model which allows relatively easy applicability across different technologies. The existing MOSFET can be simulated as MOS capacitor if the source, bulk, and drain nodes are connected together as shown on the schematics of Fig. 4.

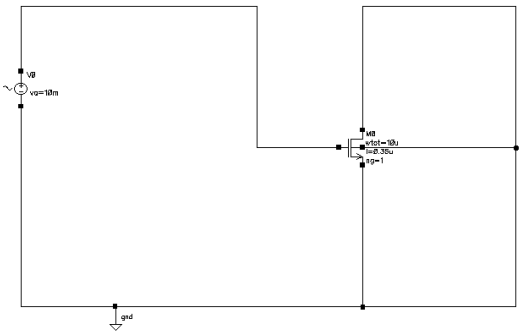

Figure 4. Bench circuit for simulation of *C-V* characteristics of capacitor-connected MOSFET.

In the schematics the MOS transistor is *N*-channel with default parameters for the S35D3 technology of the 0.35-μm CMOS design kit of AMS. V_0 is a sinusoidal voltage source with fixed amplitude of 10 mV and DC voltage sweep between –5 V ÷ +5 V. The *C–V* characteristics are simulated in AC mode by plotting the capacitance as a calculation based on the amplitude of the current through the gate node for a frequency of 50 kHz. The simulation of the *C–V* characteristics is shown on Fig. 5:

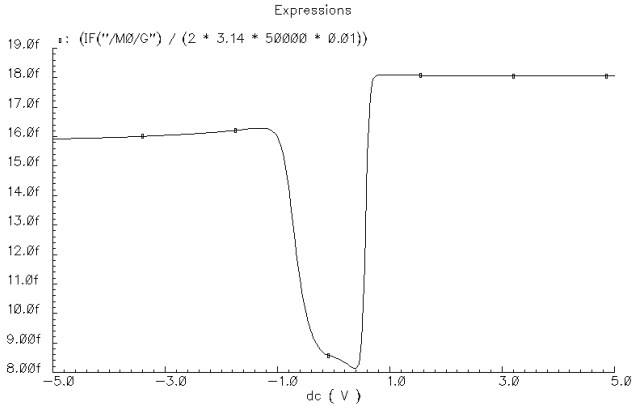

Figure 5. *C-V* characteristics simulated by the capacitor-connected MOSFET model. The onset of strong inversion is observed after the threshold voltage.

That graph shows onset of strong inversion after the threshold voltage because of the dominant impact of the doped source and drain regions. This is not the case with the analyzed HfO_2-Ta_2O_5 capacitor stacks because it has no drain and source. Therefore a modification of the BSIM3v3 equations is required. The portion of the Verilog-A code, which describes the intrinsic capacitance, was extracted, simplified, and embedded in a two-node component acting as a capacitor in the *C–V* simulation circuit.

The intrinsic capacitance equation is a sum of three charge types – the channel majority accumulation charge (Q_{ac0}), the channel minority inversion charge (Q_{inv}), and the substrate fixed charge (Q_{sub0}):

$$Q_{gate} = Q_{inv} + Q_{ac0} + Q_{sub,0} \tag{2}$$

The charge Q_{inv} can be omitted because it has dominant contribution after onset of inversion [11]. It describes the rapid exponential increase of minority carriers density which is dominating the slower increase of the depletion layer charge; this results in capacitance jump-up after the threshold voltage. The measurements (Fig. 1) show that the *C–V* slope is almost flat in strong inversion because the minority carriers contribute no capacitance and they screen further increase of the depletion width [10], [13].

The channel majority accumulation charge (Q_{ac0}) has dominant influence on the accumulation and depletion regions while in inversion the substrate fixed charge (Q_{sub0}) is with bigger impact. Therefore the model of *C–V* curve can be split into two parts — description of the accumulation and depletion regions by Q_{ac0} and description of the inversion region by Q_{sub0}.

The charge Q_{ac0} is given in [10] by the following formulas:

$$Q_{ac0} = WLC_{oxeff}(V_{FBeff} - V_{FB}) \tag{3}$$

where V_{FBeff} – effective flat-band voltage which smooth the transition between accumulation and depletion [11]. It is calculated by:

$$V_{FBeff} = \begin{cases} V_{FB} - 0.5(V_3 + \sqrt{V_3^2 + 4\delta_{3,1}V_{FB}} & if\ V_{FB} \geq 0 \\ V_{FB} - 0.5(V_3 + \sqrt{V_3^2 - 4\delta_{3,1}V_{FB}}) & if\ V_{FB} < 0 \end{cases} \tag{4}$$

$$V_3 = V_{FB} - V_{GS} - \delta_{3,2} \tag{5}$$

V_{GS} – bias voltage across the capacitor stack between the gate and substrate electrodes. $\delta_{3,1}$ and $\delta_{3,2}$ – constants with default value $\delta_{3,1}$ = $\delta_{3,2}$ = 0.02 V. These constants were separated in order to study separately their influence. C_{oxeff} – total capacitance per unit area [13] expressed as the series combination of the silicon capacitance per unit area $C_{cen} = \varepsilon_{Si} / T_{cen}$ and the oxide capacitance per unit area $C_{ox} = \varepsilon_{ox} / t_{ox}$:

$$C_{oxeff} = \frac{C_{ox}C_{cen}}{C_{ox} + C_{cen}} \tag{6}$$

where ε_{Si} and ε_{ox} – dielectric constants of the silicon and the dielectric layer, t_{ox} is the thickness of the dielectric layer. T_{cen} is calculated following the equations given in [12]. In T_{cen} expressions the parameter $A_{CDE,Nch}$ is an exponential

coefficient characterizing the charge width in accumulation and depletion [11]. It also depends on N_{ch} which is the doping concentration at the surface under the dielectric layer (the inversion channel for MOSFET):

$$A_{CDE,Nch} = A_{CDE} \times \left(\frac{N_{ch}}{2.10^{16}} \right)^{-0.25} \quad (7)$$

In BSIM3v3 the default of A_{CDE} is 1.

The substrate fixed charge (Q_{sub0}) is given in [12] by:

$$Q_{sub,0} = \begin{cases} WLC_{oxeff}\gamma_2 \left[\sqrt{\frac{K_1^2}{4} + Tmp} - \frac{K_1}{2} \right] & if\ Tmp \geq 0 \\ WLC_{oxeff}\gamma_2 \times Tmp & if\ Tmp < 0 \end{cases} \quad (8)$$

where:

$$Tmp = V_{GS} - V_{FBeff} - V_{gsteffcv} \quad (9)$$

$V_{gsteffCV}$ – effective voltage ($V_{GS} = V_{th}$) function introduced to describe the channel charge characteristics from sub-threshold to strong inversion [11] where the capacitance is increasing rapidly. That function can be omitted because the capacitance remains almost flat in strong inversion as observed from the *C–V* measurements γ_2 – body-effect in the bulk [12].

The initial model should be fitted in order to minimize the error with respect to the measurements. An accurate assessment of the fitting is given by calculating the integral error which is calculated as an average of the errors inside each interval.

Analyzing the formulas of the charges (Q_{ac0}) and (Q_{sub0}) we determined the following coefficients to be fitted:

- A_{CDE} – has an impact both in the accumulation and depletion regions.
- N_{ch} – has an impact both in the accumulation and depletion regions.
- $\delta_{3,1}$ – has a significant impact in the depletion region by changing the slope of the curve which is visible for $N_{ch} > 10^{16}$ cm^{-3}.
- V_{FB} and $\delta_{3,2}$ – these two parameters move equidistantly the curve across the *x*-axis (the applied bias voltage), therefore with biggest impact on the depletion region

The complexity of the equations and the shape of the *C–V* curve does not allow direct fitting of these parameters for the whole bias range. More flexible approach is to define values of the empirical coefficients ($\delta_{3,1}$ and $\delta_{3,2}$) for different bias voltage ranges.

The fitting started with finding the optimal value of the flat-band voltage which moved the *C–V* curve in the desired bias range. Then the surface doping concentration (N_{ch}) was fitted in accumulation in combination with the coefficient A_{CDE}. This allowed further fine fitting of the slope in depletion by changing only $\delta_{3,1}$ and $\delta_{3,2}$. The parameters for fitting in the corresponding regions of the *C–V* curve are illustrated on Fig. 6.

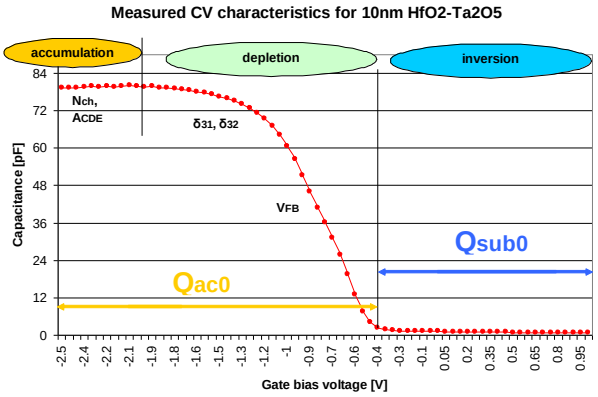

Figure 6. *C–V* characteristics split into regions for fitting. In each region the corresponding parameters for fitting are shown.

The outcomes from the first fitting iterations are the optimized values in Table I.

TABLE I. FITTED PARAMETER VALUES DESCRIBING THE *C-V* CHARACTERISTICS

Parameter	Value	Bias Voltage Range [V]
Flat-band voltage, V^*_{FB}	– 0.55 V	(–∞, +∞)
Surface doping concentration, N^*_{ch}	1.25×10^{18} cm^{-3}	(–∞, +∞)
$\delta_{3,1}$	0.02 V	< (V_{FB} – 1.2)
$\delta_{3,1}$	0.028 V ÷ 0.048 V	(V_{FB} – 1.2) ÷ (V_{FB} – 0.05)
$\delta_{3,1}$	0.038 V ÷ 0.016 V	(V_{FB} – 0.05) ÷ (V_{FB} – 0.11)
$\delta_{3,1}$	0.01 V	> (V_{FB} - 0.11)
$\delta_{3,2}$	0.02 V	< (V_{FB} – 1.45)
$\delta_{3,2}$	0.24 V	> (V_{FB} – 1.45)

* So defined V_{FB} and N_{ch} are technology constants related to flat-band voltage and surface doping concentration.

The *C–V* measurements fit very well with the simulation results of Q_{sub0} for bias voltage greater than –0.4 V. Therefore the expressions of the charge Q_{ac0} can be replaced with the expressions of Q_{sub0} for $V_{GS} \geq V_{FB} + 0.15$.

The integral error of the mismatch between the simulations and measurements curves was calculated to be err_{avg} = 3.35 %.

On Fig. 7 and Fig. 8 are shown the results from parametric analysis with the geometry parameters which validate the model flexibility.

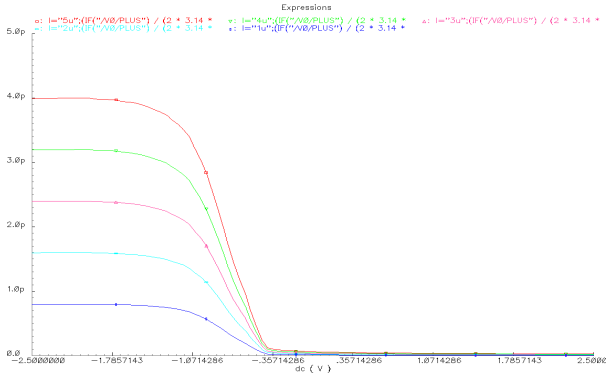

Figure 7. *C–V* simulations vs. different values of the gate length. The characteristics perfomance matches theoretical expectations.

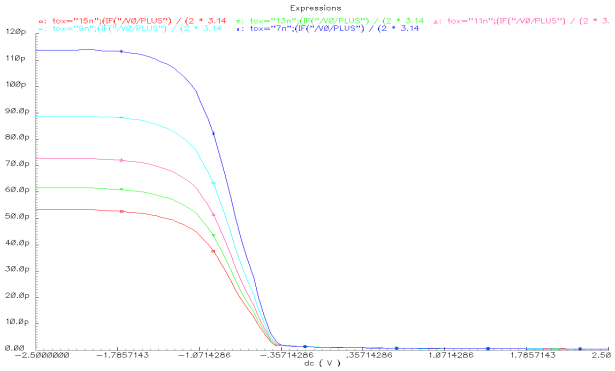

Figure 8. *C–V* simulations vs. different values of the dielectric thickness. The characteristics perfomance matches theoretical expectations.

C. *Modeling I–V Characteristics*

The *I–V* characteristics can be also split into two regions described with separate equations for the current density *J*:

- Accumulation and depletion region for $V_{GS} \le V_{FB} + 0.25$ where the current density follows exponential dependence on the applied bias voltage:

$$J(V_{GS}) = a_1 e^{-b_1 V_{GS}} \tag{10}$$

- Inversion region for $V_{GS} > V_{FB} + 0.15$ where the current density follows linear dependence on the bias voltage:

$$J(V_{GS}) = a_2 + b_2 V_{GS} \tag{11}$$

The fitting was based on the measurement results from both the 10 nm and 15 nm capacitor stacks (Fig. 2). Lower currents are observed with thicker dielectric layers in accumulation and depletion regions. Hence, different values for a_1 and b_1 are needed. At the same time no significant thickness dependence exists in the inversion region where the current seems to be more fluctuating due to the unstable conditions for forming the inversion layer. Therefore the characteristics can be approximated with same linear equation. On Fig. 9 are displayed the approximations for the capacitor stacks with both thicknesses.

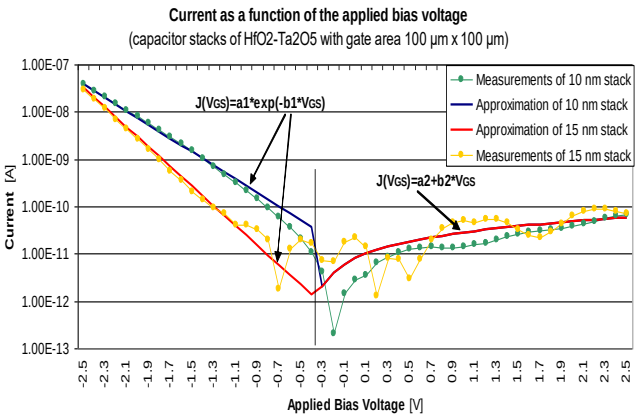

Figure 9. *I–V* measurements vs. the proposed approximations for 10 nm and 15 nm capacitor stacks from HfO_2-Ta_2O_5 (*y*-axis is in logarithmic scale).

TABLE II. COEFFICIENTS FOR *I-V* APPROXIMATION

Coefficient	10 nm thickness	15 nm thickness
a_1	1.0×10^{-11}	2.0×10^{-13}
b_1	3.3	4.8
a_2	8.0×10^{-12}	
b_2	2.0×10^{-11}	

The thickness dependence will be modeled even more accurately after gathering more characterization data. The current model was created to generate only two *I–V* curves:

- For thickness less than 12.5 nm using the values from the second column of Table II.
- For thicknesses greater than 12.5 nm using the values from the third column of Table II.

The leakage current model was simulated using similar test bench like for the *C–V* simulation (Fig. 4). The corresponding voltage source, type of analysis and current selected for plotting were replaced from AC to DC. Afterwards the *I–V* model was validated by parametric analysis versus thickness (Fig. 10). The average integral error of the mismatch between the simulations and measurements is err_{avg} = 8.83 %.

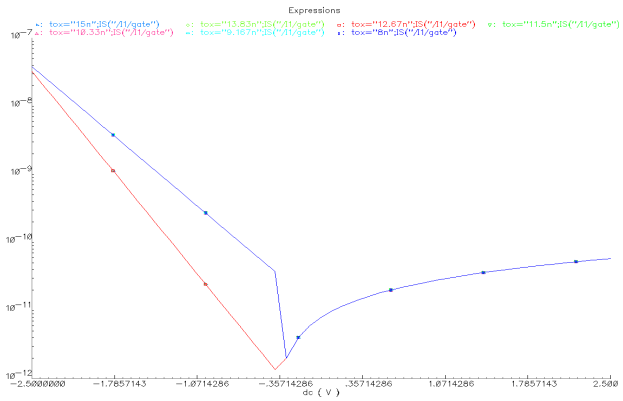

Figure 10. *I–V* simulation vs. different dielectric thicknesses (the *y*-axis is in logarithmic scale). The curves is according to the characterization results.

IV. VERILOG-A CODE

Below we provide an excerpt of the Verilog-A code of the model we developed.

```
// Calculation of the charge in accumulation //
Tox  = 1.0e8 * tox;
T0   = (Vgs - vfb) / Tox;   tmp = T0 * acde;
Tcen = ldeb * exp(tmp);    LINK = 1.0e-3*tox;
V3   = ldeb - Tcen - LINK;
V4   = exp(0.5*ln(V3*V3 + 4.0 * LINK * ldeb));
Tcen = ldeb - 0.5 * (V3 + V4);
Ccen = `EpsSi / Tcen;
T2   = Cox / (Cox + Ccen);
Coxeff   = T2 * Ccen;
CoxWLcen = CoxWL * Coxeff / Cox;
Qac0 = CoxWLcen * (Vfbeff - vfb);

// Calculation of the charge in depletion //
T0   = 0.5 * k1;//ok119
T3   = Vgs - Vfbeff;
if (T3 < 0.0)
       begin
            T1 = T0 + T3 / k1;
       end
  else
       begin
            T1 = exp(0.5*ln(T0 * T0 + T3));
       end

Qsub0 = CoxWLcen * k1 * (T1 - T0);


//  The following statements replace Qac0 with
    Qsub0 for the depletion region //
if((vfb-vgs)<=-0.15)
     qgate = Qsub0;
  else
     qgate=Qac0;


// Expressing the current as first derivative of
   the charge //
     Qgate = qgate;
     cqgate = TYPE * ddt(Qgate);
     I(gate, bulk)    <+ cqgate;

     // IV model //
     if (tox < 12.5e-9)
       begin
         a1 = `A1;
         b1 = `B1;
       end
     else
       begin
         a1 = `A2;
         b1 = `B2;
       end

     if((vfb-Vgs)>=-0.25)
     igate = a1*exp(-b1*Vgs)*w*l/(100e-6*100e-6);
     if ((vfb-Vgs)<-0.25)
     igate = (`a2 + `b2*Vgs)*w*l/(100e-6*100e-6);
     I(gate, bulk) <+ igate;
```

V. CONCLUSION

A Verilog-A formulation of circuit simulation model for a MOS capacitor using high-k HfO_2–Ta_2O_5 mixed layer structure was developed. The model proceeds from BSIM3v3 model equation core to simulate *C–V* and *I–V* characteristics of the modeled structure. The simulation results were validated against the measurements published in [7].

The simulations were performed in Spectre circuit simulator within Cadence CAD environment. They demonstrated very good agreement to the measurements – 3.35 % accuracy for *C–V* measurements and 8.83 % for *I–V* measurements.

On the other hand, the model realization represents a straightforward example of an all-purpose methodology for coding compact model equations in a portable, open-source environment applicable to various simulation platforms.

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