

# Studying Digitally Controlled Oscillator Circuits for Digital Phase Synchronizers

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**Abstract** – The Voltage Controlled Oscillator is replaced by Digitally Controlled Oscillator in the digital Phase Locked Loop systems. The Digitally Controlled Oscillator has several differences and limitations which require further study in order to compare the different circuit variations and to choose the most appropriate circuit for the application. The frequency range, frequency step and the frequency change delay are examined in this paper. The results from the testing of the different circuit variations are compared and represented in graphical form. The useful range of working frequencies is discussed.

**Keywords** – DCO; Digitally Controlled Oscillator; FPGA; Phase Synchronizer; Programmable Logic.

## I. INTRODUCTION

The completely digital Phase Locked Loops (PLL) are widely used in the modern electronics. They are preferred due to the lower cost of the components, easier scalability and the possibility for complete integration [1]. They offer more flexibility in a wide range of frequencies with the possibility for dynamic adaptation of the circuit. This leads to faster synchronization which makes it suitable for systems with frequent on/off cycles and frequency changes [1]. The development of a completely digital PLL requires the replacement of all analog circuits with their digital equivalents. In some cases, the digital replacement circuits have some differences and limitations compared to the traditional analog circuits. These limitations require more precise study of the parameters of the different circuits. After the comparison of the parameters, the decision could be taken which is the most appropriate circuit for the application. One of the most important circuit in the analog PLL is the Voltage Controlled Oscillator (VCO). In the digital PLL the VCO is replaced with Digitally Controlled Oscillator (DCO). The DCO has some different properties and limitations compared to the VCO [2]. The most important limitations are the discrete frequency step and the inability to generate frequency higher than the input clock frequency [2]. The discrete frequency step leads to phase uncertainty of the digital PLL and higher phase noise. Due to this the frequency step of the DCO should be chosen carefully. In most of the cases the DCO is designed as a programmable frequency divider. Its period step is fixed over the whole frequency range, but the frequency step is dependent on the division coefficient and is getting higher with lower division coefficients [3]. This is limiting the usable output frequency range of the DCO. Several different DCO architectures will be examined and

compared in this paper in order to choose the most appropriate circuit for the exact application.

All the circuits are developed and tested on a Field Programmable Gate Array (FPGA) integrated circuit by Xilinx.

## II. STRUCTURE OF THE TEST SETUP

The structure of the experimental setup is represented on fig. 1.

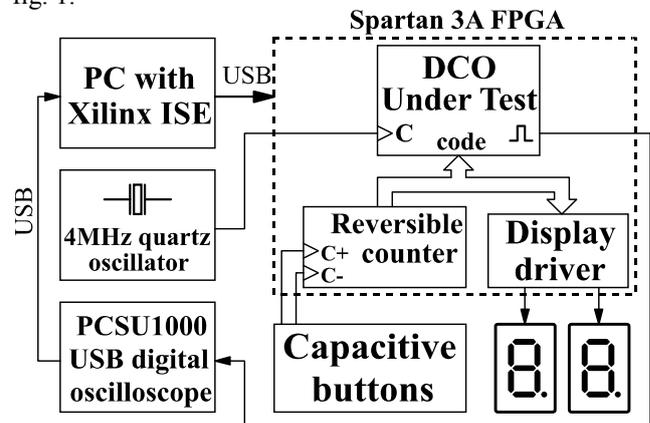


Fig. 1. DCO test setup

The circuits of the DCO under test are implemented on a Spartan 3A FPGA. The input code for the DCO is generated by reversible binary counter controlled by two capacitive buttons. The code is also applied to a display driver and is represented on a 7-segment display. A 4 MHz quartz oscillator is used for input clock signal generation. The output pulses from the DCO are viewed with a 2 channel 60 MHz USB oscilloscope PCSU 1000 by Velleman. It is also possible to implement a ratio counter into the FPGA to represent the division coefficient of the DCO on the display. The data from the testing of each DCO is collected and the code-to-frequency relation along with the frequency step is calculated and represented in graphic form. The programming of the FPGA is done through USB interface using PC with installed Xilinx ISE Project Navigator software [4].

## III. DCO CIRCUITS EXAMINATION

The most frequently used DCO consists of a fixed frequency clock generator followed by a programmable frequency divider [5]. This type of DCO is easiest for complete integration [6]. Its main limitation is that it cannot generate output frequency higher than the input clock

frequency. Due to that it cannot be used in frequency multiplying systems. There are several different circuit variations which has different frequency step, different code-to-frequency relation and a different delay between code and frequency change. For the different applications different circuits are more appropriate.

The first examined circuit is programmable frequency divider based on presettable reversible counter configured in down mode [4]. Its logical diagram is represented on fig. 2.

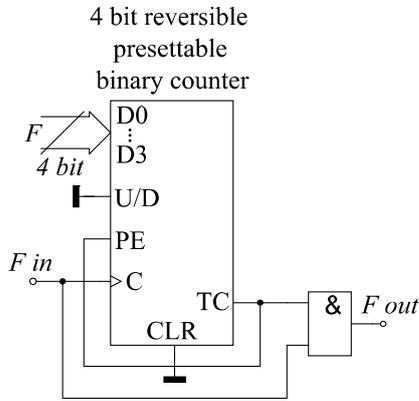


Fig. 2. First examined DCO – logic diagram

At the beginning the counter is in zero state and the  $TC$  output is in logical 1 as the counter is configured in down mode. This high level is fed to the  $PE$  input of the counter. On the next rising edge of the  $Fin$  signal, the control code  $F$  is loaded into the counter [4]. It starts counting down from the loaded number until it reaches zero again. Every time the counter reaches zero, the logic  $AND$  outputs one of the input pulses. The division coefficient equals  $1+F$ . The output frequency is given by equation (1):

$$F_{out} = \frac{F_{in}}{1+F} \quad (1)$$

The duty cycle of the output pulses is dependent on the number  $F$  and the duty cycle of the input pulses – equation (2):

$$D_{out} = \frac{D_{in}}{1+F} \quad (2)$$

Where:

$D_{out}$  is the duty cycle of the output pulses;

$D_{in}$  is the duty cycle of the input pulses;

$F$  is the control code.

The main disadvantage of this programmable frequency divider is that it loads the number  $F$  only when the counter reaches zero. Changing the code during the cycle will take effect at the end of the cycle. The delay between the code change and the output frequency change is less or equal to  $(1+F)T_{in}$ . This delay can be critical in some digital PLL circuits.

The last clock pulse of each period, when the counter reaches zero, passes through the  $AND$  gate. The rising edge of the next clock pulse which loads the counter with the number  $F$  also passes through the gate. For that reason, the  $F_{out}$  signal should not be used for clock inputs. It can be used for clock enable inputs. The output signal can be taken directly from the  $TC$  output of the counter where it does not contain glitches. The only difference will be, that with control code  $F$  less than 1, the output will be

constantly in logic 1 condition. The useful division coefficient will be equal or greater than two. The timing diagrams of the circuit are represented in fig. 3.

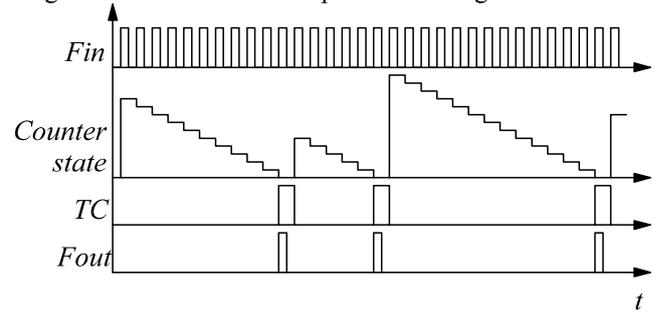


Fig. 3. First examined DCO – timing diagrams

It can be clearly seen that the input code  $F$  is taken only at the end of each period.

The code-to-frequency response of the examined DCO is represented in fig. 4.

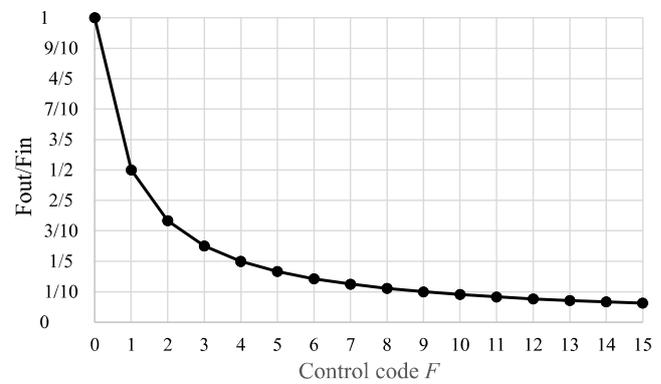


Fig. 4. Code-to-frequency response of the DCO

It can be seen that the code-to-frequency relation is not linear. It is obvious that when the division coefficient is lower than 5 the frequency step becomes too big. This property limits the usable frequency range of every DCO of this type [7].

In some PLL systems the delay between the code and frequency change is critical for the stability [8]. In these cases, the use of this DCO is not effective. For that reason, an enhanced circuit is developed, in which the delay between the code and frequency change is greatly reduced [9]. The circuit consists of binary counter with synchronous reset input  $SR$  and magnitude comparator. The logical diagram is represented in fig. 5.

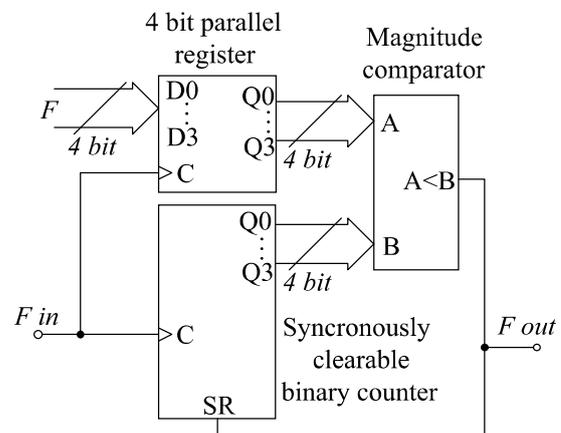


Fig. 5. Second examined DCO – logic diagram

The output of the binary counter is compared with the control code  $F$ . If the state of the counter is higher than  $F$ , the output  $A < B$  of the magnitude comparator outputs high level. This high level is fed to the synchronous reset input of the counter. The next rising edge of the  $Fin$  signal resets the counter and the process repeats. The counter always counts from zero to the number  $F+1$ . The number  $F$  is fed to the magnitude comparator through 4-bit parallel register in order to synchronize the code change with the  $Fin$  signal. The division coefficient of the circuit equals  $2+F$ . The output frequency is given by equation (3):

$$F_{out} = \frac{Fin}{2 + F} \quad (3)$$

The duty cycle of the output pulses depends on the division coefficient – equation (4):

$$D = \frac{1}{2 + F} \quad (4)$$

The delay between the change of the code and the frequency is given by equation (5):

$$T_d \leq T_{in} + \frac{T_{in}(2+F)}{2} \quad (5)$$

When the number  $F$  is changed after one period of  $Fin$  it is stored into the parallel register and compared to the current state of the counter. If the number is lower than the counter state, the reset input of the counter is activated, and the counter is cleared on the next rising edge of  $Fin$  [4]. The delay is always smaller or equal to one period of the  $Fin$  signal and half period of the new frequency [9]. The timing diagrams of the examined DCO are represented in fig. 6.

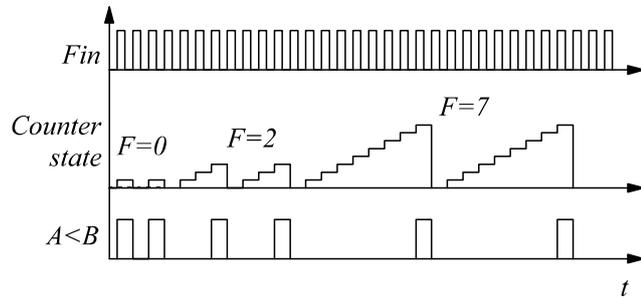


Fig. 6. Timing diagrams of the examined DCO

The pulse width of the output signal always equals one period of the input signal. The code-to-frequency relation of the examined DCO is the same as the one represented on fig. 4, with the difference that here the division coefficient has its minimal value of two and maximal value of 16. The input control code should never exceed 14 as if it reaches 15 the output of the counter will never become larger and there will be no output signal. This situation can be partially avoided if the output signal is taken with  $OR$  logic gate from the  $TC$  output of the counter and the  $A < B$  output. Although the division coefficient will have the same value for control code 14 and 15.

#### A. DCO with signed input code

In some cases, it is useful to have DCO running like ordinary VCO with bipolar input range and a free running frequency when the input code is zero [2]. To achieve this a

combinational circuit is designed based on the following logic equations (6):

$$\begin{aligned} Y0 &= A0 \oplus A3 \\ Y1 &= A1 \oplus A3 \\ Y2 &= A1 \oplus A3 \\ Y3 &= \overline{A3} \end{aligned} \quad (6)$$

The logical diagram is represented on fig. 7.

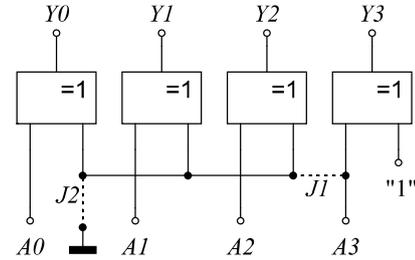


Fig. 7. Signed to unsigned binary – logic diagram

The circuit converts the input number from signed binary to unsigned binary format where the zero is in the middle of the range. The circuit has two different configurations – for numbers in signed binary format when  $J1$  is closed and  $J2$  is open. For 2's complement format when  $J2$  is closed and  $J1$  is open.

#### B. Multiplying the input frequency

In some digital PLL systems it is beneficial to have some algorithm for fine phase correction [2, 10]. Instead of just dividing the frequency it is possible to insert additional pulses. This method offers a precise control of the phase difference and can be used along with the traditional DCO designs examined in this paper. The logic diagram of a controllable rising edge injector is represented on fig. 8.

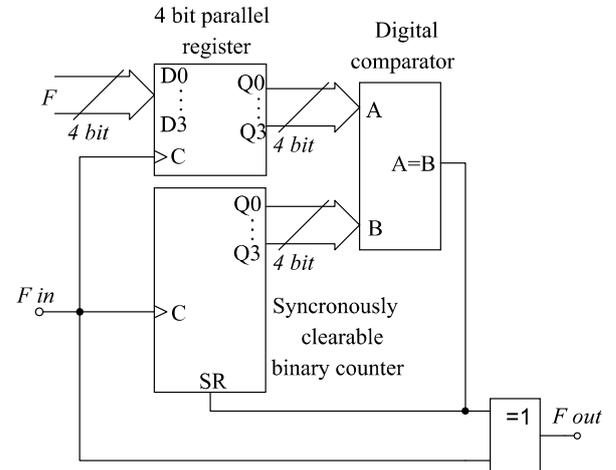


Fig. 8. Controllable rising edge injector – logic diagram

The circuit consists of a synchronously clearable binary counter, a digital comparator and an  $XOR$  logic gate. The number  $F$  is controlling the number of  $Fin$  periods between the rising edge injections. When the state of the counter becomes equal to the number  $F$ , the comparator generates a high level. It is fed to the  $XOR$  gate and to the reset input of the counter. After a short delay the output of the  $XOR$  gate switches in low state until the falling edge of the  $Fin$  signal. This falling edge is converted to an additional rising edge at the output of the circuit. The next rising edge of the  $Fin$

signal resets the counter and appears at the output of the circuit as a fast combination of falling and rising edge as synchronously with the reset of the counter, the  $A=B$  output of the comparator switches in low state and the  $XOR$  gate starts to transmit the input signal unchanged. The timing diagrams of the circuit are represented on fig. 9.

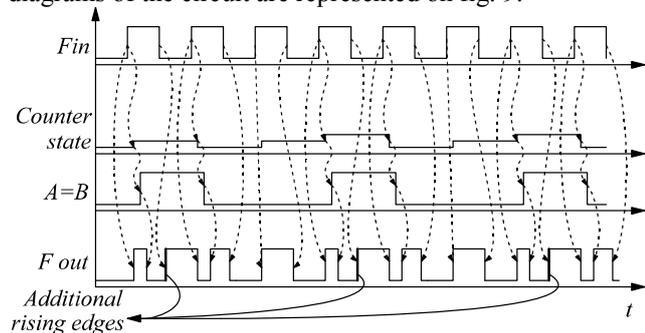


Fig. 9. Controllable rising edge injector – timing diagrams

It can be seen from the picture that every time when the counter reaches the number  $F$ , one additional rising edge is inserted into the input pulse train. This way we can precisely control the number of injected edges for a period of time. When the number  $F$  is 0 the input signal is transmitted in inverted form without edge insertion. When the number  $F$  is 1, on every second rising edge one additional rising edge is inserted. As the number  $F$  becomes higher, the number of injected rising edges becomes lower. The relation between the input and output frequency based on the number  $F$  is represented in equation (7) and fig. 10.

$$\frac{F_{out}}{F_{in}} = \frac{F + 2}{F + 1} \quad (7)$$

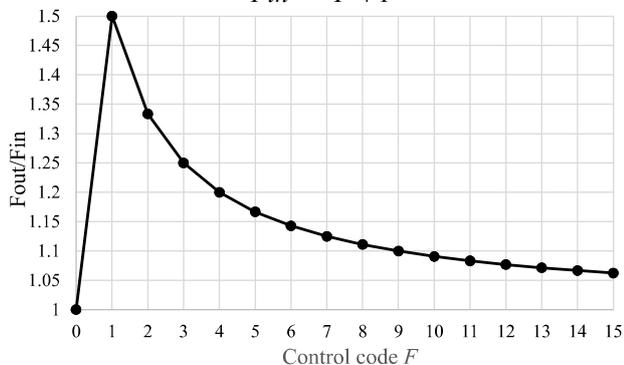


Fig. 10. Rising edge injector – code-to-frequency relation

It is clearly seen that the coefficient of frequency multiplication lies in the range from 1.5 to about 1.06 for 4-bit circuit.

#### IV. FPGA IMPLEMENTATION

All the examined circuits are completely tested on the FPGA device. The circuits are drawn as logical diagrams in the Xilinx ISE project navigator. All of the used logic blocks are from the Spartan 3A library. The circuits are compiled to *.bit* files and loaded into the FPGA using the *AV Prog* utility and the embedded JTAG controller.

All the examined circuits are 4-bit for the simplicity of testing. In the real applications their resolution can be higher, keeping all the examined properties and relations.

#### V. CONCLUSION

A test setup for studying different DCO characteristics is developed based on a FPGA integrated circuit. The use of programmable logic device gives the convenience of fast reconfiguration for the different examined circuits.

The classical DCO circuits based on fixed frequency generator and programmable frequency divider are giving reliable results when the division coefficient is high enough to give reasonably small frequency step for the application.

One of the drawbacks of the standard frequency divider circuit is the delay between the code change and the division coefficient change. A circuit modification is proposed and tested which reduces this delay significantly. Its positive effect on the stability of a digital PLL is examined.

A digital circuit for injection of additional rising edges in the input clock signal is proposed and tested. The circuit gives good results for fine phase tuning in the digital PLL system. Its use is practical with high frequency division coefficient after it. This way the introduced phase noise will be small enough to be neglected. The circuit gives good results when connected between the high frequency fixed generator and the programmable frequency divider. This way it gives additional fine-tuning mechanism.

#### ACKNOWLEDGMENT

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