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BOOK 2

DC – DC Converter Integrated on CMOS 0.35 μm Technology

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Abstract – **DC – DC converter is designed and integrated on CMOS 0.35 μm technology. Investigations results of efficiency and power losses are presented. Different control techniques of monolithic buck converter system are developed.**

Keywords – **dc – dc converter, CMOS technology, efficiency, power losses**

I. Introduction

In the modern electronic equipments different power supply voltages for the building blocks are needed. DC – DC converters with high efficiency are required to be designed [1]. A way to decreasing the size, weight and consequently the price of these devices is miniaturizations. The integration is the present and future of the electronic technique for many applications. Fully monolithic dc – dc converter could reduce the volume of the devices. The tendency in microelectronics nowadays is to continuously scale down the standard CMOS process technology, which leads to decreased breakdown voltages. In battery-powered electronic devices, however, the battery voltage remain relatively constant and it should be converted to the desired voltage levels with minimum energy loss. The requirement to increase the battery life and the system run-time of these devices becomes stringent. To reduce the power dissipations is necessary subsystems to operate at its optimum supply voltages.

A high switching frequency is the key design parameter, which help to make monolithic integration of active and passive devices. At this high switching frequency, the energy dissipated in power MOS transistors dominates the total losses in dc-dc converter. To receive the best possible efficiency we need to operate exactly at the frequency, where the inductor of low–pass filter has maximum quality factor Q. In CMOS technology, passive components and especially integrated inductor are very lossy. The passive components are for energy storage and output filtering.

The custom designed monolithic voltage converters for individual loads have high efficiency and their volumes are small. The standard PWM control, which is constant frequency method, is widely used to maintain a fixed voltage to output of the converter. When the converter operates with high load, the circuit work in the basic mode and high efficiency could be achieved. In most of the portable electronic devices, a light-load operation or standby mode is a key to achieve longer battery life, and at this mode the system should also indicate high efficiency.

This paper presents dc – dc monolithic buck converter designed on 0.35-μm CMOS technology. Section II is divided into three parts. In Section II *A* efficiency investigations results as function of different circuit's parameters are given. Power losses evaluations are presented Section II *B*. In Section II *C* developed PWM and PFM controls of the designed buck converter are described.

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II. Investigations

A. Efficiency investigations

Figure 1 shows the circuit of a buck converter implemented on standard CMOS 0.35-μm technology. The NMOS and PMOS transistors, which are forming the power stage, are synchronously controlled in a way that when one of the transistors is switched-on the other is switched-off. In the following, the efficiency performance of the power stage is evaluated assuming ideal drivers with the goal to select an appropriate switching frequency and filtering components.

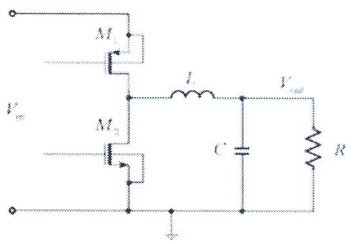

Figure 1. Synchronous buck converter schematic.

One of the most important parameters in the dc-converters is efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} \qquad (1)$$

where P_{OUT} is the average output power, P_{IN} is the average input power of the converter. The losses in power stage of buck converter are much higher compare to the energy dissipation in the feedback control system [2]. They dominate and determine the efficiency of the system.

The power losses in the filter inductor can seriously decrease the overall efficiency of the converter's system. Integration of whole dc – dc converter together with passive filter's inductor and capacitor is possible at high switching frequency f_s. On the other hand this leads to increasing of power losses in CMOS integrated circuits. The disadvantages of monolithic inductors are that they are usually with low inductance, occupied large silicon area and have low quality factor Q.

The influence of the filter's inductor value L over the efficiency of the synchronous buck converter is investigated. The received results are achieved by simulations using Cadence design tools. In Figure 2 is presented efficiency η of the evaluated circuit as a function L at different load currents.

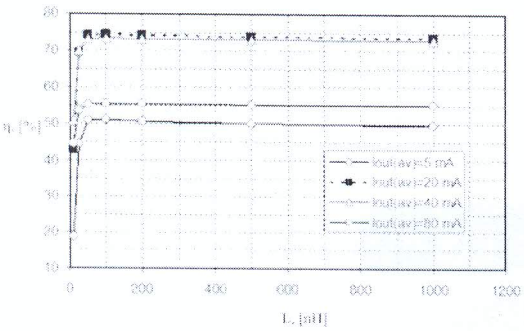

Figure 2. Efficiency of the designed monolithic buck converter as a function of filter inductor L at different load currents $I_{out(av)}$.

As can be seen from the picture at small inductor's values η of the investigated circuit is decreasing dramatically. The best efficiency results are achieved at load current equal to 20 mA, because for that current are optimized the sizes of N and P channel power MOS transistors.

The price and volume of electronic equipments is one of the major factors in their design. There are restrictions on the value and the chip area, which can occupy integrated filter capacitor in monolithic buck converter [3]. The effect of the maximum allowable output voltage ripple over efficiency performance of the converter is investigated. The influence of the capacitor value over the system efficiency is evaluated. The output voltage ripple is kept constant at three different levels respectively 10 mV, 20 mV и 50 mV. The investigations are made are average load current equal to $I_{out(av)}$ 20 mA.

In Figure 3 are presented received simulations results of the buck converter's efficiency η as function of filter capacitor C.

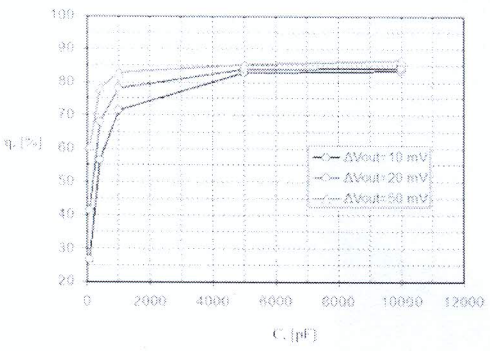

Figure 3. Efficiency of the designed monolithic buck converter as a function of filter capacitor C at different maximum allowable output voltage ripple ΔV_{out}.

In Figure 4 is presented relationship between switching frequency f_s and output filter capacitor C of the synchronous buck converter, when output voltage ripple is kept constant. As can be seen from the picture, higher ΔV_{out} leads to decreasing of f_s in order to maintain a constant value of output voltage and inductor current ripple ΔI_L at fixed value of. At lower switching frequency losses in the power MOS transistors goes down. Thereby reducing the requirements to output voltage ripple ΔV_{out} is increasing the efficiency of monolithic buck converter at fixed filter capacitor C.

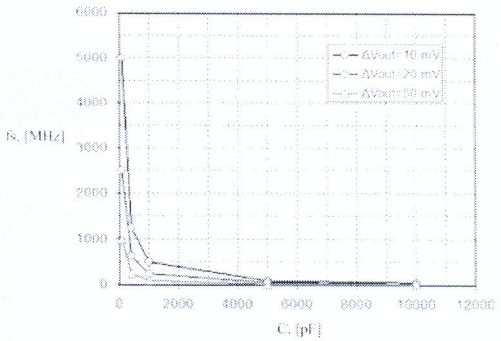

Figure 4. Switching frequency f_s of the designed monolithic buck converter as a function of filter capacitor C at different maximum allowable output voltage ripple ΔV_{out}.

Decreasing the switching frequency f_s is increased the reliability of the whole integrated buck dc-dc converter system, because the design of PWM control technique became simple.

B. Power losses investigations

At high switching frequencies the losses in the transistors are inadmissibly large and the efficiency of the converter decreases:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \qquad (2)$$

where P_{LOSS} are all power losses occurring in the power transistors, as well as in the controlling stages. To obtain high converter efficiency, all conversion losses should be kept to a minimum. The conducting losses in the transistors are proportional to the switching frequency f_s and the rms-value of the current flowing through the device 0. This relationship is repeated bellow:

$$P_{MOS} = k_1 i_{rms}^2 + k_2 f_s \qquad (3)$$

where $k1$ and $k2$ is are technology dependent coefficient, which are taking into account the size of the power MOS, as well as the resistive and the capacitive losses associated with the MOS structure. Small inductor ripple current will result in smaller rms-value of the current through the MOS structure, and it will respectively lead to better efficiency.

Power losses in filter inductor of designed monolithic dc-dc converter are evaluated.

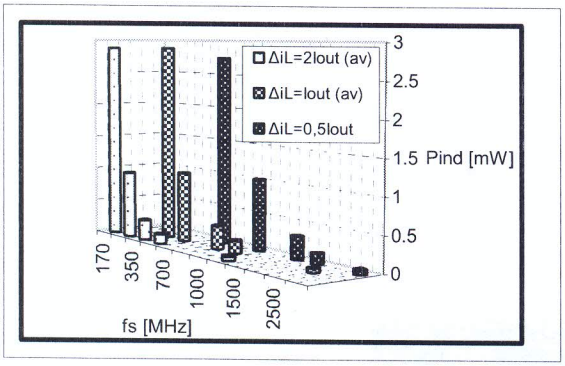

Figure 5. Power losses in the filter inductor of buck converter of fs and ΔI_L, for $Iout\ (av)$=20 mA.

In Figure 5 are presented received simulations results. Power losses in the filter inductor are investigated as a function of switching frequency f_s and inductor current ripple ΔI_L at $I_{out(av)}$ =20 mA. The received results show that by increasing of switching frequency f_s of the circuit power dissipations in the filter inductor decreased. By increasing of the ΔI_L requirements for the inductor's value decreased for fixed switching frequency f_s. This reduces the parasitic impedance of the filter inductor and the related power loss. A higher value of the ΔI_L leads to the increasing of rms current through the inductor which causes to the bigger conduction losses in the inductor.

C. PWM and PFM controls

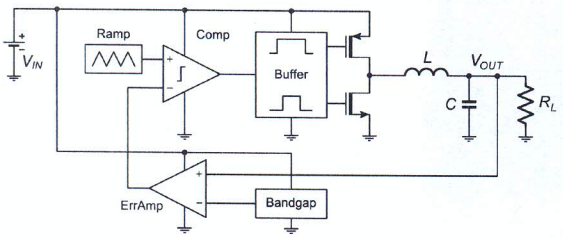

Figure 6. PWM block diagram

The block diagram of the switching-mode DC-DC buck converter system using standard PWM control loop is shown in Figure 6. The system consists of bandgap reference, error amplifier, ramp generator, comparator, buffer and power buck stage. The power losses in the controlling stages are minimized in order to improve the overall converter efficiency η. The nominal supply voltage of the converter is 3.6 V and steps-down to 1.2. The system operates at switching frequency f_s of 150 MHz.

The bandgap voltage reference provides a stable voltage for the whole converter system that is independent from the power supply, load current, and temperature variations. This stage consumes only 0.27 mA, which helps to improve η.

The error amplifier determines the control voltage, which amplifies the difference between the output voltage V_{out} and the reference voltage V_{ref}. The ramp generator is a part of the regulation system, which performs the Pulse-Width Modulation (PWM) control. This stage determines the switching frequency f_s of the buck converter. In Figure 7 is shown designed circuit of ramp generator.

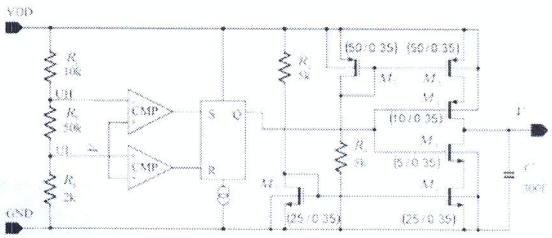

Figure 7. Ramp Generator.

This circuit helps to whole designed buck converter system to react when input voltage is changed. When V_{in} jumps the threshold voltages of two comparators, which are included in the ramp generator, are changed. The reason is simple resistive divider consist of R_1, R_3 and R_5. Therefore duty cycle of the control circuit is changed eliminating delay of the output reaction of the buck dc-dc converter system.

In Figure 8 are presented reactions of synchronous dc-dc buck converter system respectively with ramp generator including resistive divider and with ramp generator without resistive divider, when input voltage V_{in} jumps.

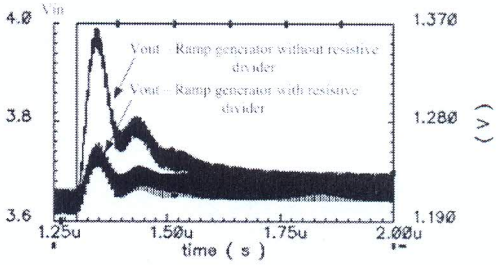

Figure 8. Reactions of synchronous dc-dc buck converter system respectively with ramp generator including resistive divider and with ramp generator without resistive divider, when input voltage V_{in} jumps.

The control pulses for the power transistors are generated by comparing the sawtooth signal generated by the ramp generator and the control signal from the error amplifier. The comparator generates rectangular pulses whose duty-cycle is a function of the output voltage, and the PWM control loop regulates the output to the desired value.

The buffer stage delivers the controlling pulses for the power transistors. The short-circuit losses are prevented by providing a short gap time during which the NMOS and the PMOS transistors are both switched-off 0. Thus, power losses generated due to this phenomenon are avoided.

In Figure 9 is presented efficiency of the designed buck dc-dc converter as function of average load current $I_{out(av)}$.

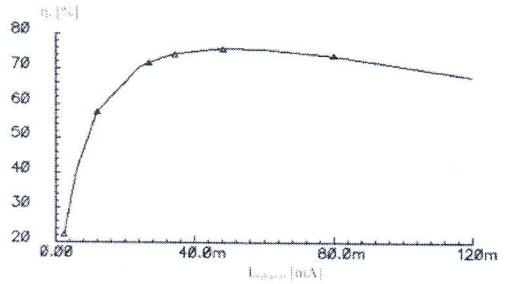

Figure 9. Efficiency of the designed buck dc-dc converter as function of average load current $I_{out(av)}$.

As can be seen from the picture efficiency of the buck dc-dc converter system is decreasing dramatically at light-load. PFM control technique is developed to improve the performance of the designed system at these conditions.

In Figure 10 are illustrated output voltages V_{out} of the converter respectively before and after layout design of the integrated circuit, when PWM control technique is used.

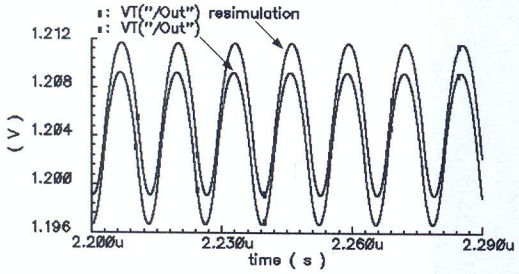

Figure 10. Output voltage V_{out} respectively before and after layout design when PWM control technique is used.

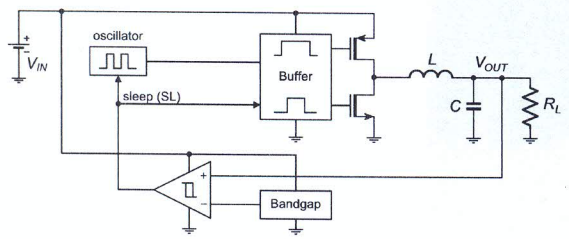

Figure 11. PFM block diagram

The block diagram of the converter utilizing a PFM control technique is shown in Figure 11. Here, a generator with a fixed duty-cycle (50%) is used to drive the power transistors. The voltage regulation is achieved by turning on and off the control loop. When the output voltage exceeds a predefined value, the comparator generates a control signal, which puts the whole system in sleep mode. In sleep mode, the filtering capacitor C delivers power to load, while all active blocks are disabled, except the comparator and the bandgap. When the output voltage goes below certain value, the comparator wakes up the system and the normal operation is restored. This technique allows minimization of the static control block consumption in light-load conditions, thus the overall efficiency is improved.

In Figure 12 are illustrated output voltages V_{out} of the converter respectively before and after layout design of the integrated circuit, when PFM control technique is used.

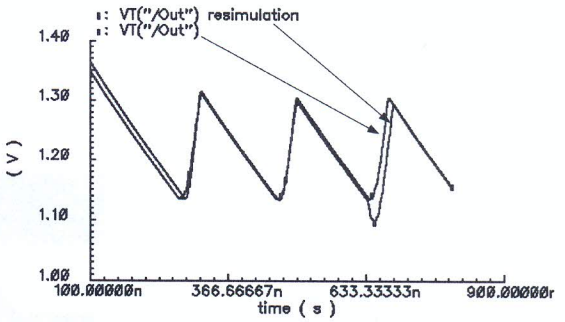

Figure 12. Output voltage V_{out} respectively before and after layout design when PFM control technique is used.

III. Conclusion

In this paper dc – dc buck converter integrated on CMOS 0.35 μm technology is presented. Efficiency of whole system is investigated as a function of different circuit parameters. Power losses in the power stage are evaluated. PWM and PFM control techniques are developed. Resimulation results after layout design of the integrated circuit show good overlapping.

Acknowledgments

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