Design and Signal Processing Techniques on 0.18μm CMOS Hall Microsensors

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Abstract – **This paper presents the design of 0.18μm CMOS Hall plates, characterized with high sensitivity and very low offset and the further signal processing block comprised of main second order switched capacitor filter and anti-aliasing filter. As a result, we developed a method for signal processing, which presents minimal 1/f noise values.**

Keywords – **Hall microsensor, 0.18μm CMOS technology, offset, sensitivity, signal processing, switched capacitor filter.**

I. Introduction

Most of the magnetic sensors nowadays are used as integrated circuits, because of the opportunity the sensor and the electronic circuit which amplifies the signals to be integrated in one chip.

Hall effect switch sensors have been well established for their great application in many fields. Due to the development of the CMOS techniques and its advantageous characteristics related to cost, high-gain of amplifier and chip size, Hall sensors using CMOS technology has been proposed [1].

Unfortunately, CMOS integrated Hall sensors have suffered from a lot of non-idealities, such as large offset, temperature drifts, low sensitivity, non-linearity and packaging stress influence etc., which severely deteriorates their performance.

The reasons for these drawbacks are geometrical errors in mask alignment, mechanical strain, crystal damage and stress, non-uniform temperature distribution and heat dissipation in the substrate, thermoelectric voltage across Hall leads, non-homogeneities, etc. The problems with offset may come from process variation over the device, temperature gradients across the device in operation, mechanical stress imposed by packaging, etc. Different methods for offset compensation are known, as improvement of the manufacturing technologies, device symmetry, calibration, mutual compensation, trimming, spinning current offset reduction, etc [1] and [2].

Continuous time sensors are the most basic of the Hall effect sensors. Their architecture contains just a voltage regulator, the Hall transducer, an amplifier and a comparator with an output stage [3]. One of its major disadvantages is the big input offset voltage of the amplifier which in CMOS fabrication processes may have typical values of 1mV to 20mV multiple times larger than signal generated by the Hall transducer for usual magnetic fields values (1…20mT) which is smaller than 1mV. Common technique to reduce this offset voltage is to use a chopper stabilized amplifier which may have input offset voltages in the filed of 100μV and less. In this technique the amplifier modulates the input offset at a high frequency and then it has been removed using a low-pass filter. Another benefit is that when modulating the Hall transducer signal into the high frequencies, we are minimizing the noise. Chopper stabilization and the design of chopper stabilized switched capacitor amplifiers are presented in detail in [3] and [4].

In this paper we focus on the design of the subsequent filter stage and the necessary supplementary circuit blocks – switch control generation circuitry and anti-aliasing filter on a modern 0.18μm CMOS fabrication process.

II. Sensor Layout and Offset Compensation Method

The investigated Hall sensors were designed on 0.18μm CMOS technology. The designed sample is a thin plate of conducting material (pSi) with four electrical contacts at its periphery. A bias current (or voltage) is applied to the device through two of the contacts, called the current contacts (C1 and C2). The other two contacts are placed at two equipotential points at the plate boundary and are called the voltage contacts or the sense contacts. If a magnetic field is applied to the device, a voltage appears between the sense contacts, called the Hall voltage.

The Hall device is with the form of a square plate and is with microscopic dimensions (40x40μm). A bias voltage V_{DD} is applied to the plate through the two current contacts C_1 and C_2. The bias voltage creates an electric field *E* and forces a current *I*. If the plate is exposed to a perpendicular magnetic induction ***B***, the Hall electric field E_H occurs in the plate. The Hall electric field gives rise to the appearance of the Hall voltage V_H between the two sense contacts H_1 and H_2. The designed and investigated sensor's layout is illustrated on Fig. 1.

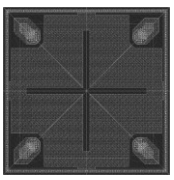

Fig. 1. Hall Plate Layout

The Hall microsensors were manufactured in a standard planar technology on p-Si wafers, with substrate resistivity 0,01 Ωcm and crystallographic direction (100). The heavy doped n+ and p+ regions are with depth of 35nm and STI (shallow trench isolation, which is used) depth is 400nm. The microdevices are confined in N-well, which serves as an active sensor zone with depth of 1.5μm.

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In order the offset to be compensated, a four-phase spinning method was used which involves a combination of reversing source voltage polarity and the input and output terminals, which is explained in details in [5]. Due to the fact that the Hall structure is symmetric with rotation, this technique leaves the output Hall voltage V_H unchanged in value and sign. During the terminals' rotation, this results in polarity reversion of the offset voltage.

III. Signal Processing

In accordance with the amplifier and subsequent comparator which both are often realized in switched capacitor manner, our filter will be also realized using switched capacitor design techniques. We have chosen elliptic approximation because of its optimally fast pass band to stop band transitions for a given maximum attenuation variation (ripple) and optimal group delay.

The filter specification is given in Table 1.

TABLE I
FILTER SPECIFICATION

Cut-off frequency: fc	15kHz ≥ 6 dB/oct
Transition band slope: fs	166.7 kHz
Stopband attenuation: As	≥ 20 dB
Attenuation on the odd harmonics of fs	≥ 40 dB
Maximum ripple - ε	≤ 0.5 dB
Step response overshoot	≤ 5%
Group delay	≤ 12 μs typ.
Sampling frequency - fCLK	1.33 MHz
Gain	5
Supply voltage range	3V ± 10%
Temperature range	-40°C ÷ 135°C

The stop band frequency is the same as the frequency of the modulated input signal. Step response overshoot should be less than 5% of the median value because of the subsequent comparator circuit. The sampling frequency was chosen 8 times the stop band frequency.

Our design is second order low pass elliptic switched capacitor filter, where the switches have the configuration from Fig.2.

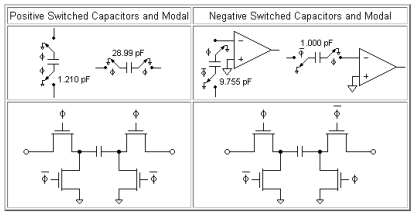

Fig. 2. Switch configurations

Its transfer function in the s-plane is:

$$H(s)=\frac{R_{1,4}C_{1,2}R_{1,7}C_{1,3}R_{1,1}R_{1,6}s^2-R_{1,4}R_{1,7}}{-R_{1,4}R_{1,7}C_{1,3}R_{1,1}R_{1,6}C_{1,5}s^2-R_{1,7}C_{1,3}R_{1,1}R_{1,6}s+R_{1,4}R_{1,1}} \quad (1)$$

where $R_{1,i}=\frac{1}{C_{1,i}f_{CLK}}$ (2)

The next step in the design of switched capacitor circuits is to choose switch topology and to verify its parameters. For this design we used 3.3V low power NMOS and PMOS devices available as part of the 0.18μm CMOS fabrication process. In order to minimize charge injection and complexity we have chosen the transmission gate as switch topology.

The other vital size dependable parameters of the switches are the charge clock feed through, which increases with W/L ratio, the on resistance which decreases with W/L ratio, the thermal noise which increases with the increase of the on resistance.

In order to obtain good balance between all these parameters and acceptable topological area, in the sizing process, the transmission gate was verified across supply voltage margins (2.7, 3.0, 3.3V), temperature margins (-40°C, 27°C, 125°C). Based on the worst case scenario, where R_{ON} of the switch should not exceed 5% of the minimal switched capacitor equivalent resistance in the design (because in "on state" it is in series with the equivalent resistance) and its calculated value, using (2) is 1.5MΩ.

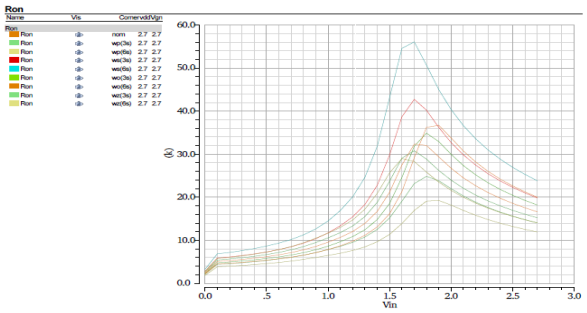

Fig. 3. Corner analyses of the transmission gate

We have chosen $\frac{w_N}{w_P}=\frac{w_P}{L_P}=\frac{0.4}{0.35}\mu m$.

As operational amplifier in the design of the filter, we used single stage amplifier with gain boosting stages and switched capacitor common-mode feedback, provided in the design kit for the given technology process. It is characterized by DC gain of 100 dB and gain bandwidth of 30MHz which were sufficient according to the rule of the thumb that the GBW should be 5 to 10 times the sampling frequency f_{CLK}.

In order to eliminate first order mismatch effects the capacitors were formed so that the ratio between their area and perimeter is kept constant. Capacitor dimensions and predicted mismatch are given in Table 2.

TABLE II
CAPACITOR DIMENSIONS AND MISMATCH

Label	Value [fF]	Area [μm²]	Perimeter [μm]	Mismatch [%]
C1.1	500	588.24p	130	0.056
C1.2	108.32	127.44p	28.16	0.12
C1.3	787.59	926.58p	204.78	0.044

C1.4	178.88	210.44p	46.51	0.093
C1.5	787.59	926.58p	204.78	0.044
C1.6	100	117.65p	26	0.125
C1.7	100	117.65p	26	0.125

The mismatch values were calculated based on the process specification according to (4).

$$\sigma(\frac{\Delta C}{C}) = \frac{X}{\sqrt{A}}[\%] \qquad (3)$$

where X ≈ 1.30 %/µm.

The filter schematic (Fig. 4) was verified with periodic analyses available in Cadence® Virtuoso® Spectre® circuit simulator – Periodic Steady State (PSS), Periodic AC (PAC) and transient analysis.

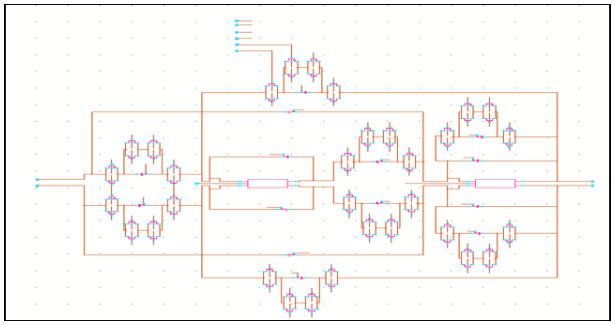

Fig. 4. Filter schematic in Cadence® Virtuoso®

As required by the Nyquist–Shannon sampling theorem we need one additional low-pass filter before the main switched capacitor filter to reduce the signal aliasing to minimum. According to the theorem the cut-off frequency of this filter should be calculated using (4).

$$f_{-3dB} = \frac{f_{CLK}}{2} \qquad (4)$$

But the optimum solution for our design (Attenuation on 1.33 MHz = -20 dB and group delay $\tau \leq 1\mu s$) is shown in (5).

$$f_{-3dB} = \frac{f_{CLK}}{10} = 133kHz \qquad (5)$$

The filter topology of choice will be first order passive low-pass filter with the well known transfer function, shown in (6).

$$f_C = \frac{1}{2\pi RC} \qquad (6)$$

And group delay is equal to (7).

$$\tau(f_C) = \frac{1}{2\pi fC} = RC \qquad (7)$$

The 133 kHz cut-off frequency is possible with R = 1MΩ и C = 1.2 pF but when taking into account the fully differential nature of our design we can halve the value of one of the elements. Because the resistors are two and their area is technologically larger than the capacitor area it is logical to choose to use R = 500kΩ.

When taking into consideration the load of the filter which is actually the input impedance of the main switched capacitor filter – R1.1E = 1.5MΩ and C1.2 = 100fF connected to the virtual grounds of the amplifiers, we have that in order to meet our specification for f-3dB we need to use R = 330kΩ.

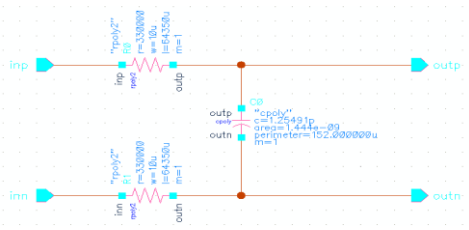

Fig. 5. Anti-aliasing filter schematic in Cadence® Virtuoso®

After optimization and for smaller process variations the capacitor was chosen with area of 38µm by 38µm and capacitance C = 1.25 pF.

IV. Experimental Results

The structure from Fig. 1 was tested at six supply voltages (0.5, 1.0, 1.5, 2.0, 2.5, 3.0V) and three constant currents (100, 200 and 300µA). Also the magnetic measurements involve generation of a perpendicular magnetic field which value is ±8mT. All measurements were taken at room temperature (25ºC).

The first experimental results for the residual offset are shown in Fig. 6a) at V_{DD} and in Fig. 6b) at I_{DD}.

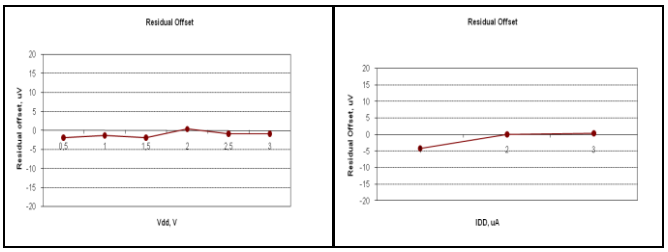

Fig. 6. Residual Offset as a Function of VDD (a)) and as a function of IDD (b))

At supply voltage the highest offset value is 1.42µV and at constant current supply is 2.41µV which are excellent results for such type magnetic sensors at this technology. They are specified to be under 10µV and they are much smaller than this value taking into consideration that the output signal is about mV. There is no need to use compensation offset circuits which complicate the design.

Next, the voltage and current related sensitivities were investigated. The maximum achieved voltage related sensitivity is $0.11T^{-1}$, and the current related sensitivity is 170V/AT. For example, typical value for the voltage related sensitivity is 0.5 to $0.8T^{-1}$. We achieved really high sensitivity in this technology which is a great advantage for our sensor. Typical value for S_I is from 85 to 250V/AT, but it depends on the size of the sensor and the supply constant current.

Next, the simulations were made in order to prove the performance of the designed filters, which will be part of the sensor integrated circuit. First frequency response, step and transient response of the second order low pass elliptic switched capacitor filter were given in Fig. 7, Fig. 8 and Fig. 9 respectively.

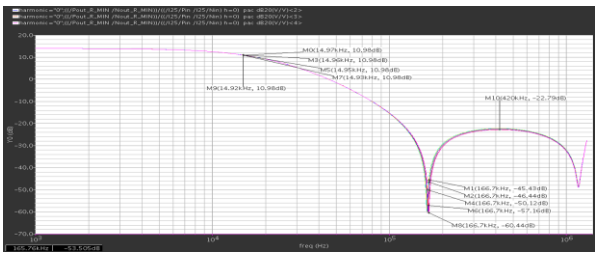

Fig. 7 Frequency response of the filter – PAC corner analyses

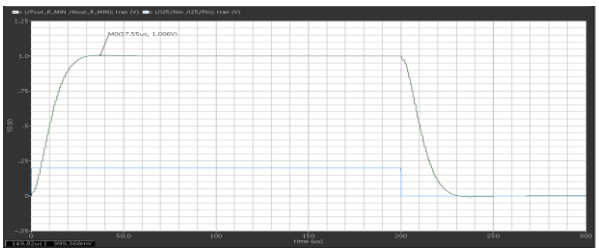

Fig. 8 Step response of the filter

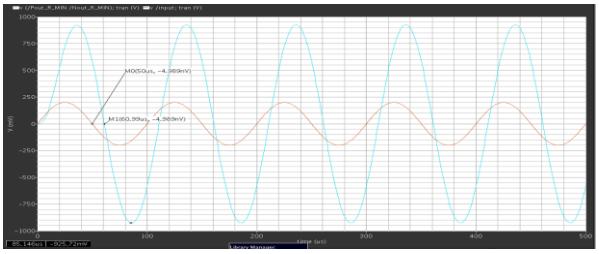

Fig. 9 Transient response of the filter for group delay verification typical conditions (27°C, VDD = 3V)

The switch control clock generation circuit have been developed prior the design of the main switched capacitor filter so that the later be verified with real control signals for the switches.

Next the anti-aliasing filter was simulated to see the frequency response for verification of the cut-off frequency (Fig. 10).

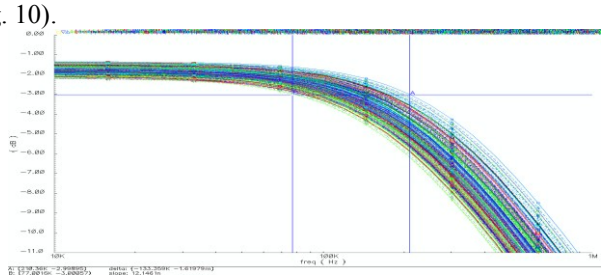

Fig. 10 Frequency response of the AA filter for verification of the cut-off frequency

As seen from the above figure process and temperature variations have significant impact on the value of the cut-off frequency:

f_{Cideal} = 133.333 kHz

f_{Cmin} = 77.001 kHz≈-42% of the ideal value

f_{Cmax} = 210.360 kHz ≈+58% of the ideal value

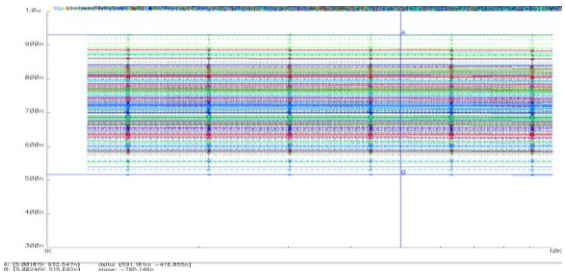

Fig. 11 Transient response of the AA filter for verification of the group delay

τ_{ideal}≈705 ns

τ_{min}≈516ns ≈ -27% of the ideal value

τ_{max}≈933ns ≈ +33% of the ideal value

The impact of the temperature and process variations is clearly seen in the group delay values as well but nevertheless the obtained values are well tolerable for the design margins.

CONCLUSION

In this paper microscopic Hall structure was designed and characterized, achieving highly sensitive sensor which have wide range of practical applications. We presented a method for signal processing in integrated CMOS Hall effect sensors, which greatly diminished sources of errors like amplifiers input offset voltage and the low frequency 1/f noise.

We have shown the design of several practical signal processing blocks: main low pass switched capacitor filter and anti-aliasing filter. Furthermore all of these blocks were designed and verified for 0.18µm CMOS fabrication process, so in effect this paper also shows the main characteristics and possibilities offered by this process for integrated Hall effect sensors.

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