USB Proceedings

ICIT 2013 - 2013 IEEE International Conference on Industrial Technology (ICIT)

Pavilion - Clock Tower Conference Centre
Cape Town, South Africa
25 - 28 February, 2013

Sponsored by

The Institute of Electrical and Electronics Engineers (IEEE)
IEEE Industrial Electronics Society (IES)
IEEE Technology Management Council
IEEE Region 8
IEEE South Africa Section IE/IA/PEL Joint Chapter

IEEE Catalog Number: CFP13CIT-USB
ISBN: 978-1-4673-4568-2

sensitivity of the three cells is due to the fact that they are with different size (20μm, 40μm and 80μm). As a comparison, a typical value for voltage related sensitivity in the literature is 0.05 to 0.08 T^{-1}. We obtained much higher sensitivity which is a key characteristic for such type magnetic devices. The highest current related sensitivity is 172.8 V/AT at 100μA. A typical value for current related sensitivity, mentioned in other state of the art works ([8] for example) is 250 V/AT at a biasing current of 350 μA.

Making a comparison between the three Hall cells (20 μm cell, 40 μm cell and 80 μm cell), and investigating their parameters, it can be concluded that the dimensions of the cells do not affect the residual offset values at temperature of 25 °C, the Hall voltage and the voltage related sensitivity are really with high value and are almost equal for 40 μm cell and 80 μm cell. So, taking into consideration these experimental results, the best choice for the designer, with respect to low residual offset, high output signal, high voltage related sensitivity and relatively small dimensions, is the 40 μm cell.

CONCLUSION

Summarizing microscopic Hall sensors were designed and characterized, achieving highly sensitive Hall sensors for integration in CMOS integrated circuits in the deep submicron region. One of the most common problems in the Hall sensors is the compensation of the offset and the proposed sensors are appropriate solutions, achieving offset in the micro scale without the need a compensation circuits to be used. The sensors show good stability and reproducibility of its parameters and are also compatible monolithic and hybrid Hall circuits with analog and/or digital output. The sensors are ready for a lot of applications as magnitometry, non-contact automation, etc. and can guarantee for long-term stability and low noise.

ACKNOWLEDGMENT

This work is funded with support from the SCOPES project "Skills development for young researchers and educational personal in nano and microelectronics curricula: implementation of methods for bilateral knowledge transfer between universities and SMEs", no. IZ74Z0_137353 and Contract no. 122PD0060-03.

REFERENCES

[1] Yue Hu, Wen-Rong Yang, "CMOS Hall Sensor Using Dynamic Quadrate Offset Cancellation", Sensors 2011, 11(6), 6284-6296; doi:10.3390/s110606284, P. R. China.

[2] S. Lozanova, Ch. Roumenin, "A novel parallel-field double – Hall microsensor with self-reduced offset and temperature drift", Science Direct, Procedia Engineering 5, 2012, pp. 617-620.

[3] Ed Ramsden, Hall Effect Sensors Theory & Application, Advanstar Communications Inc, 2001.

[4] F. Shanehsazzadeh and M. Sayedi, "OPTIMUM GEOMETRICAL PARAMETES FOR HALL SENSORS", International Journal of Applied Engineering and Technology ISSN: 2277-212X, 2012 Vol. 2 (1) January-March, pp.23-29/Shanehsazzadeh and Sayedi

[5] Ivelina N. Cholakova, Member, IEEE, Tihomir B. Takov, Radostin Ts. Tsankov, Nicolas Simonne, "Temperature Influence on Hall Effect Sensors Characteristics", 20th Telecommunications forum TELFOR 2012 Serbia, Belgrade, November 20-22, 2012, ISBN: 978-1-4673-2984-2, pp. 967-970.

[6] C. Roumenin, S. Noykov, S. Lozanova "THREE CONTACT PARALLEL-FIELD HALL MICROSENSOR WITH DINAMICALLY REDUCED OFFSET AND 1/f NOISE", Comptes rendus de l'Academie bulgare des Sciences, Vol. 63, No. 4, 2012, pp. 609-615

[7] Maria-Alexandra Paun, Jean-Michel Sallese, Maher Kayal, "Offset and Drift Analysis of the Hall Effect Sensors. The Geometrical Parameters Influence", Digest Journal of Nanomaterials and Biostructures Vol. 7, No. 3, July - September 2012, p. 883 – 891

[8] C. Schott, R. Racz, A. Manco, N. Simonne. "CMOS Single-Chip Electronic Compass With Microcontroller" Journal of Solid-State Circuits, Vol42, No.12, December 2007, Page(s):2923 - 2933.

Design and Investigation of 0.18μm CMOS Hall Sensors with different dimensions

Ivelina Cholakova, Tihomir Takov, Slavka Tzanova
Department of Microelectronics
Technical University
Sofia, Bulgaria
inch@ecad.tu-sofia.bg

Radostin Tsankov, Nicolas Simonne
Melexis
Sofia, Bulgaria
rts@melexis.com

Abstract—**Horizontal CMOS Hall microsensors, comprising a silicon substrate and four contacts, providing simultaneously two supply inputs and two differential outputs, are designed and characterized. The influence of the geometry of the Hall cells is analyzed and how it affects the offset, the Hall voltage and the sensitivity of the devices. Experimental results for the parameters of interest are given for three different sizes, designed in 0.18μm CMOS technology, using certain biasing voltages. The purpose is the best Hall cell dimensions to be selected.**

Index Terms—**Horizontal Hall microsensors, offset compensation, voltage related sensitivity, current related sensitivity, 0.18μm CMOS technology.**

I. INTRODUCTION

Hall effect switch sensors have been well established for their great application in the DC brushless motor, position sensors, etc. Due to the development of the CMOS techniques and its advantageous characteristics related to cost, high-gain of amplifier and chip size, Hall sensors using CMOS technology has been proposed [1].

Unfortunately, CMOS integrated Hall sensors have suffered from a lot of non-idealities, such as large offset, temperature drifts, low sensitivity, non-linearity and packaging stress influence etc., which severely deteriorates their performance.

The reasons for these drawbacks are geometrical errors in mask alignment, mechanical strain, crystal damage and stress, non-uniform temperature distribution and heat dissipation in the substrate, thermoelectric voltage across Hall leads, non-homogeneities, etc. In integrated Hall effect transducers where features can be defined with very high submicron resolutions, geometric flaws can be a source of output offset voltage. The problems with offset may come from process variation over the device, temperature gradients across the device in operation, mechanical stress imposed by packaging, etc. Process variations, as amount and depth of doping, can vary slightly over the surface of a wafer which can lead to very slight non uniformities between individual devices. Different methods for offset compensation are known, as improvement of the manufacturing technologies, device symmetry, calibration, mutual compensation, trimming, spinning current offset reduction, etc [2] and [3]. The magnetic sensitivity or the transduction efficiency is the most important figure of merit of the magntosensitive devices and all other types of sensors.

The geometry plays a key role on the Hall-effect sensors performance and has been studied a lot by the authors. The development of an efficient compact model of CMOS integrated Hall sensors is therefore a big factor that will improve design time and efficiency, and which will widen the applications range of Hall devices in integrated systems [4].

The present paper analyzes the influence of the dimensions of the Hall plates. Our aim is to assess the key parameters, in order the optimum structure for future projects in this technology to be chosen.

II. SENSORS STRUCTURE AND MODE OF OPERATION

The investigated sensors are with higher degree of symmetry and the input and output terminals are interchangeable. Because the positions of the sensors' terminals are absolutely symmetrical, the two contacts are equipotential when applying a supply voltage and in the ideal case there is a zero offset in the absence of magnetic field. In a magnetic field $\boldsymbol{B} \neq 0$, the total Hall voltage generated in the sensor appears between the output terminals. In order the geometrical correction factor to be increased, the contacts should be with minimal dimensions. The output is a linear function of the supply current or voltage and the magnetic field $\boldsymbol{B}$.

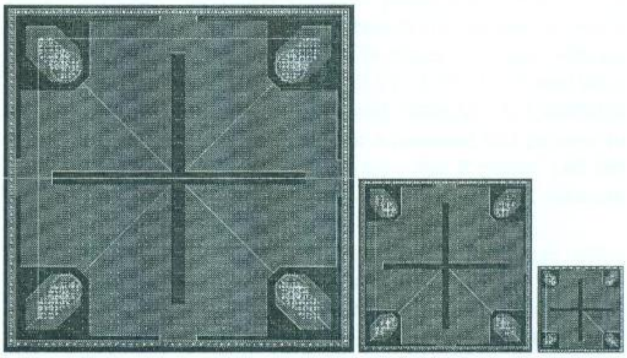

Fig. 1. Hall sensors with dimensions 80 μm, 40 μm and 20 μm respectively.

The Hall devices have equivalent contacts and therefore some compensation methods can be used to suppress the offset.

The Hall microsensors were manufactured in a standard planar technology on p-Si wafers, with substrate resistivity 0.01 Ωcm and crystallographic direction (100). The heavy doped n+ regions and p+ regions are with depth of 35nm. The microdevices are confined in N-well, which serves as an active sensor zone with depth of 1.5μm. The isolation between n+ and p+ regions is shallow trench isolation and its depth is 400 nm. Fig. 2 illustrates the measurement principle [5].

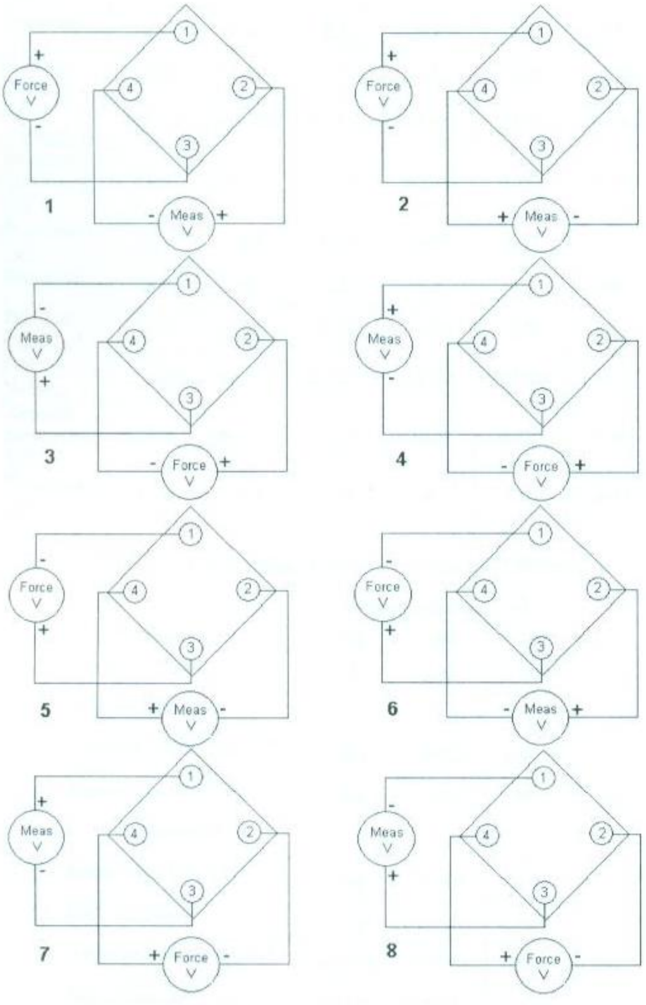

Fig. 2. Measurement principle.

The measurements involve forcing a voltage (from 0.5V to 3.0V with step 0.5V) and measuring a voltage (Hall voltage). The basic idea of the four-phase spinning approach lies in reconnection of the relevant contact pairs, whereas the bias contacts become output contacts, and the supply contacts are used as sense terminals. Due to the fact that the Hall structure is symmetric with rotation, this technique leaves the output Hall voltage V_H unchanged in value and sign.

The Hall plate can be presented as a Wheatstone bridge and the ohmic offset can be represented as a small difference ΔR in value of some of the four identical leg resistors, for example $(R_3+\Delta R) \neq R_1$, $R_1 = R_2 = R_4$. So, the Hall sensor is not symmetric with respect to the location of this "leg resistor" in the Wheatstone bridge. During the terminals' rotation, this results in polarity reversion of the offset voltage. The net effect is "to see" the Hall signal as rotating in the same direction as the bias voltage, while the ohmic offset rotates in the opposite direction. If those two periodic measurements of the output voltage $V_H + V_{OFF}$ and $V_H - V_{OFF}$ are averaged, the true value of the output Hall voltage will be obtained [6].

III. EXPERIMENTAL RESULTS

Three Hall effect microsensors, implemented in 0.18μm CMOS technology have been measured and analyzed in terms of specific parameters, such as residual offset, voltage and current related sensitivity and Hall voltage. All structures are symmetric and invariant to a rotation with π/2.

In order more automated process of measurements to be achieved, the test equipment shown in Fig. 3 was created and implemented.

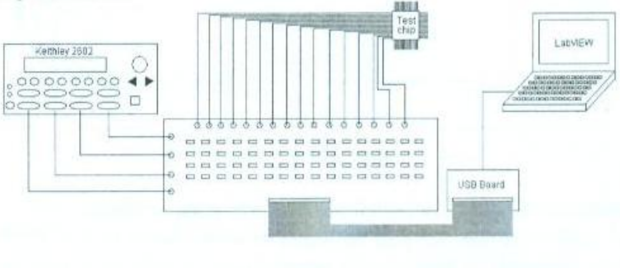

Fig. 3. Test equipment

A four-phase spinning method is used for offset compensation, which involves a combination of reversing source voltage polarity and Hall voltage polarity and also reversing the input and output terminals.

The equipment gives the opportunity four Hall plates to be tested at once. It is composed of one switch matrix board with 64 relays which switch the Hall plates' diagonals for offset compensation. Also for chip measurements a Keithley 2602 was used, which is duo channel source meter with 10 000 readings/s and 5500 source-measure points/s to memory. The first channel is used to supply the sensors and the second one is used to measure the output signal. The plates are tested with six supply voltages (0.5V, 1.0V, 1.5V, 2.0V, 2.5V, 3.0V) and three supply currents (100μA, 200μA and 300μA). A LabVIEW program was created in order more automated test process to be achieved. Its functions are to drive the Keithley and the switch matrix board, so consecutively to supply and measure all diagonals of the tested four Hall structures.

Characterization was performed on all structures using voltage biasing without and with magnetic field.

The results for the residual offset, measured using the 4-phase spinning technique for the three dimensions of the Hall plates, Hall voltage, absolute sensitivity and magnetic field equivalent residual offset, at voltage biasing are shown in Table I and at current biasing are shown in Table II.

TABLE I. EXPERIMENTAL RESULTS AT VOLTAGE BIASING

	Supply Voltage, V					
20µm cell	*0.5*	*1.0*	*1.5*	*2.0*	*2.5*	*3.0*
Residual Offset, µV	-0.03	-0.97	2.29	1.65	-0.77	-4.05
Hall Voltage, V	0.42	0.84	1.25	1.66	2.07	2.46
Absolute Sensitivity, V/T	0.051	0.103	0.155	0.206	0.256	0.306
$B_{ResidualOffset}$, µT	0.58	9.3	14.7	8.0	3.0	13.2
40µm cell	*0.5*	*1.0*	*1.5*	*2.0*	*2.5*	*3.0*
Residual Offset, µV	-0.26	-0.86	0.70	-1.23	-1.42	-0.92
Hall Voltage, V	0.1128	0.1129	0.1126	0.1123	0.1121	0.1119
Absolute Sensitivity, V/T	0.056	0.112	0.168	0.225	0.280	0.336
$B_{ResidualOffset}$, µT	4.62	7.64	4.14	5.46	5.07	2.73
80µm cell	*0.5*	*1.0*	*1.5*	*2.0*	*2.5*	*3.0*
Residual Offset, µV	-1.52	1.85	1.19	-3.23	-2.75	1.17
Hall Voltage, V	0.1145	0.1137	0.1139	0.1136	0.1138	0.1135
Absolute Sensitivity, V/T	0.056	0.113	0.171	0.227	0.285	0.340
$B_{ResidualOffset}$, µT	27.0	16.2	6.94	14.1	9.64	3.44

TABLE II. EXPERIMENTAL RESULTS AT CURRENT BIASING

	Supply Current, µA		
20µm cell	*100*	*200*	*300*
Residual Offset, µV	3.29	2.48	3.09
Hall Voltage, mV	13.7	27.5	41.5
Absolute Sensitivity, V/T	0.0171	0.0343	0.0519
$B_{ResidualOffset}$, µT	192	72.4	59.7
40µm cell			
Residual Offset, µV	2.41	0.214	2.37
Hall Voltage, V	13.6	27.1	40.9
Absolute Sensitivity, V/T	0.0170	0.0338	0.0511
$B_{ResidualOffset}$, µT	142	6.34	46.6
80µm cell			
Residual Offset, µV	3.91	0.894	3.165
Hall Voltage, V	13.5	25.4	39.3
Absolute Sensitivity, V/T	0.0168	0.0317	0.0491
$B_{ResidualOffset}$, µT	233	28.2	64.4

The absolute sensitivity is calculated using (1):

$$S_A = \left|\frac{V_H}{B}\right|, V/T. \tag{1}$$

V_H is the Hall voltage, $\boldsymbol{B}$ is the normal component of the magnetic induction.

The magnetic field equivalent residual offset is calculated using (2).

$$B_{ResidualOffset} = \left|\frac{V_{offset,residual}}{S_A}\right|, T. \tag{2}$$

$V_{OffsetResidual}$ in Volts is the residual offset voltage, obtained after the application of the current spinning technique, S_A is the absolute sensitivity.

The graphic of the residual offset for the three structures is shown in Fig. 4.

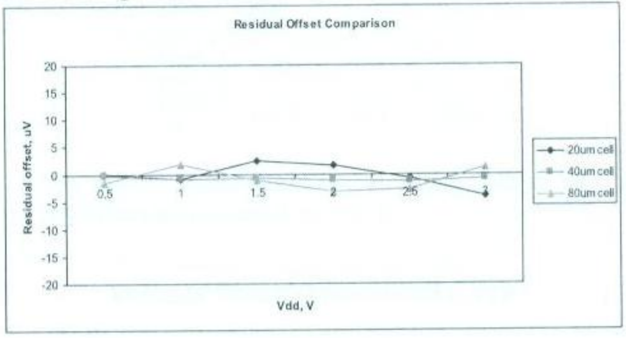

Fig. 4. Residual Offset.

The measurements are accomplished at room temperature (25 °C). It is clearly visible from the graphic that the offset do not vary a lot due to the different dimensions of the cells, so it can be concluded that at room temperature the size of the Hall sensor do not affect the offset value.

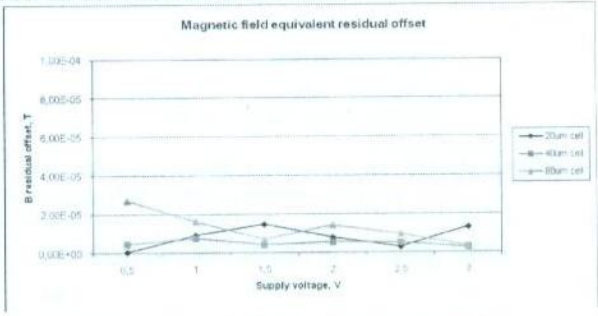

Fig. 5. Magnetic Field Equivalent Residual Offset.

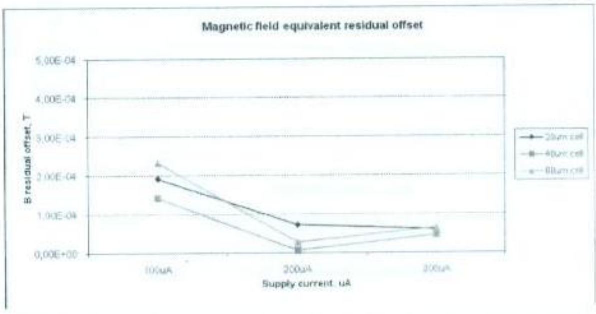

Fig. 6. Magnetic Field Equivalent Residual Offset

Fig. 5 displays the magnetic field eqiuvalent residual offset characteristics at room temperature with respect to the supply voltage, for the proposed three dimensions of the Hall sensors. As it can be seen the lowest residual offset is for the 20μm and 40μm Hall cells. The 40μm cell distinguishes itself by having residual offset under 10μT for the sixth supply voltages. Fig. 6 illustrates the magnetic field equivalent residual offset at current biasing. The results, compared to [7] are not high enough to affect our sensors' characteristics.

Next, the Hall effect voltage was measured for magnetic field $\boldsymbol{B} = 8$ mT and $\boldsymbol{B} = -8$ mT respectively. The achieved Hall effect voltage as a function of the increasing supply voltage is illustrated on Fig. 7. The higher measured value at $\boldsymbol{B} = -8$mT is 2.75mV for the 80μm cell and the lower value is 2.46mV for the 20μm cell at room temperature. The Hall voltage is increased by an increasing in dimensions of the sensors, but this trend does not continue infinitely, as the dimensions are larger. This is traded off between Hall voltage and space. It is clearly visible that for 40 μm cell and 80 μm cell the Hall voltage no longer increases a lot as it is increasing comparing the 20 μm and 40 μm cells. So, the designer should choose the right value for dimension in order to have an optimum sensor.

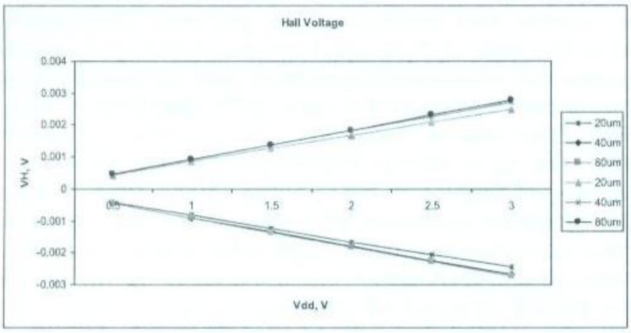

Fig. 7. Hall voltage as a function of the supply voltage.

Also voltage and current related sensitivities are measured and investigated. In Tables III and IV the calculated values are presented for the three Hall cells. The voltage related sensitivity is calculated using (3).

$$S_V = \frac{V_H}{V_{DD}B}, T^{-1}. \tag{3}$$

And the current related sensitivity is calculated using (4).

$$S_I = \frac{V_H}{I_{DD}B}, V/AT. \tag{4}$$

S_V is the voltage related sensitivity, V_H is the Hall voltage, V_{DD} is the supply voltage, I_{DD} is the current biasing and $\boldsymbol{B}$ is the applied magnetic field.

TABLE III. VOLTAGE RELATED SENSITIVITY [V/VT]

Plate size	**Supply Voltage, V**					
	0.5	***1.0***	***1.5***	***2.0***	***2.5***	***3.0***
20μm cell	0.1038	0.1035	0.1033	0.1031	0.1026	0.1021
40μm cell	0.1128	0.1129	0.1126	0.1123	0.1121	0.1119
80μm cell	0.1145	0.1137	0.1139	0.1136	0.1138	0.1135

TABLE IV. CURRENT RELATED SENSITIVITY [V/AT]

Plate size	**Supply Current, μA**		
	100	***200***	***300***
20μm cell	171.1	171.7	172.8
40μm cell	169.5	169.2	170.3
80μm cell	168.2	162.4	163.8

The voltage related sensitivity at supply voltage 3.0V, for the three sizes are presented on Fig. 8.

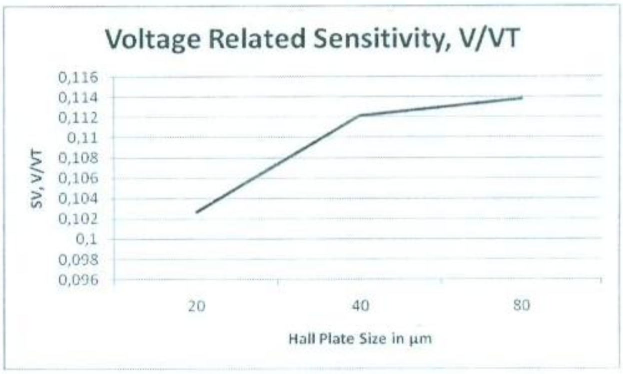

Fig. 8. Voltage related sensitivity.

The current related sensitivity at 100μA for the three dimensions Hall plates is shown in Fig. 9.

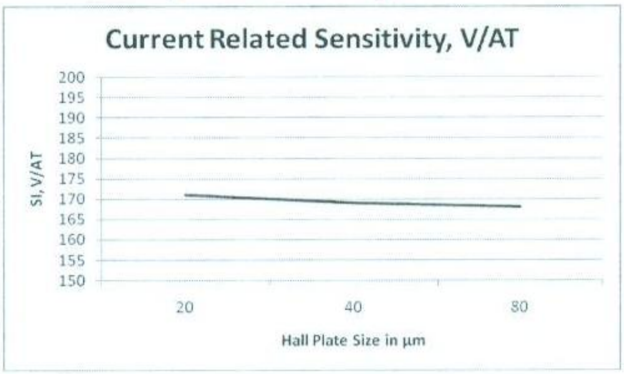

Fig. 9. Current Related Sensitivity

The achieved sensitivity is 0.10 T^{-1} for the 20μm cell and 0.11 T^{-1} for 40μm and 80μm cell. The difference in the