Measurement of PCB deformation during parametric testing and evaluation of the impact on the installed components

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Abstract—**Using the IPC / JEDEC-9704 and KEMET-MLCC (Multilayer Ceramic Chip Capacitors) Fex Failure Rate standards is a defined area of critical deformation in parametric testing of circuit boards. An intelligent measuring system was used to measure and determine the deformation, as well as a methodology for conducting experimental measurements. The results of practical studies of deformations in parametric testing of electronic modules on a panel for a specific automotive product are presented. A conclusion is made using the obtained results with conclusions about the acceptability of the process according to the standard and analysis of the transients in parametric testing.**

*Keywords— **electronic modules, standard, parametric testing, deformations, statistics***

I. Introduction

It is essential in the production of electronic modules to apply the optimal design for long-term and stable operation, especially in the spirit of EU decisions to reduce e-waste and pollution. The main reasons leading to module failures are related to the appearance of defects during installation and testing of elements on the board [1]. A significant contribution to the appearance of defects, the result of installation processes and testing, is the occurrence of mechanical stress, both during installation and during testing, leading to mechanical failure of elements [2].

For modern electronic devices, it is necessary to check the saturated boards for functionality and suitability. The testing is parametric, functional and mixed and is performed by different types of contacting, measuring and analysis [3]. Parametric testing [4] is widely applicable in mass production because it provides information about functionality at the element level. The assessment of mechanical stress is one of the determining factors for maintaining high reliability during the operation and aging of the product.

In all cases, however, the question is to determine the deformations in this case by applying the appropriate methodologies. For this purpose, the standards [5, 6] and a specific methodology for measurement and analysis are applicable. Depending on the setting, the type of strain gauge, measurement scheme and impact are selected [7]. If the results are critical, options for additional mechanical hardening are sought by changing the structure or non-standard methods of contact [8] and soldering [9], [10].

II. Procedure

A. Standard procedure

The purpose of this development is validation and maintenance of a process of parametric testing in the production of electronic modules by measuring and analyzing mechanical stress on components.

The control of the bending of the boards by measuring mechanical stress has established itself as an accepted method for detecting and preventing failures in the production processes of the electronics industry. The complexity of the modules determines an increased concentration of components, which in turn leads to an increase in the potential for damage. This requires a large number of electronic module manufacturers to produce with certain limits on the stress levels imposed by customers and component suppliers. Mechanical stress measurement technologies use different methodologies, which makes it impossible to compare data and measurement results. The standard covers variations in the placement of sensors, their positioning, the design of the experimental installation, the data collected and the units of measurement. The measurement itself includes the placement of the sensors at the specified places on the board and the measurement of the deformation in the technological process of assembly. Processes in which stress levels are above certain limits are considered dangerous, and corrective action should be taken immediately. In determining the tolerable levels of stress, the following factors are mainly taken into account:

• Manufacturer's specification, which indicates the permissible stress levels related to the dimensions of the components - fig. 1. to the left.

• Permissible levels in accordance with the results of mechanical stress measurements in direct dependence on the stress rate / change in the absolute value of stress per unit time.

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The relationship between the stress rate, the absolute value of the stress and the thickness of the board is shown in fig. 1. to the right.

A KEMET-MLCC Fex Failure Rate diagram was used for the allowable stress levels at 100 ppm depending on the dimensions of the SMT components and the IPC / JEDEC-9704 standard, describing the specific guidelines for stress testing of assembled printed circuit boards.

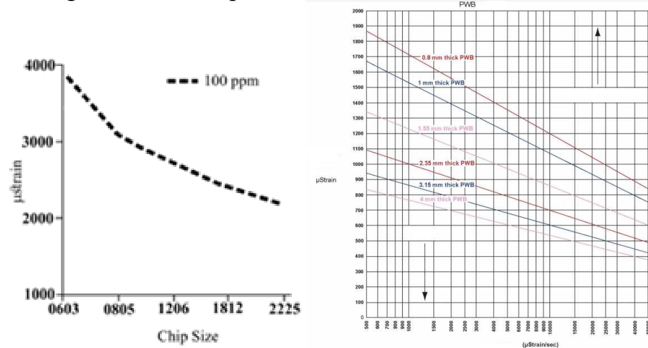


Fig. 1. KEMET-MLCC (Multilayer Ceramic Chip Capacitors) Fex Failure Rate [KEMET inc.] and diagram for determining the maximum stress depending on the thickness of the board (IPC/JEDEC-9704)

B. Application

The purpose of this decision is to prevent the consequences of component overload in the production and testing of electronic modules and to create prevention tools. The test itself allows to make an objective analysis of the stress levels on SMT components during the parametric testing process.

Using the specific specifications of the module under study in this work, which is constructed with components 0603, which are mounted on a board with a thickness of 1.55 mm and according to the standards used, shown in Fig. 1, a mechanical stress limit value of 1000 με.

When a tensile force is applied to the material, normal stresses σ appear in it, which are related to the applied force. The extensions of the material shown in Fig. 2 to the left.

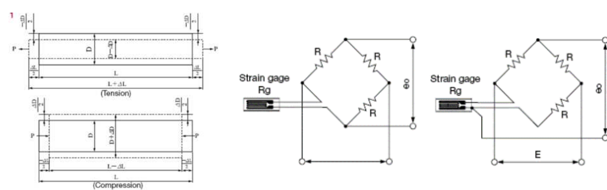


Fig. 2. Relationship between tension, stress and position [Vishey Beyschlag] and strain gauge with its connection scheme in the Wheatstone bridge

The ratio of the elongation to the original length is called the tensile stress:

$$\varepsilon = \Delta L / L \tag{1}$$

If the applied force is under pressure, then the ratio takes the following form:

$$\varepsilon = (-\Delta L)/L \tag{2}$$

The connection between stress and tension is expressed through Hooke's law:

σ=E.ε, where ε is stress, E is modulus of elasticity, σ is internal stress.

The specific resistance of the sensor (Fig. 2. on the right) increases (decreases) when it is subjected to tensile forces (pressure). The ratio of the change in resistivity to the original resistance is equivalent to the product of the voltage with the coefficient expressing the sensitivity of the sensor:

$$\frac{\Delta R}{R} = \frac{\Delta L}{L} K_s = \varepsilon K_s \tag{3}$$

For more accurate reading, the Wheatstone bridge shown in fig. 2. to the right, through which the changes of the resistances are transformed into changes of the voltages.

Thus the output voltage is proportional to the change in resistance, ie. of the change of the applied forces (stresses):

$$l_o = \frac{(R_1 \Delta R) R_3 - R_2 R_4}{(R_1 + \Delta R + R_2)(R_3 + R_4)} E = \\ = \frac{1}{4} \frac{\Delta R}{R} E = \frac{1}{4} K_s \varepsilon E \tag{4}$$

When measuring stress, the measuring frequency, bitrate and signal level play a decisive role. All samples must be received and processed simultaneously in order to avoid calculation errors. For correct measurement in the present experiment in parametric testing were used:

1. Measurement frequency – 5000 Hz;
2. IC Tester SPEA 3030 Multimode;
3. IC Test Head;
4. Sequence of actions:
- Insert the panel into the IC Test head;
- Testing.

The location of surfactants is selected to be close to critical components, and their appearance is consistent with the recommendations for their use. The investigated module with the mounted strain gauges is shown in Fig. 3.

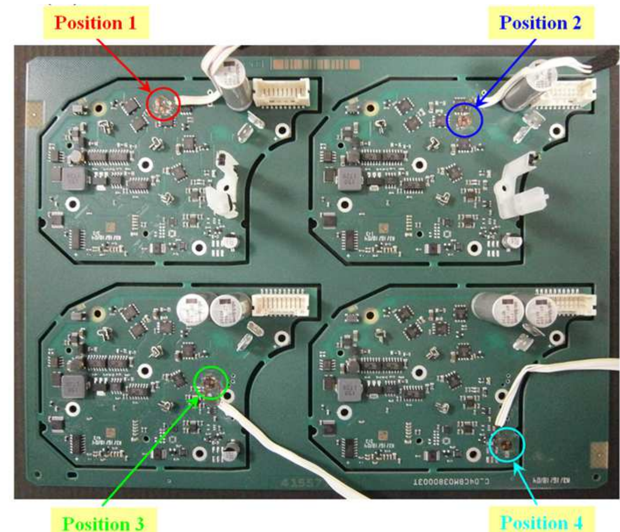


Fig. 3. Experimental panel with located sensors

The mounted strain gauges with the respective measuring channels are shown in Fig. 4.

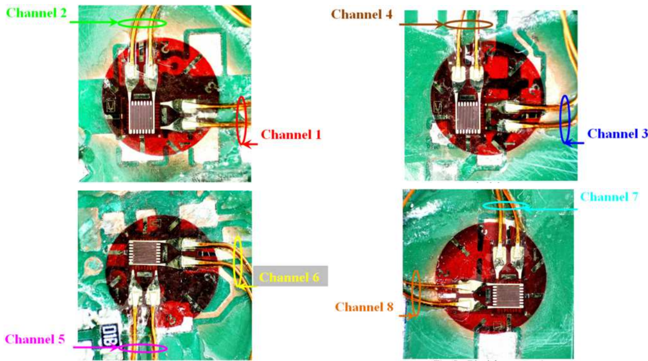


Fig. 4. Strain gauges and their connection

Strain gauge specification according to fig. 4 is:

Position 1, 2, 3, 4: KFG-1-120-D16-11L3M3S, Biaxial, 120.8 **Ω**, scale gage factor (Fig. 4):

- channel 1 – 2.08
- channel 2 - 2.08
- channel 3 - 2.08
- channel 4 - 2.08
- channel 5 - 2.08
- channel 6 - 2.08
- channel 7 - 2.08
- channel 8 - 2.08

In the present experiment, the intelligent measuring system shown in Fig. 5 with the following specification:

1. Measuring interfaces KYOWA PCD 300A - 4 channels - 2 pieces;

2. HP Pavilion G6 Notebook PC / Intel Core i7 - 3.1GHz, 8Gb RAM /;

3. Measuring software - PCD 30A;

4. DAS 100 analysis software.

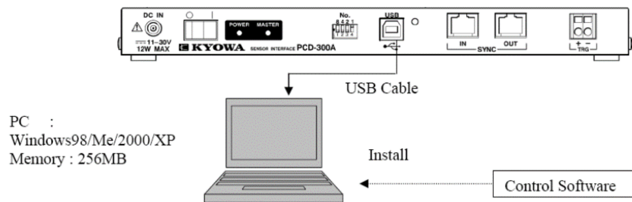


Fig. 5. KYOWA intelligent measuring system

In Fig. 6 shows the experimental set-up, which consists of an SPEA tester, a contact head fixator for the test panel and the panel with the connections between the mounted strain gauges and the KYOWA measuring equipment. The clamp used has a vacuum-driven piercing of the contact head and a large area.

There is a possibility to use statistics and machine learning for optimal testing, which is also used in the present experiment. The measured results processed in this way are used in real time with great reliability, which allows for fast and accurate analysis with subsequent actions to maintain the necessary reliability.

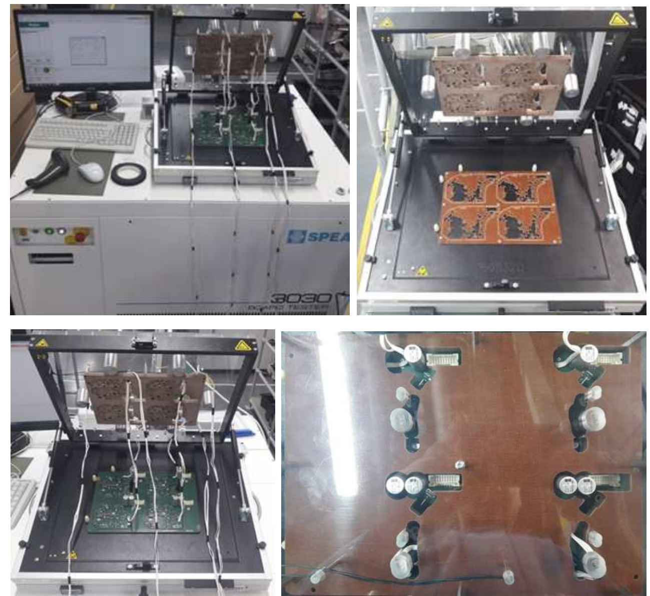


Fig. 6. Experimental staging with a studied panel

They were used for the specific experiment:

- PCB with dimensions – **245x220x1.6mm;**
- Type of PCB – **FR4 TG≥150 C** – multilayer;
- 4 modules on a panel with 5 bridges with dimensions **4x2x1.6mm;**
- Top and bottom board are 30mm, center board 24mm.

The preparation of the tested panel is done precisely and in accordance with the instructions of the strain gauge manufacturer, as well as with the requirements of the IPC / JEDEC-9704 standard, which includes:

- IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits;
- IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies;
- IPC-9701 Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments;
- IPC/JEDEC-9702 Monotonic Bend Characterization of Board - Level Interconnects;
- IPC 9703 Mechanical Shock Test Methods and Qualification Requirements for Surface Mount Solder Attachments.

The methodology for the assessment of the deformations of the board during its testing is important for determining the specificity of rigid, flexible boards and rigid-flexible boards. The obtained results can also be compared with the testing of micromodules.

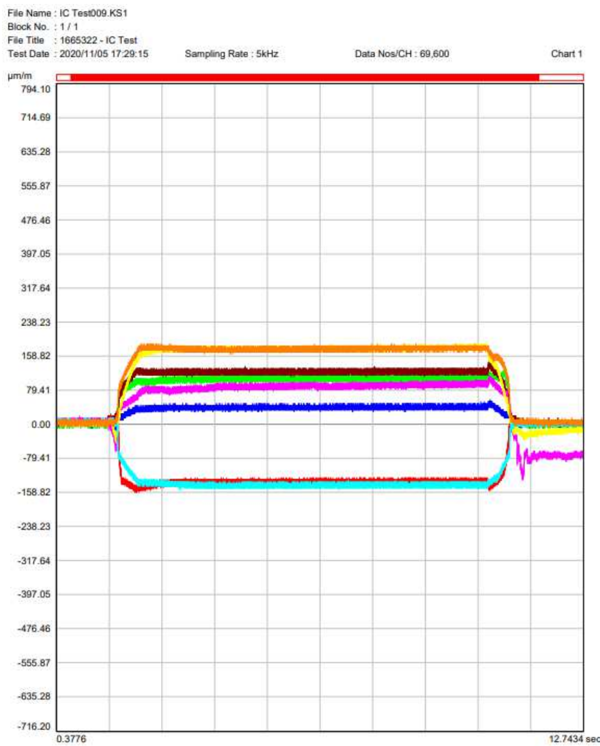
Of particular interest is the effect of deformation on contact with probes in the case of active tuning of hybrid circuits or micromodules.

III. Results

A. Measurement results

Following the test instructions with the SPEA 3030 Multimode tester, the electronic module was tested.

In Fig. 7. the obtained results from the measurement are shown.



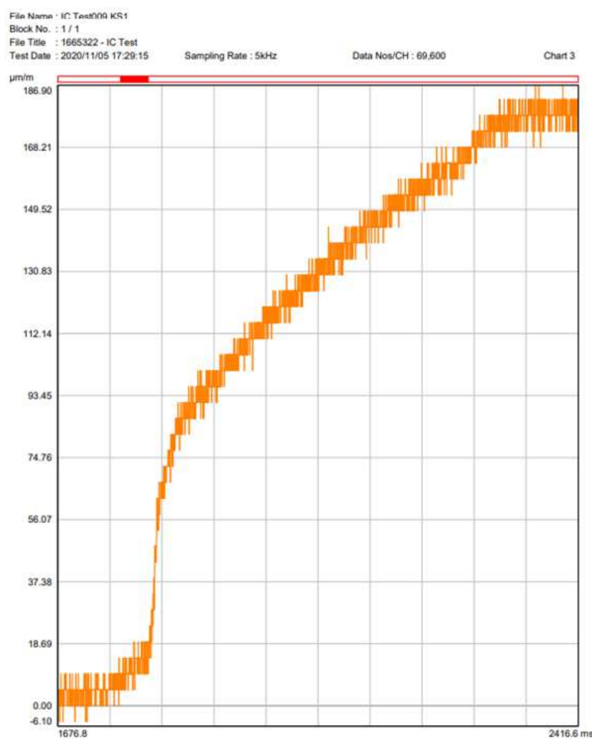


Fig. 7. ICT measurement results

The maximum value of the deformation is 186.9 με and is measured on channel 8, according to Fig. 7 Chart 1 and Chart 2. The processing time for ICT is 9 seconds. In fig. 7 Chart 2 has a stress background of 15 με and a maximum unit amplitude of 50 με.

B. Analysis

According to the thickness of the PCB, taking into account the requirements of Fig. 1, the maximum deformation must not exceed 1000 με. During the measurement, a maximum value of 186.9 με was recorded for all monitored points. Therefore, the deformations at the critical points in the periphery of the panel are many times lower, which allows for future further optimization of the location of elements within the board, as well as the design of the panel.

IV. Conclusion

The requirements and methods for determining the stress in printed circuit boards in the process of their production and specifically for the parametric test are applied. Variants for determining the control points, fixing the sensors and measuring for a specific board and panel topology are presented. The results are for the ICT (In-circuit tester) process.

After many measurements and analysis of the results, we can assume that the described method is a necessary tool for prevention, as well as a method for locating and proving sources of mechanical stress in parametric testing.

The methodology has the potential for development at the micro level in probe control of micromodules and active adjustment of the same.

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