A Neural Synapse Based on Ta_2O_5 Memristor

Valeri Mladenov
Department of Theoretical Electrical Engineering
Technical University of Sofia
Sofia, Bulgaria
e-mail: valerim@tu-sofia.bg

Stoyan Kirilov
Department of Theoretical Electrical Engineering
Technical University of Sofia
Sofia, Bulgaria
e-mail: s_kirilov@tu-sofia.bg

***Abstract* — The main purpose of this paper is to propose an improved memristor-based synaptic scheme, containing a resistor-memristor current divider and a differential amplifier with Metal Oxide Semiconductor (MOS) transistors. The memristor is made of tantalum oxide, doped by oxygen vacancies. The synaptic circuit contains only one memristor and produces positive, zero and negative weights. The applied tantalum oxide memristor model is based on the classical Hewlett-Packard model with several modifications and simplifications. Owing to the applied optimizations, the considered memristor model is faster than the corresponding original model. The synaptic weights of the considered memristor scheme, applied in a neural network are adjusted by voltage pulses and its operation is analyzed in LTSPICE environment.**

Keywords — tantalum oxide memristor, simplified memristor model, memristor-based synapse, differential amplifier

I. Introduction

In the last 10 years the memristor element predicted by Chua [1] and first realized in the Hewlett-Packard research labs by Williams [2] is an object of intensive investigations [3], [4], [5], [6]. It is a two-terminal element, which conductance depends on the time integral of the voltage [2], [6]. It has a memory effect – retaining the value of its conductance after switching the sources off [1], [2], [7]. The observed resistance switching effect is related to the change of memristor's state owing to an applied external voltage signal [3]. Due to their useful properties, as switching and memory effect, the memristors could be applied in many electronic schemes and devices of different kind – nonvolatile memories [7], reconfigurable devices [8], neural networks [9], [10] and others [4], [6]. The memristors are mainly based on transition metal oxides, as TiO_2 [2], [3], HfO_2 [3] and Ta_2O_5 [5], [11]. In the recent several years the tantalum oxide is under intensive investigations as a perspective material for creating memristors owing to its stable switching properties [5], [11]. For simulation of memristor schemes appropriate models must be available [11]. Several enhancements of the original Ta_2O_5 memristor model [11] are made [12], [13], [14], [15].

According to the application of memristors in synaptic schemes, minimization of the number of the used memristors per synapse and realization of positive, zero and negative weights are very important tasks [9], [10], [16]. Several basic realizations of memristor synapses exist in the scientific literature [10], [16], [17], [18], [19]. The partial absence of simplified memristor synapses with minimal number of memristors and capable to realize positive, zero and negative weights is the main motivation for the paper. The improved memristor model [15] is applied for analysis of a neural network with memristor synapses. Paper [19] presents a unified and LTSPICE memristor models' library which is freely available at https://github.com/mladenovvaleri/Advanced-Memristor-Modeling-in-LTSpise [19]. The applied memristor model is available in the considered library [19].

The proposed synaptic device [19] contains a memristor, a resistor and a differential amplifier with Metal Oxide Semiconductor (MOS) transistors. It is applied and successfully tested in a simple neural network [20] for estimation of several risk factors affecting the COVID-19 illness [21], [22] for potential patients, and the results are presented in [20]. The considered synapse realizes positive, zero and negative weights with a memristor per synapse. The applied differential amplifier ensures scaling of the synaptic weights.

The rest of the paper is organized as follows. Section 2 briefly represents the basic tantalum oxide memristor models, the applied in the work modified model and its LTSPICE equivalent schematic. In Section 3 the considered memristor-based synapse and its LTSPICE realization are presented. The tuning of the weights of the considered memristor-based neural synapse and its application in a neural network are discussed in Section 4. The conclusion is shown in Section 5.

II. Background of Ta_2O_5 Memristor Models, The Considered Model and Its LTSPICE Realization

Brief information about the main existing Ta_2O_5 memristor models [11], [12], [13] and the applied modified model [15], [19] is first given for better understanding and completeness of the presentation. The Ta_2O_5 memristor contains two terminals – top electrode and bottom electrode, respectively [11]. Several parallel-oriented conducting channels exist in its nanostructure [11], [12]. The peripheral region is made of stochiometric Ta_2O_5. The central channel is based on a solid solution of oxygen atoms in tantalum. An additional channel of doped tantalum oxide is formed between these two regions [11]. The state variable x is expressed as a ratio between the area of the conducting region and those of the entire memristor's intersection [11].

A. The Standard Hewlett Packard Memristor Model [11]

The maximal memductance is denoted by G_{max} and has a value of 0.025 S [11]. The conductance of the doped region is described by the Frenkel–Poole relationship [8], [9], [10], [11]. According to the standard Hewlett-Packard model for tantalum oxide memristors [11], the *i-v* relation is:

$$i = G_{eq} \cdot v = \left[a \cdot \exp\left(b \cdot \sqrt{|v|} \right) \cdot (1 - x) + G_{\max} \cdot x \right] \cdot v \qquad (1)$$

where a and b are fitting coefficients, G_{eq} is the equivalent conductance. The state equation of the memristor is [11]:

$$\frac{dx}{dt} = A \cdot \sinh\left(\frac{v}{\sigma_{OFF}} \right) \cdot \exp\left(-\frac{x_{OFF}^{\,2}}{x^2} \right) \cdot \exp\left(\frac{1}{1 + \beta\, i\, v} \right) \cdot stp(-v) + B \cdot \sinh\left(\frac{v}{\sigma_{ON}} \right) \cdot \exp\left(-\frac{x^2}{x_{ON}^{\,2}} \right) \cdot \exp\left(\frac{v i}{\sigma_P} \right) \cdot stp(v) \qquad (2)$$

where B, A, σ_{OFF}, σ_{ON}, σ_P, β, x_{ON}, and x_{OFF} are coefficients for adjustment of the model [11]. The included in equation (2) Heaviside step function *stp(.)* is [11], [12], [13]:

$$stp(v) = \begin{cases} 0, & v < 0 \\ 1, & v \geq 0 \end{cases} \qquad (3)$$

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The classical memristor model [11] is completely described by (1) and (2). It has a good precision and properly describes the behavior of Ta_2O_5 memristors in electronic schemes and devices [11], [12]. Its main drawbacks according to SPICE realization are the inclusions of non-smooth step function and a non-differentiable modulus function [11].

B. *Improvements of HP Ta_2O_5 Memristor Model [12], [13]*

The basic improvement in [12] is the replacement of the modulus expression and the Heaviside function by their smooth analogues [12]. The step-like smooth function used in the enhanced memristor models [12], [13] is:

$$f(v)=\frac{1}{1+\exp(k\cdot v)} \tag{4}$$

where k is a coefficient with a negative value of -100 [9]. An alternative of the non-differential modulus expression used in [11] is the following modulus-like function [12], [13]:

$$f_{\mathrm{mod}}(v)=v\cdot\left[\frac{1}{1+\exp(-\rho\cdot v)}-\frac{1}{1+\exp(\rho\cdot v)}\right] \tag{5}$$

where ρ is a fitting coefficient with a suitable value of 1000 [12], [13]. The main improvement in these models is the lack of convergence problems [12], [13]. A disadvantage of these modified models is their comparatively high complexity.

C. *A discussion on the applied Ta_2O_5 memristor model [15]*

The applied modified model contains several main replacements [15], [19]. The Heaviside function *stp(v)* in (2) is substituted by a smooth step-like alternative *s(v)* [15], [23]:

$$s(v)=\frac{v}{2\sqrt{m+v^2}}+0.5 \tag{6}$$

where m = 0.001 is a coefficient for fitting the steepness of the function in the region of switching [23]. The following term *F(v)=a.exp(b.sqrt(|v|))* in (1) is approximated by a low-order polynomial in MATLAB environment [24]:

$$F(v)=a\cdot\exp\left(b\cdot\sqrt{|v|}\right)\approx h_1\cdot v^4+h_2\cdot v^2+h_3 \tag{7}$$

where h_1, h_2 and h_3 are fitting parameters [15]. A simple smooth window function *f(x,i)* dependent on the state variable x and on the current i is applied. It is founded on the Biolek window [25] and on the logistic function (6) [15], [23]:

$$f_{win}(x,i)=1-\left[s(-i)-x\right]^2 \tag{8}$$

The state equation of the memristor is [15], [19]:

$$\frac{dx}{dt}=\left[\begin{array}{l}\left(k_1\cdot v^3+k_2\cdot v\right)\cdot\exp\left(\dfrac{v\cdot i}{\sigma_P}\right)\cdot\\ \exp\left(-\dfrac{x^2}{x_{ON}{}^2}\right)\cdot s(v)+\\ +A\cdot\sinh\left(\dfrac{v}{\sigma_{OFF}}\right)\cdot\exp\left(-\dfrac{x_{OFF}{}^2}{x^2}\right)\cdot\\ \exp\left(\dfrac{1}{1+\beta\cdot i\cdot v}\right)\cdot s(-v)\end{array}\right]\cdot f_{win}(x,i) \tag{9}$$

where k_1 and k_2 are tuning parameters. The current-voltage relationship of the Ta_2O_5 memristor element is [15], [19]:

$$i(x,v)=\left[G_{\max}\cdot x+\left(h_1\cdot v^4+h_2\cdot v^2+h_3\right)\cdot(1-x)\right]\cdot v \tag{10}$$

where the parameters for adjustment are: h_1 = 9.897.10^{-5}; h_2 = 0.0006531; h_3 = 2.88.10^{-5} [15], [19]. The applied model is fully described by (9) and (10) [15].

D. *Tuning the applied memristor model [15], [19]*

The modified model applied in the paper and described by (9) and (10) has several parameters for adjustment [15]. It is tuned according to experimental *i-v* characteristics by change the parameters till approaching a minimum of the RMS error [15, 17]. A procedure for extraction of the parameters is realized in MATLAB [24], [26], [27]. The derived model's coefficients are: k_1 = 0.0002359, k_2 = 0.0002121; h_1= 9.897.10^{-5}, h_2 = 0.0006531, h_3 = 2.88.10^{-5}, A = 1.05•10^{-10}, B = 0.98.10^{-4}, σ_p = 3.7•10^{-5}, σ_{off} = 1.9•10^{-2}, σ_{on} = 4.5•10^{-1}, G_{max} = 2.51•10^{-2}, x_{off} = 0.41, x_{on} = 6•10^{-2}, a = 7.2•10^{-6}, β = 523, b = 4.7, x_0 = 0.105, p = 5, m = 0.0001. Due to the simplifications in [15] its functioning is faster than the existing models.

E. *LTSPICE schematic of the improved memristor model*

LTSPICE [17] model of the considered memristor is created in accordance with the improved mathematical model (9) and (10). For realization of the respective mathematical operations, the standard functions in LTSPICE are used [19], [24], [25]. The equivalent schematic of the considered model is presented in Fig. 1 for clarification of its operation. The state variable x is expressed as a voltage drop across the capacitor C_1, which current is proportional to the time derivative of x. The memristor current is expressed by G_1 [15].

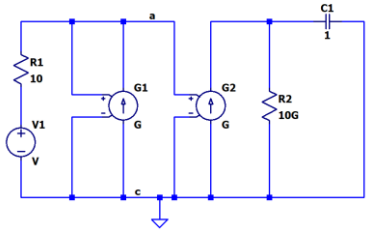

Fig. 1 An equivalent LTSPICE schematic of the considered model

The obtained LTSPICE memristor model is successfully analyzed for several sinusoidal voltage signals with different frequencies and amplitudes. The derived current-voltage relationships are presented in Fig. 2 to illustrate the correct functioning of the applied memristor model. Its proper operation is confirmed by the observed shrinking of the pinched *i-v* hysteresis loop with increasing the frequency of the voltage. The considered model is also analyzed for pulse voltage signals and convergence problems are not observed.

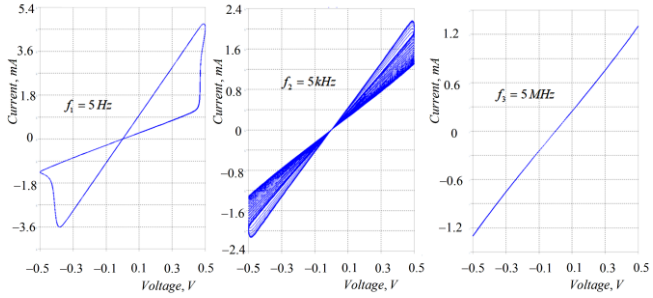

Fig. 2 Current-voltage relations of the memristor model for sinusoidal signals with different frequencies (5 Hz, 5 kHz, 5 MHz) and amplitude of 0.5 V

III. The Memristor-Based Synaptic Circuit and its LTSPICE Realization

The proposed synaptic scheme is presented in Fig. 3 for better understanding and explanation of its functioning [19]. It is based on a current divider and a differential amplifier with two MOS transistors – T_1 and T_2. The differential amplifier contains two branches, which are connected in parallel. The first branch contains a memristor element M and the resistor R_4. The second branch of the differential amplifier is made of two resistors, connected in series - R_1 and R_5. The flowing currents are denoted by i_1 and i_2, correspondingly. The input voltage signal is denoted by v_1. The voltage drops across the resistors R_4 and R_5 are proportional to the currents i_1 and i_2. They are denoted by v_2 and v_3, respectively:

$$v_2 = \frac{v_1}{M + R_4} R_4 \tag{11}$$

$$v_3 = \frac{v_1}{R_1 + R_5} R_5 \tag{12}$$

The output voltage signal of the synaptic device is denoted by v_4 and it is calculated as follows:

$$v_4 = k_v \cdot (v_2 - v_3) = k_v \cdot v_1 \cdot \left(\frac{R_4}{R_1 + R_4} - \frac{R_5}{M(x,v) + R_5} \right) \tag{13}$$

where k_v = 10 is the coefficient of voltage amplification of the considered differential amplifier. The values of the resistances are: R_1 = 300 Ω, R_4 = R_5 = 1 kΩ. The synaptic weight $w(M)$ of the considered circuit as a function of the memristance M is expressed as follows:

$$w(M) = \frac{v_4}{v_1} = k_v \cdot \left(\frac{R_4}{R_1 + R_4} - \frac{R_5}{M(x,v) + R_5} \right) \tag{14}$$

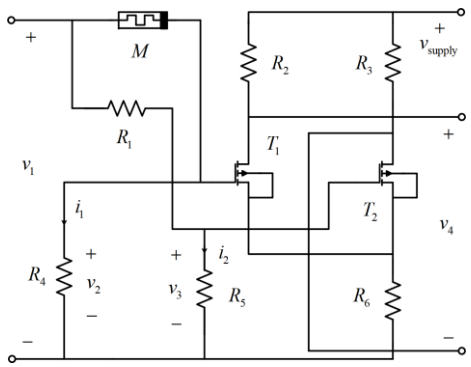

Fig. 3 A schematic of the considered memristor synapse

The memristance $M(x,v)$ is a function of the state variable x and the applied voltage v. It is expressed according to equation (9) of the applied memristor model [15], [19]:

$$M(x,v) = \frac{1}{G_{\max} \cdot x + \left(h_1 \cdot v^4 + h_2 \cdot v^2 + h_3 \right) \cdot (1 - x)} \tag{15}$$

The resistance of the memristor M and the corresponding synaptic weight w are changed by external voltage pulses and the corresponding alteration the memristor state variable x. After simple transformation of (14) and having in mind that $R_4 = R_5$, it is derived that if $R_1 = M$, then $w = 0$. Positive synaptic values are obtained when $M > R_1$. If $M < R_1$ then $w < 0$. By the change of the operating points of the MOS transistors and the respective coefficient of voltage amplification k_v it is possible to scale the synaptic weights. The resistors R_2 = 300 Ω and R_3 = 300 Ω are used for limitation the drain currents of the MOS transistors. The resistor R_6 is connected between the source electrodes of the transistors T_1 and T_2 and the ground. This resistor R_6 is used for realization of negative voltage feedback.

The LTSPICE netlist of the considered synaptic circuit is correspondent to the schematic presented in Fig. 3:

```
* LTSPICE code of the memristor synapse
XU1 N003 N005 N007 A10
R1 N004 N003 300
R2 0 N007 10G
V1 N003 0 PWL(0 0 1m 0.7 2m 0.7)
M1 N002 N004 N008 N008 Si4836DY
M3 N006 N005 N008 N008 Si4836DY
R3 N008 0 100
R4 N001 N002 200
R5 N001 N006 200
V2 N001 0 2
R6 N004 0 150
R7 N005 0 150
R8 N002 N006 10k
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\PC-Admin\Documents\LTspiceXVII\
lib\cmp\standard.mos
.tran 0 2 0 1u
.lib C:\Users\PC-Admin\Modified Memristor
Models\Modified model A10
.backanno
.end
```

IV. Tuning of the Memristor-Based Synapse

The memristor state and the corresponding weight are changed when external voltage pulses with a level higher than 0.15 V are applied to the synapse [12]. The alteration of synaptic weight Δw as a function of the memristance M is:

$$\Delta w(M) = k_v \cdot R_5 \left(\frac{1}{R_5 + M(x,v)} - \frac{1}{M(x,v) + \Delta M + R_5} \right) \tag{16}$$

where ΔM is the change of the memristance. If a voltage with a positive polarity is applied to the input of the synaptic circuit, then the memristance M decreases. This leads to increasing of the synaptic weight w. After the conducted analyses of the synapse, it was established that voltages lower than the threshold of 0.15 V do not affect the memristor state and the synaptic weight does not change. The weight adjustment by voltage pulses is presented in Fig. 4 a) and Fig. 4 b) for describing the tuning process of the synapse.

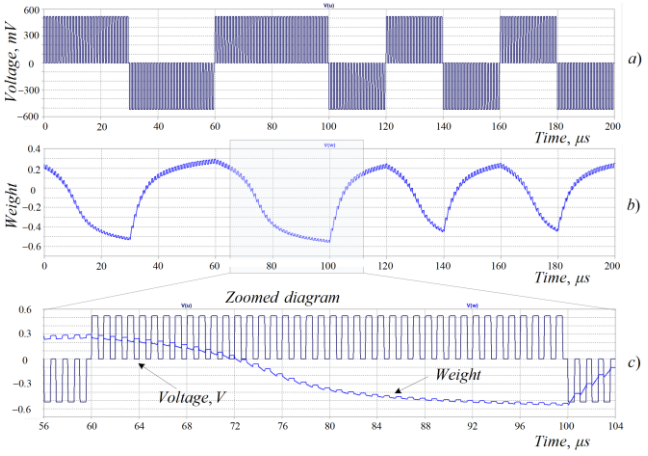

Fig. 4 a) Time diagram of the voltage v, applied to the synapse; b) diagram of the corresponding synaptic weight w, c) zoomed time diagrams of the voltage and the corresponding synaptic weight between 60 μs and 100 μs

The voltage signal shown in Fig. 4 a) is a sequence of packages of positive and negative pulses with an amplitude of 0.52 V. The duration of a pulse is 1 μs. A detailed diagram of the voltage and the weight are shown in Fig. 4 c). An applied pulse causes altering the synaptic weight by 0.02. The corresponding change of the state variable x is 0.021 and the respective alteration of the memristance M is about 6.2 Ω. When the needed change of the weight w is higher, then a package of impulses with the same polarity must be applied. Increasing the synaptic weight w and the respective decreasing of the state variable x are realized by a sequence of negative voltage pulses. The considered synapse is applied in a neural network for evaluation the risk factors for potential patients with COVID-19 illness [20]. The level of the input signals applied during the pauses is lower than 0.15 V, and the state variable of the memristors and the corresponding synaptic weights do not change. By decreasing of pulse level or its duration, the change of the weight is also decreased.

V. Conclusion

In the present work a modified synaptic circuit based on memristor is applied and analyzed. It is founded on a current divider and a differential amplifier with MOS transistors. The current divider contains a memristor element and a resistor. The LTSPICE code of the synapse is presented. An advantage of the proposed circuit is its ability to ensure positive, zero and negative synaptic weights. Another advantage of the offered synaptic device is the minimal number of memristors per synapse. The considered synaptic scheme is successfully analyzed, using an improved model of the applied tantalum oxide memristor. It is successfully applied in a neural network for evaluation several risk factors affecting potential patients with COVID-19 syndrome. The conducted analyses confirm the proper operation of the applied memristor model and the memristor-based synapse.

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