Simulation of 1T DRAM Memory Cell with Verilog-A Model of CNTFET in Cadence

Mariya Lyubomirova Spasova, George Vasilev Angelov and Marin Hristov Hristov

Abstract - **Carbon nanotubes are promising materials for the nanoscale memory devices. A Verilog-A formulation of the Stanford compact model for CNTFET is used for simulation of 1T DRAM cell in Cadence Spectre circuit simulator. Read and write operations of the 1T DRAM circuit with CNTFET are compared to the memory circuit with standard nmos4 transistor from 0.35 μm CMOS design kit of AMS. The analysis showed that CNTFET is applicable to 1T DRAM memory cell and CNTFET memory cell has better performance compared to the standard MOSFET.**

Keywords – **Carbon nanotubes, CNTFET, 1T DRAM, compact model, circuit simulation.**

I. INTRODUCTION

The state-of-the-art high density integrated circuits are based on the bulk CMOS (complimentary metal-oxide-semiconductor) technology and the classic MOSFET. Technology progress and device scaling have driven semiconductor devices into nanometer scale of dimensions. This implies unwanted physical effects such as leakage currents, tunneling, etc. i.e. arises the need for introducing new devices that could follow the Moore's law overcoming the physical limits of the conventional MOS transistor [1].

Dynamic RAMs are important class of semiconductor devices based on the MOSFET with huge range of applications to all computational devices. DRAM integrated circuits also obey the Moore's law and thus, there is an urgent need of new materials to address the problems related to higher data storage, smaller sizes, higher density of integration, lower power consumption, higher reliability, faster performance, etc. And all these requirements have to be met at a low cost.

One very important aspect of device scaling is the extremely reduced oxide thickness of MOSFETs. A prospective solution to this issue is the use of electronic devices with channels made of a single carbon nanotube or a semiconductor nanowire. Carbon nanotubes are sheets of graphite layers (grapheme, a semi-metal) rolled into a tube [2]. Depending on the way the sheet is rolled up (its chirality) the CNT may be metallic or semiconducting. Interest in carbon nanotubes is driven by their electronic, optical, thermal, and mechanical properties [2], [3].

There are several types of alternatives to the conventional SiO_2 used to overcome this problem: carbon nanotube (CNT) transistors [4], Silicon (Si) nanowire transistors [5], Gallium Antimonide (GaSb) nanowire transistors [6], Gallium Nitride (GN) nano-field effect transistors [7], Zinc oxide (ZnO) nanowire transistor [8], FinFET [9].

As one of the most important nanomaterials with excellent mechanical and electronic properties, carbon nanotube has been explored for various memory applications. The first Carbon NanoTube Field-Effect Transistor (CNTFET) was reported in 1998 [4], [10]. Since then the progress of CNTFET technology and the understanding of its device physics has been very quick [11].

Carbon nanotubes are form of carbon that can be considered as the result of folding graphite layers into carbon cylinders and may be composed of single shell–single wall nanotubes (SWNTs), or of several shells – multi-wall nanotubes (MWNTs). Depending on the folding angle and the diameter, nanotubes can be metallic or semiconducting. Simple theory predicts that the band gap of semiconducting nanotubes decreases with increasing diameter. These predictions have been verified in recent scanning tunneling spectroscopy experiments [4], [12].

Recent experimental and theoretical studies have shown that the CNTFET device can outperform state-of-the-art silicon MOSFET in many ways [3], [10], [13], [14]. It has been listed in the International Technology Roadmap of Semiconductors as an emerging candidate succeeding silicon CMOS device [11]. The tremendous developments in CNTFETs promise that there will soon be implemented an alternative material to replace silicon in conventional microelectronics.

Concerning memory applications, a simple CNTFET can work as a memory device through storing charges in SiO_2. The detailed charge injection process, however, is still not well studied [15]. This causes uncertainty on the reliability and the retention capability of the device because the SiO_2 itself works as both tunneling barrier and storage media in such device and the trap density determines both the charge density and the leakage current.

In the non-volatile memory application, however, it is not a straight forward solution to simply replacing silicon MOSFET with CNTFET in a Flash cell without a significant change of the cell structure [15]. Unlike the FinFET [16], whose channel is still considered bulky comparing with a CNT channel, the bulk floating gate in the present flash cell structure seems unlikely to be able to pull out the full advantage of the CNTFET considering the electrostatic coupling and the charge injection efficiency.

In the present paper we focus on application of CNTFET model to volatile memories. We simulate a CNTFET in one transistor (1T) DRAM memory circuit using a Verilog-A formulation of the Stanford CNTFET model [17]. The Verilog-A code is implemented in Cadence Spectre circuit simulator as an external model. Simulation results concerning CNTFET are compared to the results simulated

M. Spasova is PhD student at ECAD Laboratory, Technical University of Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: mls@ecad.tu-sofia.bg

G. Angelov, PhD, is asst. professor with the Dept of Microelectronics FETT, TU–Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: gva@ecad.tu-sofia.bg

M. Hristov is professor with the Dept. of Microelectronics, FETT, Technical University of Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: mhristov@ecad.tu-sofia.bg

for the standard NMOS transistor in the 0.35 mm AMS CMOS technology design kit.

II. CIRCUIT DESCRIPTION AND SIMULATIONS

The compact model of the CNTFET developed by the Nanotechnology/Nanoelectronics Group at Stanford University describes enhancement mode MOSFET with semiconducting single wall carbon nanotube as channel. The model is based on a quasi-ballistic transport assumption and accounts for the capacitor network in a CNFET. Each device may have one or more carbon nanotubes and the effects of channel length scaling can be accurately modeled down to 20nm [18], [19].

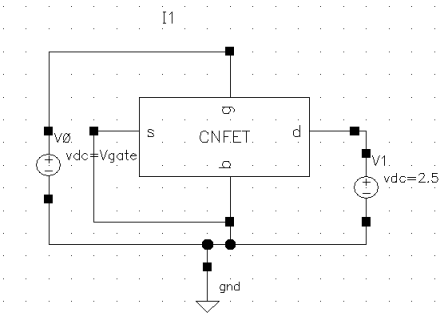


FIGURE 1. CNTFET OUTPUT *I-V* CHARACTERISTIC.

Figures 2 and 3 present the *I–V* characteristics of the standard nmos4 transistor within AMS 0.35 µm design kit and the CNTFET transistor, respectively.

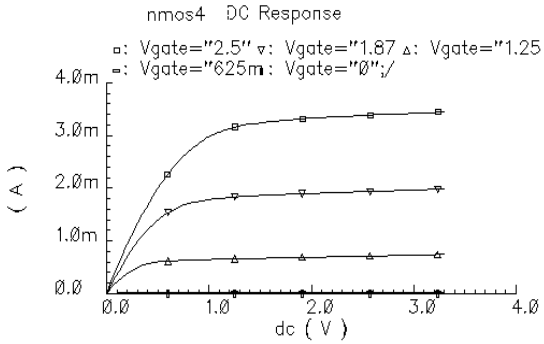


FIGURE 2. IDS(VDS) AT VGS = 0, 0.625, 1.25, 1.87 AND 2.500 V; VBS = 0 V; L = 0.35 µM W = 10 µM NMOS4 MODEL TO CADENCE LIBRARY.

Since our design kit is for 0.35 mm CMOS technology, when we set submicron dimensions to both standard design kit nms4 transistor and the CNTFET transistor, we obtain unrealistic results. This is due to model limitations: in the Stanford CNTEFT compact model the channel length should be between (10-100 nm); there are no limitations to channel width.

Figures 4 present the transfer *I-V* characteristics of the standard nmos4 transistor and the CNTFET, respectively. Both characteristics match almost perfectly to each other between 1 V and 2 V. The Stanford CNTFET compact model has higher transfer characteristics in the range between 0 V to 1 V and 2 V to 3 V.

Transconductance is a fundamental parameter characterizing MOSFET amplifier properties. It is defined by the following expression:

$$S = \Delta I_D / \Delta V_{GS} \quad \text{at} \quad V_{DS} = \text{const} \tag{1}$$

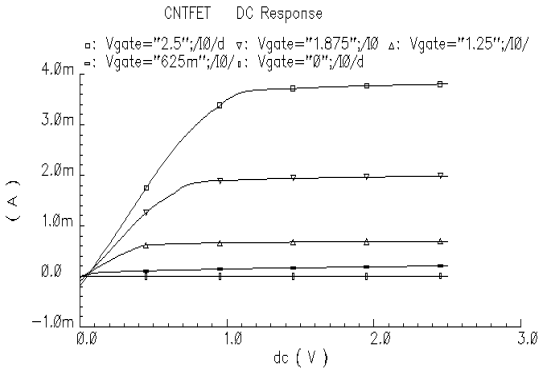


FIGURE 3. IDS(VDS) AT VGS = 0, 0.625, 1.25, 1.87 AND 2.500 V; VBS = 0 V; L = 14 NM W = 0.1 µM FOR CNTFET.

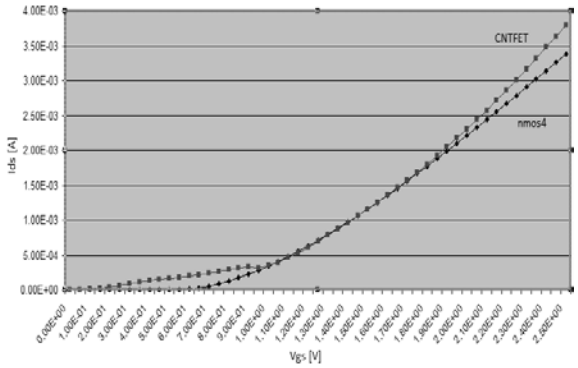


FIGURE 4. I_{DS} (V_{GS}) AT V_{DS} = 2.5 V; V_{BS} = 0 V; L = 14 NM W = 0.1 µm FOR CNTFET COMPACT MODEL AND L = 0.35 µm W = 10 µm FOR NMOS4 MODEL FROM CADEBCE LIBRARY.

Figure 5 shows the transconductance characteristics of the two transistors. For the Stanford CNTFET the transconductance has greater value in the range between 0 V – 0.7 V and 1.3 V do 3 V. In the range between 1.2 V – 1.3 V the characteristics of both MOS transistors match to each other. Transconductance of Stanford CNTFET compact model is less in the range from 0.7 V – 1.2 V.

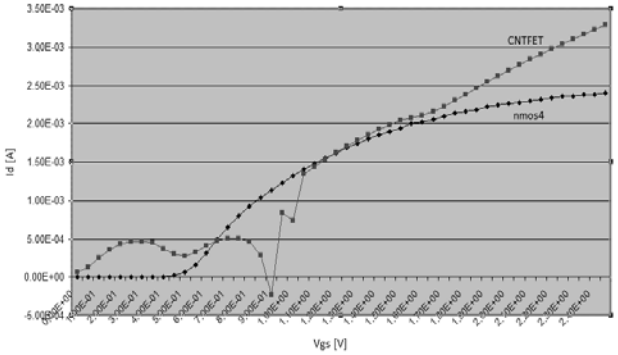


FIGURE 5. TRANSCONDUCTANCE OF BOTH MODELS AT I_{DS} (V_{GS}) AT V_{DS} = 2.5 V; V_{BS} = 0 V; L = 14 nm W = 0.1 µm FOR CNTFET COMPACT MODEL AND L = 0.35 µm W = 10 µm FOR NMOS4 MODEL FROM CADENCE LIBRARY.

Figure 6 shows 1T DRAM cell memory circuit with Stanford CNTFET compact model. In our previous paper [20] we made simulations with the same memory cell, using high-*k* capacitor. Now we replace the standard transistor in the memory cell with CNTFET transistor to compare the results.

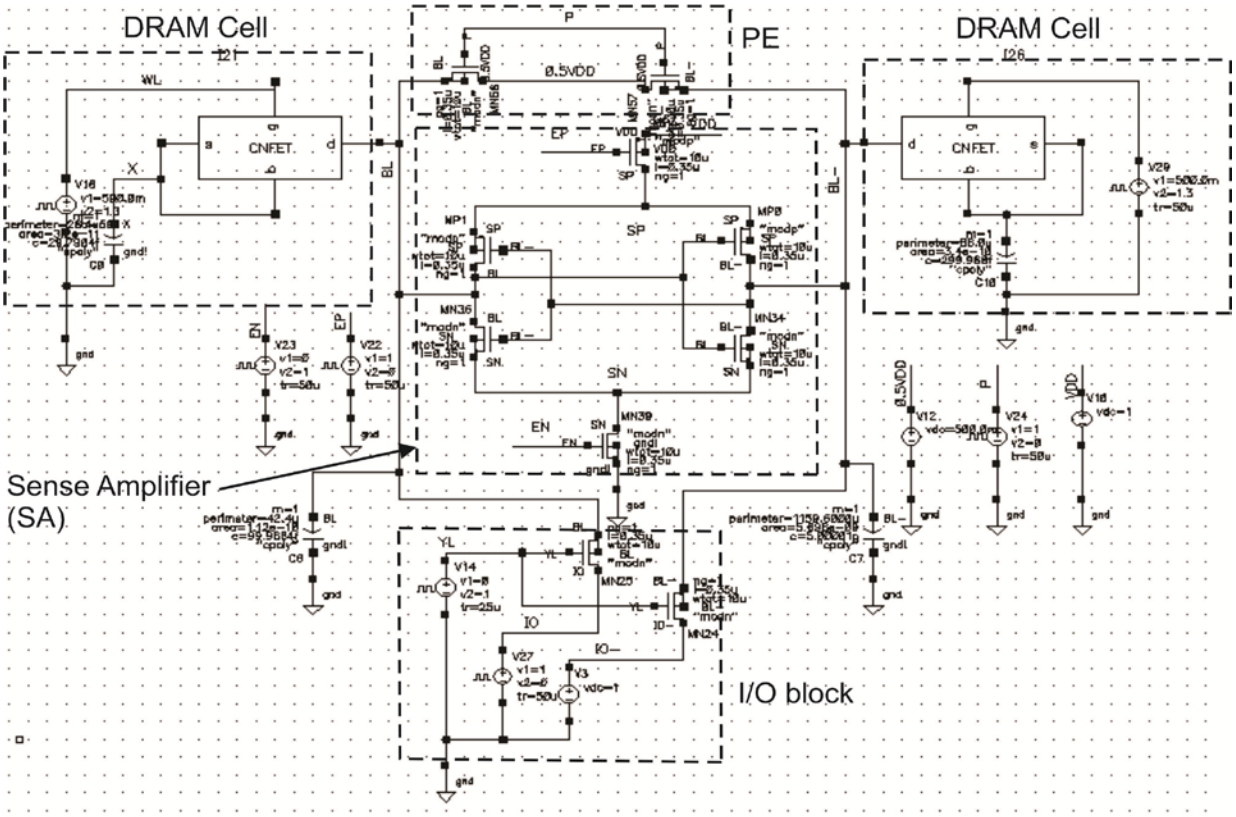
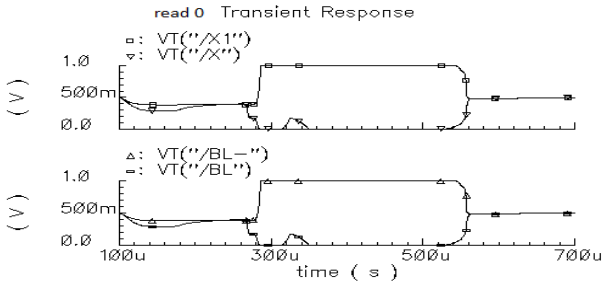
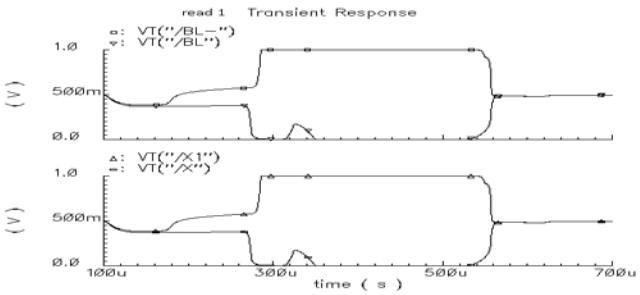


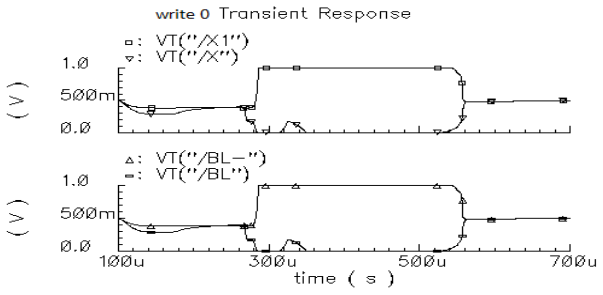
FIGURE 6. DRAM ARRAY AND DATA LINE CONFIGURATION WITH CNTFET.



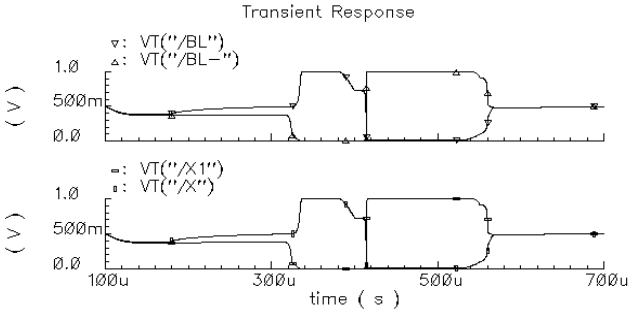
A) OPERATION READ OF 0 WITH CNTFET TRANSISTOR.



B) OPERATION READ OF 1 WITH CNTFET TRANSISTOR



C) OPERATION WRITE OF 0 WITH CNTFET TRANSISTOR.



D) OPERATION WRITE OF 1 WITH CNTFET TRANSISTOR

FIGURE 7. THE READ/WRITE OPERATIONS OF THE WITH CNTFET TRANSISTOR

On Figure 7 voltage sources V22 and V23 (Fig. 6) are turned ON; Sense Amplifier (SA) has applied voltage of 0 V and 1 V. Voltage source V24 with a voltage 0 V и 1 V is applied to PE. Voltage sources V14, V24, V3 are applied to the I/O block with a voltage 0 V и 1 V.

Figure 7a), operation "read of 0". The voltage defined on data lines (WL and WL1) by voltage sources V18 and V20 is between 0.5 V ÷ 1 V. Capacitances of the two cell capacitors are as follows C_0 = 30 fF, C_{10} = 90 fF. The voltage defined on data lines (BL and BL-) are C_6 = 100 fF

and C_7 = 5 pF.

Figure 7b), operation "read of 1". The voltage on WL defined by voltage source V18 is WL = 0.5 V ÷ 1V. The voltage on WL1 defined by sources of voltage V20 is 0.5 V ÷ 1.3 V. Capacitances of the two cell capacitors are C_0 = 90 fF, C_{10} = 500 fF. Capacitances of the capacitors on data line (BL и BL-) are C_6 = 3 pF и C_7 = 5 pF.

The parameters of the memory cell with the nmos4 transistor are as follows: capacitance of the capacitors in cells C_1= 300 fF, C_2 = 90 fF for "read of 0" operation and C_1 = 90 fF, C_2 = 300 fF for "read of 1" operation. Capacitances of the capacitors on data line are CBL1 = 30 fF, CBL2 = 5 pF for "read of 0" operation and CBL1 = 3 pF and CBL2 = 5 pF for "read of 1" operation. The other transistors parameters used in the simulation circuit are listed in Table 1.

TABLE 1. PARAMETERS FOR COMPARISON OF TRANSISTORS

Transistor	Type of channel	Layer width	Layer length
nmos4	Si	10 µm	0.35 µm
CNTFET	CNT	0.1 µm	14 nm

Figure 7c), operation "write of 0". The voltage on data lines (WL and WL1) defined by voltage sources V18 and V20 is between 0.5V ÷ 1.3V. Capacitances of the two cell capacitors are C_0 = 30 fF, C_{10} = 300 fF. Capacitances of the capacitors on data line BL and BL– are C_6 = 100 fF and C_7 = 5 pF.

Figure 7d), operation "write of 1". The voltage on WL defined by voltage source V18 is between WL = 0.5 V ÷ 1.2 V. The voltage on WL1 defined by voltage source V20 is 0.5 V ÷ 1 V. Capacitances of the two cell capacitors are C_0 = 50 fF, C_{10} = 300 fF. Capacitances of the capacitors on data line BL and BL– are C_6 = 5 pF and C_7 = 3 pF.

From the simulations presented in Figure 7, we can see the benefits of using the CNTFET in Dynamic RAM cell. The circuit has small sized transistor (the dimensions are in Table 1), the transistor operates at lower voltages (for the CNTFET, on WL and WL1 are applied voltages between 0.5 V ÷ 1.3 V while for the standard nmos4 transistor the applied voltages vary between 0 V ÷ 2.2 V).

III. CONCLUSION

Standard 1T DRAM cell circuit was simulated in Cadence Spectre simulator using 1) standard nmos4 transistor with SiO_2 gate dielectric from AMS 0.35 µm design kit and using 2) single-wall CNTFET transistor implemented as an external Verilog-A model. The simulated output and transfer *I-V* characteristics, transconductance, and read and write operations of the memory cell showed better performance of the CNTEFET cell compared to the standard nmos4 memory cell.

The use of CNTFET transistor in a 1T DRAM cell proved to be applicable to memory circuits.

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