STUDY OF THE ELECTRICAL PROPERTIES OF CNTFETS BASED ON COMPUTER SIMULATIONS

Angel Pashev, Dobromir Gaydazhiev, George Angelov, Ivan Uzunov

Abstract – **The paper reviews two approximations for energy level calculation based on the tight-binding model. Basic static and dynamic characteristics of CNTFET with doped source/drain area are performed using the Stanford University CNTFET model. The dependence of the output characteristics from the device geometry is given. An estimation of the transit frequency shows that the device can operate in the multi-GHz range.**

Keywords – **Carbon nanotubes (CNT), graphene, CNTFET, device modeling, tight-binding model.**

INTRODUCTION

The physical limit of the CMOS technology scaling is expected to be reached in the next 5-10 years. Increasingly more efforts are targeted at development of alternative electronic devices, to allow further frequency increase and power consumption reduction in the semiconductor technologies that will follow the 7 nm node [1]. Among the most promising novel devices are carbon based transistors in which graphene or carbon nanotubes (CNT) are used to form the channel region. Different types of carbon electronic devices have been reported in the literature – back-gate or top-gate graphene FETs, CNTFET using Schottky barrier formed at the CNT - Drain/Source metal contact interface [2], top-gate CNTFET with doped D/S area and others [3]. Those devices benefit from the extremely high electron mobility and nearly ballistic transport to achieve very high speed and low power consumption, but still pose technological challenges that have to be overcome before they can move out of the laboratories into the production plants. The main technology issues are related to overcoming the high contact resistance at the interface between the carbon and most metals, selective removal of conducting CNTs and achieving good on/off current ratio.

In this paper an overview of the CNTFET devices and their models is presented. The models are used to analyze the basic static and dynamic characteristics of CNTFETs with doped source and drain regions (Fig.1). This structure is very similar to the planar CMOS FETs, thus it is possible to use many of the existing semiconductor processes in the device production. It inherits all the advantages of CNT electrical properties and has good on/off ratio [4], but also suffers from some of the common issues – high contact resistance and the need to selectively remove the conducting CNTs.

Most of the results reported here are obtained by simulations using the Verilog-A implementation of the Stanford University CNFET model reported in [5] and [6] or by theoretical analysis and custom Matlab code for calculations. The molecule structure, energy levels and other electrical properties of the carbon nanotubes are reviewed in the first section of the paper. The second section investigates the static characteristics of the CNTFET from Fig. 1 and their dependence on the CNT geometry. The influence of the different parasitic capacitances on the device speed is analyzed in the third section.

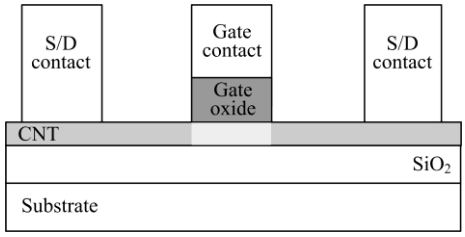

FIG. 1 CROSS-SECTION OF CNTFET WITH DOPED SOURCE AND DRAIN AREAS. THE DOPED S/D REGIONS OF THE CNT ARE MARKED WITH DARKER GRAY AND THE INTRINSIC CHANNEL IS WITH LIGHTER GRAY.

I. MODELING OF ELECTRICAL PROPERTIES OF CARBON NANOTUBES

Electrical behavior of the carbon nanotubes can be explained by reviewing the atomic structure and energy diagram of graphene –its building material. In essence, graphene is a single layer of graphite. It is a single atomic layer crystalline carbon with a hexagonal atomic lattice. The crystal lattice of this material and its Brillouin zone are shown in Fig. 2 (a) and (b) respectively. The valence and conducting bands of graphene touch at 6 points (marked with black dots on Fig. 2 (b)) throughout its Brillouin zone, zeroing the bandgap. In all other points, there is a gap between the energy bands. This defines graphene as a *"zero-bandgap"* semiconductor [7]. It has very high electron mobility which may exceed 15000 cm^2/Vs. In comparison, the electron mobility of silicon at room temperature is around 1400 cm^2/Vs [8].

Carbon nanotube is actually a hollow cylinder made of rolled up piece of graphene. The tube may have very different electrical properties depending on the angle at which the piece of graphene that makes it up is "cut". This angle is described by the chirality vector *C(n,m)*, illustrated on Fig. 2 (a). In a planar sheet, the three carbon-carbon (C-C) covalent bonds for each atom are at 120° of each other. When a tube is rolled up, the angles between the bonds change, which leads to change in the allowed energy levels. The energy structure of a CNT is obtained by quantizing

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the energy structure of graphene (Fig. 2 (b)). The quantized levels can be expressed theoretically using the tight-binding model [7]:

$$E(k) = \pm\gamma\left[1+4\cos\left(\frac{3C_x ka}{2C}-\frac{3\pi paC_y}{C^2}\right)\cos\left(\frac{\sqrt{3}C_y ka}{2C}+\frac{\sqrt{3}\pi paC_x}{C^2}\right)+4\cos^2\left(\frac{\sqrt{3}C_y ka}{2C}+\frac{\sqrt{3}\pi paCx}{C^2}\right)\right]^{1/2} \quad (1)$$

where k is the wave vector in the axial direction, p is the quantized wavevector in circumferential direction, $\gamma \approx 3.03$eV is the C-C covalent bond energy, $C_x = a(\sqrt{3}n + (\sqrt{3}/2)m)$, $C_y = a(3/2)m$ and the length of the covalent C-C bond a=0.142 nm.

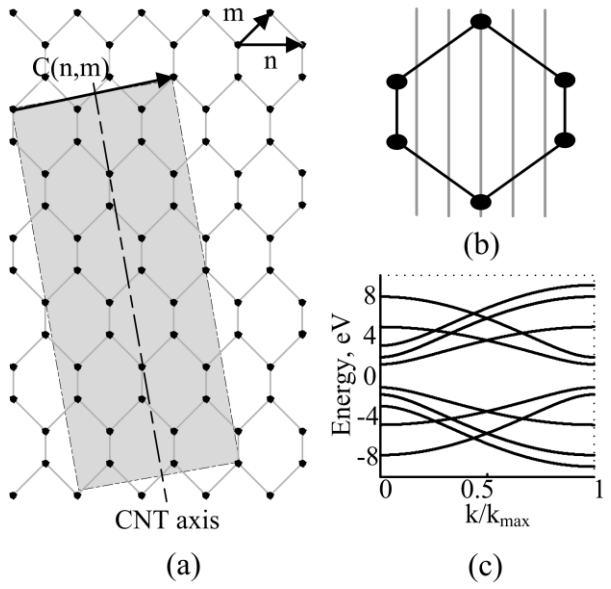

FIG. 2 (A) CARBON NANOTUBE WITH CHIRALITY VECTOR *C*(2,1) OVERLAID ON GRAPHENE ATOMIC LATTICE; (B) GRAPHENE BRILLOUIN ZONE AND CNT DISCRETIZATION LINES; (C) ENERGY LEVELS OF A *C*(5,0) CNT CALCULATED BY THE TIGHT-BINDING MODEL APPROXIMATION.

The chiralities for which the quantization lines pass through the zero bandgap points of graphene yield conducting (metallic) CNTs. When the quantization lines do not pass through the zero bandgap points – the tubes are semiconducting. A CNTFET has to have only semiconducting tubes to achieve good on/off current ratio. In this article only FETs with semiconducting nanotubes are analyzed.

Expression (1) is used to create Matlab code calculating the energy levels and bandgap values of carbon nanotubes with different chiralities. A sample energy diagram for CNT with *C*(5,0) is shown in Fig. 2 (c). This is a semiconducting tube with energy gap between the highest valence and lowest conduction level of ~2.29 eV. This model can be used to calculate the energy levels of any CNT with high accuracy, but this approach is calculation intensive. If applied to simulate the behavior of larger CNTFET circuits, it will require a lot of processing power and the analysis runtimes will increase proportionally to the circuit complexity. For this reason a simplified approximation of the tight-binding model has to be used for circuit simulators targeted at larger circuits, i.e. Stanford CNTFET model [5], [6], PTM model [8]. Apart from precisely modeling the energy levels of the CNT, a number of other effects have to be taken into account to achieve accurate device model – scattering mechanisms in the intrinsic channel and S/D areas, band to band tunneling, Schottky resistance on the CNT-metal contact interface, parasitic capacitances etc.

A Verilog-A implementation of the model developed by Stanford University [5], [6] is used in this paper to analyze the static and dynamic characteristics of CNTFETs with different chiralities. The model includes the effects mentioned above and is computationally optimized to allow simulation of large circuits. It uses an approximation of the tight-binding model. The diameter of the tube is calculated by the following formula:

$$d = \frac{\sqrt{3}a}{\pi}\sqrt{n^2+nm+m^2}\,, \quad (2)$$

where a = 1.42 Å is the length of C-C covalent bond and C(n,m) is the chirality vector.

In order to calculate the energy levels the CNT is quantized in its circumferential and axial directions. The energy levels are calculated by the following approximation [5], [6].

$$k_p = \frac{2\pi}{a\sqrt{n^2+nm+m^2}}\lambda\,, \quad (3)$$

$$k_l = \frac{2\pi}{L_g}l \;,\; l = 1, 2, 3\ldots\,, \quad (4)$$

$$E_{p,l} \approx \frac{\sqrt{3}}{2}aV_\pi\sqrt{k^2{}_p + k^2{}_l}\,, \quad (5)$$

where k_p and k_l are the quantized levels in axial and circumferential directions respectively. The parameter λ is equal to the index p for metallic and to $(6p\text{-}3\text{-}(-1)^p)$ for semiconducting tubes, L_g is the gate length and V_π = 3.033eV is the C-C covalent bond energy.

II. DC CHARACTERISTICS OF CNTFETS WITH DIFFERENT CHIRALITIES

The model uses only the first two k_p and ten k_l values, since for voltages up to 1 V for typical devices (d < 3 nm, L_g <100 nm), only these values have significant effect on the current [5], [6]. From (3) and (5) it is obvious that tubes with equal diameter yield identical energy levels. In reality, there are tubes with different chirality and equal diameters that have different energy levels and energy gap (E_g). For example if (1) is used to calculate the energy gaps of tubes with chirality *C*(5,3) and *C*(7,0), which have equal diameters of 0.548 *nm*, the result is respectively 1.566 eV and 1.482 eV. But equation (5) will result in energy gap of 1.556 eV for both tubes. Evidently, the simpler expression (5) should be used in cases where moderate accuracy is needed, while (1) is for the cases when high precision is needed.

The Stanford model is used to simulate the input and output characteristic of the CNT transistor from Fig. 1. To be able to compare the CNTFET performance to planar MOSFETs, the geometry of the transistor in all simulations is taken to be similar to the geometry of the modern planar MOSFETs – gate length L_g = 32 nm, gate oxide thickness t_{ox} = 4 nm, gate oxide permittivity ε_{ox} = 15. CNTFETs with single nanotube under the gate are used for the sake of simplicity. The channel resistance is governed primarily by the diameter and the number of CNTs, so the gate width is

not a crucial parameter for the static behavior of this transistor. However, it defines the gate parasitic capacitances and will be taken into account when reviewing the dynamic behavior in the next section of the article.

The output characteristics of two transistors with different chiralities are compared in Fig. 3. They closely resemble the output characteristics of a planar MOSFET, despite the fact that the physical principles defining both regions of the characteristic (linear and saturation) are different. The chirality vector defines the nanotube circumference and in practice, it is equivalent to the channel width of planar MOSFETs, defining the channel resistance and the maximum current that can flow through the tube. This is illustrated in Fig. 4, where the drain currents of tubes with different chiralities are compared. In fact, the dependence of the drain current from the CNT circumference, respectively CNT diameter, is approximately linear for constant gate voltages (Fig. 5). These dependencies are numerically illustrated in Table 1 where the bandgap values are also given.

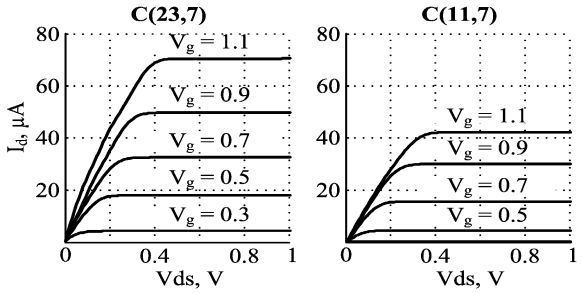

FIG. 3 FAMILY OF OUTPUT CHARACTERISTICS OF CNTFETS WITH C(23,7) AND C(11,7).

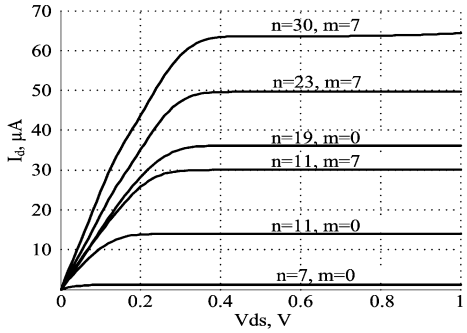

FIG. 4 OUTPUT CHARACTERISTICS OF CNTFETS WITH DIFFERENT CHIRALITIES AT V_{GS} = 0.9 V.

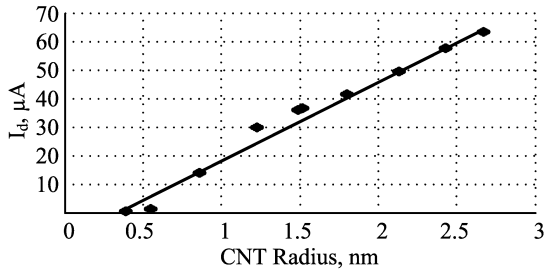

FIG. 5 THE DEPENDENCE OF THE DRAIN CURRENT FROM THE CNT DIAMETER. THE DRAIN CURRENT IS AT V_{GS}=0.9 AND V_{DS}=0.6.

Table 1 also shows that the energy gap decreases with the increase of CNT diameter. This is explained by the fact that when increasing the diameter the tube gets more atoms and hence gets more available energy levels. Statistically there is a bigger chance to have closer energy levels, resulting in lower energy gap. This is confirmed also by the transfer characteristics in Fig. 6. The lower energy gap results in lower threshold voltage V_{th} at fixed V_{gs} and V_{ds}, which leads to higher drain currents.

TABLE 1. CNTFET STATIC PARAMETERS FOR DIFFERENT CHIRALITIES. THE DRAIN CURRENT IS AT V_{GS}=0.9 AND V_{DS}=0.6.

Chirality		Diameter, nm	Current, μA	Eg, eV
n	m			
5	0	0.392	0.470	2.292
7	0	0.548	1.257	1.482
11	0	0.861	13.965	1.015
11	7	1.231	30.036	0.686
19	0	1.488	36.137	0.563
15	7	1.524	36.750	0.563
23	0	1.801	41.660	0.479
23	7	2.129	49.650	0.397
27	7	2.435	57.900	0.353
30	7	2.666	63.639	0.322

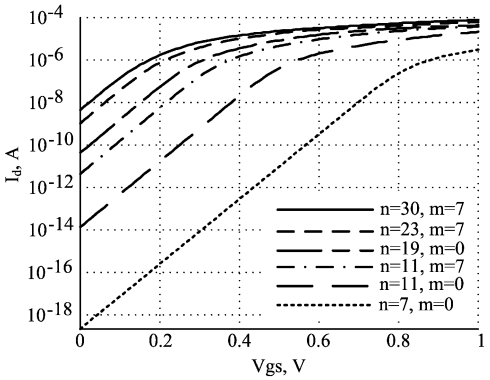

FIG. 6 TRANSFER CHARACTERISTICS OF CNTFETS WITH DIFFERENT CHIRALITIES AT V_{DS} = 0.9V

III. STUDYING OF THE DYNAMIC CNTFET PROPERTIES

Two basic factors determine the dynamic performance of the transistor – the intrinsic channel propagation time and the delay caused by the parasitic capacitances. The channel propagation delay is basically defined by the carrier mobility. The parasitic capacitances are illustrated in Fig. 7 and they are as follows: $C_{g\text{-}CNT}$ is the intrinsic gate to channel capacitance, $C_{g\text{-}sd}$ are the parasitic capacitances from the gate contact to the dopes source/drain area, $C_{g\text{-}sub}$ is the capacitance between the gate and substrate (back-gate), $C_{CNT\text{-}sub}$ is from the CNT to substrate and $C_{g\text{-}cont}$ represents the capacitances between the gate and source/drain contacts.

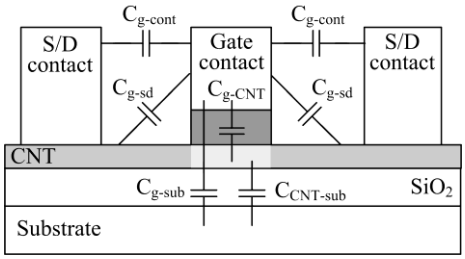

FIG. 7 PARASITIC CAPACITANCES AFFECTING THE CNTFET

DYNAMIC PERFORMANCE.

The dynamic properties are studied by a frequently employed approach of simulating a waveform of an inverter-type ring oscillator (RO). The RO inverters are using identical N-type and P-type CNTFETs with L_g = 32 nm, t_{ox} = 4 nm, ε_{ox} = 15, gate width w = 48 nm, gate height h = 64 nm and single CNT with C(19,0). The capacitance values are: $C_{g\text{-}CNT}$ = 4 aF, $C_{g\text{-}sd}$ = 2 aF, $C_{g\text{-}sub}$= 1.4 aF, $C_{g\text{-}cont}$ = 15 aF. Since the SiO_2 layer is assumed to be 10 μm and the tube diameter is small, the $C_{CNT\text{-}sub}$ capacitance becomes less that 0.5 aF and can be neglected. Those values are given in [10] as typical for CNTFET with the geometry size listed above.

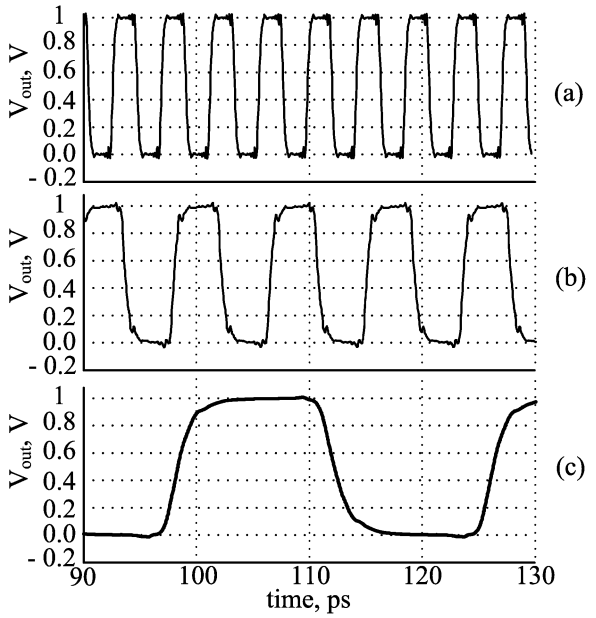

FIG. 8 TRANSIENT RESPONSE OF 7-STAGE RING OSCILLATOR CIRCUIT USING CNTFETS. (A) WITHOUT ANY PARASITIC CAPACITANCES, (B) $C_{G\text{-}SUB}$ AND $C_{G\text{-}SD}$ ARE ADDED, (C) ALL PARASITIC CAPACITANCES FROM FIG. 7 ARE ACCOUNTED FOR.

The output waveform is simulated at three different conditions: Fig. 8 (a) shows the effect only of the channel propagation delay; Fig. 8 (b) includes also the effects of $C_{g\text{-}sub}$ and $C_{g\text{-}sd}$; Fig. 8 (c) includes all parasitic capacitances. The parameters of the waveform (period and frequency of oscillation and delay of a single inverter stage) are summarized in Table 2. The first waveform actually gives the theoretical limit of the device. The extremely high carrier mobility results in a very high transit frequency of 1.61 THz (1/stage delay). It is reduced to 820 GHz by $C_{g\text{-}sub}$ and $C_{g\text{-}sd}$ and further to 251 GHz when the effect of $C_{g\text{-}cont}$ is taken into account. Even after including the parasitic capacitances, the transit frequencies are still impressive and demonstrate the big potential of those devices.

TABLE 2. RING OSCILLATOR DYNAMIC PERFORMANCE SUMMARY.

Waveform	Period, ps	Freq, GHz	Stage delay, ps
Fig. 8 (a)	4.32	231.71	0.62
Fig. 8 (b)	8.54	117,05	1.22
Fig. 8 (c)	27,96	35,76	3.99

CONCLUSION

Some basic properties of the CNTFET devices are investigated by simulations and theoretical analysis. The calculation of the energy bands based on the tight-binding model is discussed and two different approximations are examined. The dependence of the energy levels from the geometry of the nanotubes is reviewed. The parallel between the static characteristics of CNTFETs and planar CMOS transistors is articulated and their similarity is noted. The dependence of those characteristics on device geometry is investigated. Time domain simulation gives an estimation of the dynamic properties of the CNTFET and confirms its suitability for multi-GHz operation.

ACKNOWLEDGEMENT

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REFERENCES

[1] *International Technology Roadmap for Semiconductors: 2011 Edition Executive Summary*, 2011

[2] H.-S. P. Wong, D. Akinwande, *Carbon Nanotube and Graphene Device Physics*, Cambridge University Press, 2011.

[3] Spasova, M.L., G.V. Angelov, M. H. Hristov, Overview of Nanowire Field Effect Transistors, *International conference on Engineering, Technologies and System (TECHSYS 2013)*, Plovdiv, Bulgaria, May 29-31, 2013, Book 2, Vol. 19, pp. 161-166, ISSN 1310-8271.

[4] Ph. Avouris, M. Radosavljevic, Sh. J. Wind, *Carbon Nanotube Electronics and Optoelectronics*, Material Research Society Bulletin, Volume 29, Issue 06, pp. 403-410, June 2004.

[5] J. Deng, H.-S.P. Wong, *A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part I: Model of the Intrinsic Channel Region*, IEEE Transactions on Electronic Devices, Vol. 54, Issue 12, pp. 3186 – 3194, .2007

[6] J. Deng, H.-S.P. Wong, *A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part II: Full Device Model and Circuit Performance Benchmarking*, IEEE Transactions on Electronic Devices, Vol. 54, Issue 12, pp. 3195 – 3205, 2007

[7] M. P. Anantram, F. Leonard, *Physics of carbon nanotube electronic devices,* Reports on Progress in Physics 69.3, 2006.

[8] http://en.wikipedia.org/wiki/Electron_mobility#Doping_concentration_dependence_in_heavily-doped_silicon

[9] http://ptm.asu.edu/

[10] N. Patil, et al., *Circuit-level performance benchmarking and scalability analysis of carbon nanotube transistor circuit.* IEEE Transactions on Nanotechnology, Vol 8.1, pp. 37-45, 2009.