Surface Potential Model of a High-*k* HfO_2-Ta_2O_5 Capacitor

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Abstract — **A compact model of a MOS capacitor with high-*k* HfO_2–Ta_2O_5 mixed layer stack is developed in Matlab. Model equations are based on the surface potential description of PSP model. After fitting the *C–V* characteristics in Matlab the model is coded in Verilog-A hardware description language to interface with Spectre circuit simulator within Cadence CAD system. The results are validated against experimental measurements of high-*k* dielectric structure.**

Index Terms — **Device modeling, compact models, PSP, circuit simulation, high-*k* gate dielectric, Verilog-A, Spectre.**

I. Introduction

The semiconductors industry has been facing new challenges due to CMOS device downsizing. Linear scaling will not be possible in the future unless new materials are introduced in CMOS device structures or unless new device architectures are implemented. The strong association between devices and materials research is the key enabler here. The demand for low voltage, low power and high performance are the great challenges for the engineering of sub 45-nm gate length CMOS devices.

In this context device modeling is the milestone to efficiently implementing design objectives based on the new devices [1]. The scaling of classical bulk Si CMOS transistors approaches its physical limits. The SiO_2 gate dielectric thickness of a few atoms raises unwanted quantum mechanical effects such as electron tunneling and gate leakage currents that compromise the classic MOS transistor operation. To maintain the Moore's law progress in microelectronic technologies [2] it is needed to use new materials with higher dielectric constant (high-*k* materials) to replace the conventional SiO_2. The high-*k* gate dielectrics are also required for ensuring high-performance and low-power CMOS applications in the 45 nm technology node and beyond [3]. The emerging nanoelectronic transistors will rely on non-silicon high-*k* materials with target effective oxide thickness (EOT) of less than 10 Å to advance beyond the sub-20 nm regime [2], [4].

There are many high-*k* candidates being studied. Ionic metal oxides, having highly polarized metal-oxygen bonds, would have much larger *k* values than that of the covalent dielectric materials. Amongst those materials, Hf-based materials, such Hf silicates, Hf aluminates, have been considered as the most promising materials and have already been used in the state-of-the-art CMOS technology.

Promising high-*k* candidates for alternative gate dielectric materials are the multicomponent dielectrics based on a multiple metal oxides. Ta_2O_5 is best high-*k* candidate for storage capacitors of nanoscale DRAMs; HfO_2 appears to be the respective candidate for nano-MOSFETs [4], [5], [6]. The electrical characteristics prove that the structure composed of HfO_2–Ta_2O_5 mixed layer on Si performs as a high-*k* layer in terms of permittivity, allowable level of leakage current, and appropriate oxide interface properties [7].

II. Surface potential based modeling

Compact device models need to be physical, simple (compact), accurate, and technology independent. Fitting of device data from different technologies across the industry with high accuracy is the most challenging task. The models are generally coded in circuit simulators using general-purpose languages. Accordingly, they are targeted specifically to the interface and internal data structures of their host simulator, and hence are inherently non-portable. In this context modification and optimization of a given model becomes a time-consuming and error-prone task.

An effective approach to obtain flexible modeling approach is to formulate open source code models in analog hardware description languages (HDLs) such as Verilog-A/AMS or VHDL-AMS. In the recent years Verilog-A has become increasingly viewed as most promising candidate for compact modeling purposes [8].

The basic equations for describing the MOS device characteristics are the Poisson's equation, the continuity equations, and the current-density equations [9]. Historically there are two major approaches to analytically describing device behavior: piece-wise modeling approach (also called regional approach or threshold-voltage based approach) and surface-potential based approach [10].

Piece-wise models describe MOSFET operation in the linear and saturation regions with separate equations. A fundamental problem is the discontinuity of drain current

characteristics which is solved by smoothing functions to interpolate the *I-V* characteristic between linear and saturation regions. With surface-potential based approach, on the other hand, model development focuses on surface potential (ϕ_s) formulation. These models allow an inherently single equation and accurate calculation of I_D. From the wide spread models in electronic design automation (EDA) industry the BSIM3/4 models are piece-wise based and PSP – surface-potential based.

In this paper a compact model for circuit simulation of the high-*k* MOS capacitor HfO_2–Ta_2O_5 mixed layer structure presented in [7] is developed. The model is coded in Verilog-A HDL based on the PSP model core. Capacitance–voltage (*C*–*V*) characteristics are compared to the measurements to validate the model. The BSIM3v3 formulation of the model of this same HfO_2–Ta_2O_5 structure is described in [11].

III. Model Formulation

The test structures for electrical measurements are MIS capacitors with a back side electrode of ~ 300 nm evaporated Al. The detailed characteristics of the modeled structure can be found in [7]. The capacitors are electrically characterized by means of *C*–*V* (Fig. 1) curves in the frequency range 50 kHz ÷ 100 kHz for minimizing the effects of parasitic series-parallel circuits [12].

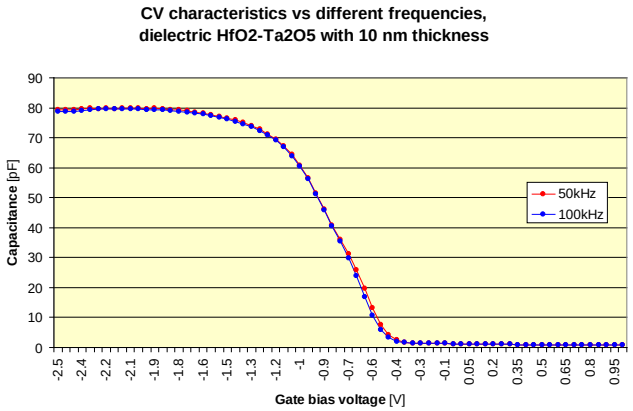

Figure 1. *C*–*V* characteristics measured by RLC meter versus two frequencies across 10 nm HfO_2-Ta_2O_5 capacitor stack.

By MOS capacitor measurements are obtained the physical properties of the developed technology for fabrication of high-*k* MOS devices. For example the effective dielectric constant ε_{eff} of the films is determined from the capacitance C_0 at an accumulation using ellipsometrically measured values of *d*. The oxide charge Q_f is also evaluated from the *C*–*V* curves.

A. Parameter extraction

The modeled high-*k* dielectric capacitor stack has parameters which are directly measured after its fabrication – gate area defined by width *W* and length *L*, and type of substrate conductivity (acceptor or donor). These parameters are typical design inputs which can be changed depending on the requirements of the layout.

Other parameters needed for the model are: relative permittivity of the dielectric, dielectric thickness, substrate doping concentration and flat band voltage. These parameters are technology dependant inputs for model adaptation which are not changed during layout design. Their values are summarized in **Table I** and they are determined either by direct measurements or by extraction based on the characterization *C*-*V* curves.

TABLE I. Summary of Preliminary Measured or Extracted Technology Parameters

Technology Parameter	Value	Dimension
Relative dielectric permittivity – ε_{rox}	9	dimensionless
Substrate doping concentration – N_{sub}	$1.25.10^{21}$	[m^{-3}]
Flat band voltage – V_{FB}	-0.55	[V]
Dielectric thickness – t_{ox}	10	[nm]

B. Model description

The objective of our MOS capacitor compact model is to enable simulation of the high-*k* MOS device using different design and technology parameters keeping model equations as simple as possible while giving highly accurate results. A model meeting the above requirements was already developed in [11] based on the BSIM3v3 core which is one of the most well-known regional models. It describes different operating regions with different equations.

Here we are focused on developing a compact model based on the novel surface-potential approach proceeding from PSP model equations that inherently possess continuous *I-V* characteristics. In this approach the equations are explicit functions of the surface potential ϕ_s instead of the applied voltage and as a result they are continuous for all bias conditions [13]. The main disadvantage is the requirement of separate iterative procedure for calculation of the surface potential ϕ_s as function of the applied voltage. In this model the iterative procedure is replaced with regional approach which is an easy way to incorporate all significant effects into the surface potential description

After simplifying the original PSP equations the intrinsic charge at the gate is expressed with the product of the oxide capacitance C_{ox} and the mid-point voltage V_{oxm}:

$$Q_g = C_{ox} V_{oxm} \tag{1}$$

$$C_{ox} = (\varepsilon_{rox}\varepsilon_o WL)/t_{ox} \tag{2}$$

$$V_{oxm} = \phi_T . x_{gm} \tag{3}$$

where $\phi_T = kT/q$ is the temperature potential and x_{gm} is a variable which depends on the surface potential described by the following expressions:

$$x_{gm} = G.\sqrt{D_m + P_m} \tag{4}$$

$$D_m = [1/E_s - x_s - 1 - \chi(x_s)]\Delta_{ns} \tag{5}$$

$$P_m = x_s - 1 + E_s \tag{6}$$

In equations (5) and (6) x_s is dimensionless potential at the silicon substrate surface which is computed from the temperature and real surface ϕ_s potentials:

$$x_s = \phi_s / \phi_T \tag{7}$$

The parameter G is calculated from the body effect coefficient γ:

$$G = \gamma / \sqrt{\phi_T} \tag{8}$$

where $\gamma = \sqrt{2.q.\varepsilon_{Si}.N_{sub}} / C'_{ox}$. The parameter $C`_{ox}=(\varepsilon_{rox}\varepsilon_0) / t_{ox}$ is the oxide capacitance per unit gate area.

The variables E_s and $\chi(x_s)$ are functions of the surface potential:

$$E_s = \exp(-x_s) \tag{9}$$

$$\chi(x_s) = x_s^2 / \left(2 + x_s^2\right) \tag{10}$$

The variable Δ_{ns} is in exponential dependence from the dimensionless bulk potential deep in the silicon substrate $x_{ns} = \phi_B/\phi_T$:

$$\Delta_{ns} = \exp(-x_{ns}) \tag{11}$$

Equations (1) ÷ (11) show the modeled charge is explicit function only of the surface potential and it is already described with same formulas for all bias operation regions.

However, the surface potential is not described continuously even in the PSP model. It is split into two regions separated by the marginal dimensionless band bending parameter x_{mrg} calculated from the body effect coefficient:

$$x_{mrg} = 10^{-5}\left(1 + G/\sqrt{2}\right) \tag{12}$$

The dimensionless band bending caused by the bias voltage is:

$$x_g = (V_{GB} - V_{FB} - ST_{V_{FB}}\Delta T) / \phi_T \tag{13}$$

The parameter ST_{VFB} is the temperature coefficient of the flat band voltage and ΔT is the temperature difference from the nominal temperature (21 °C).

The surface potential is described in two regions:

1) Accumulation and depletion when $x_g < x_{mrg}$

$$x_s = A_1\eta + a.\tau/(a + c) \tag{14}$$

$$\tau = -A_2\eta + A_3 \ln\left(a / G^2\right) \tag{15}$$

$$a = (-x_g - \eta)^2 \text{ and } c = 2.(-x_g - \eta) \tag{16}$$

$$\eta = \left(z + 10 - \sqrt{(z-6)^2 + 64}\right)/2 \tag{17}$$

$$z = -1.25x_g / \xi \tag{18}$$

2) Inversion and depletion when $x_g \geq x_{mrg}$

$$x_s = B_1\eta + a.\tau/(a + c) \tag{19}$$

$$\tau = x_{ns} - \eta + B_2 \ln\left(a / G^2\right) \tag{20}$$

$$\eta = \left(x_g + b_x - \sqrt{(x_g - b_x)^2 + 5}\right)/2 \tag{21}$$

$$b_x = x_{ns} + 3 \tag{22}$$

For the variables *a* and *c* are used expressions (16).

IV. Simulation Results and Fitting

The above model equations are coded in Matlab. Equations (14) ÷ (15) are simplified PSP equations in which the fitting non-physical variables A_1, A_2, A_3, B_1 and B_2 are introduced. The need for further fitting of these variables arises after comparing measurements versus simulation results at $A_1 = A_2 = A_3 = B_1 = B_2 = 1$ (cf. Figure 2).

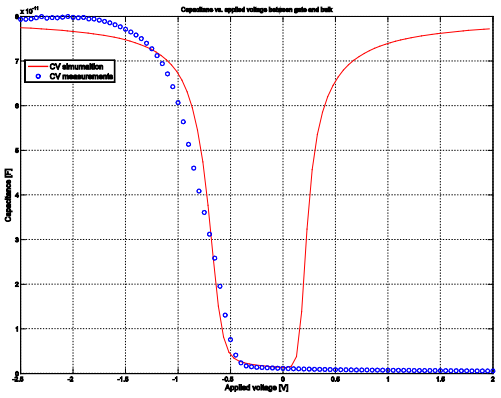

Figure 2. Simulation of *C-V* curve compared to measurements based only on the simplified PSP equations. Further fitting in all bias regions is need.

Both regions are additionally split into smaller pieces where different effects are dominant over different parts of the curve. In Figure 3 and Figure 4 it is observed how the MOS capacitor characteristics are changed after applying the piece-wise fitting of the variables.

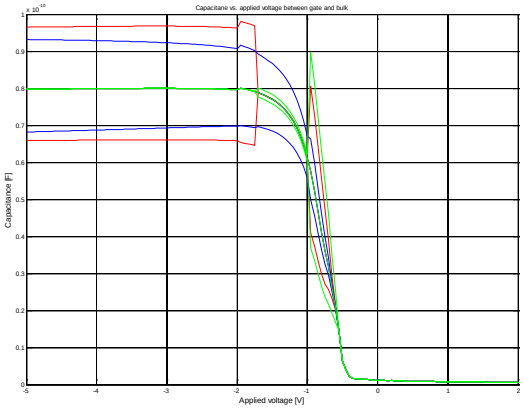

Figure 3. Fitting *C-V* curves by changing variables A1 (green), A2 (red) and A3 (blue) in accumulation and depletion regions.

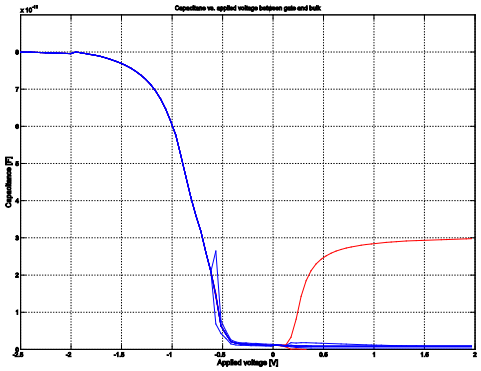

Figure 4. Fitting *C-V* curves by changing variables B_1 (blue) and B_2 (red) in inversion and depletion regions.

The performed additional split enables further easy adjustment of the surface potential so that the integral error of the mismatch between the simulations and measurements curves is calculated to be below a certain maximum of e.g. 3%. The outcomes from fitting of the variables within the entire bias range are given in the lookup Table II. The achieved matching between the model and the experimental data is presented in Figure 5.

TABLE II. LOOKUP TABLE OF THE FITTING VARIABLES A_1, A_2, A_3, B_1 AND B_3

Parameters: **Bias Voltage Range** [V]	A_1	A_2	A_3	B_1	B_2
$< (V_{FB} - 2.0)$	1	0.955	0.979	1.7	0.5
$(V_{FB} - 2.0) \div (V_{FB} - 1.75)$		1.022	1.02		
$(V_{FB} - 1.75) \div (V_{FB} - 1.0)$	0.04	0.002	0.9875		
$(V_{FB} - 1.0) \div (V_{FB} - 0.65)$	1.15	1.84	1.5		
$(V_{FB} - 0.65) \div (V_{FB} - 0.5)$	1.3	1.94		1.5	
$(V_{FB} - 0.5) \div (V_{FB} - 0.45)$				0.6	
$(V_{FB} - 0.45) \div (V_{FB} - 0.4)$				0.5	
$(V_{FB} - 0.4) \div (V_{FB} - 0.3)$				0.6	
$(V_{FB} - 0.3) \div (V_{FB} - 0.2)$				0.7	
$(V_{FB} - 0.2) \div (V_{FB} - 0.0)$				0.9	
$(V_{FB} - 0.0) \div (V_{FB} + 0.15)$				0.938	
$(V_{FB} + 0.15) \div (V_{FB} + 0.25)$				0.94	
$> (V_{FB} + 0.25)$					

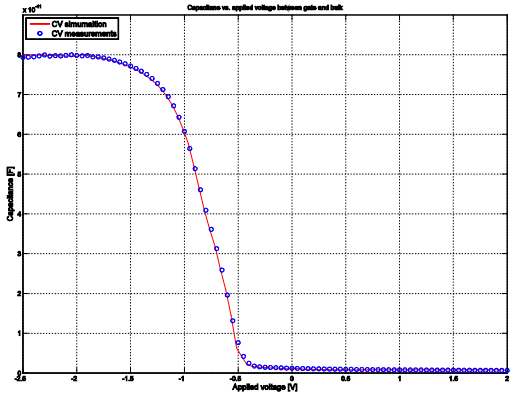

Figure 5. Plot of *C-V* simulation compared to experimental data after fitting. Highly accurate matching is achieved.

Essential part of the model is the surface potential ϕ_s and its function of the applied voltage is plotted in Figure 6. The abstract description of the surface potential is very important because it is developed together with the technology of the researched high-*k* MOS devices.

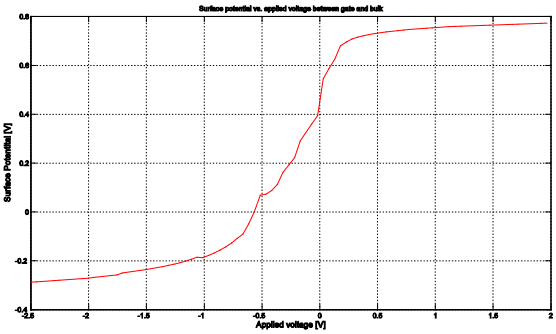

Figure 6. Plot of the surface potential versus the applied voltage. This function is technology dependant.

To perform the circuit simulations, the Matlab code was recoded in Verilog-A in order to input it to Spectre circuit simulator as an external model. The existing MOSFET in Cadence design kit can be simulated as MOS capacitor if the source, bulk, and drain nodes are connected together as described in [13]. The *C–V* characteristics are simulated in AC mode by plotting the capacitance as a calculation based on the amplitude of the current through the gate node for a frequency of 50 kHz. The input voltage is sinusoidal with fixed small signal amplitude of 10 mV and DC voltage sweep between –5 V ÷ +5 V.

Simulations with the developed model can be run well beyond the bias range (–2.5 ; 2.5) V for which we have experimental data. Outside this range the device behavior follows the natural asymptotic expectations. This is proven with parametric simulations within twice extended range (–5 ; 5) V using the dielectric thickness for parameter. The simulation plots in Figure 7 validate the model by confirming the proper asymptotic behavior.

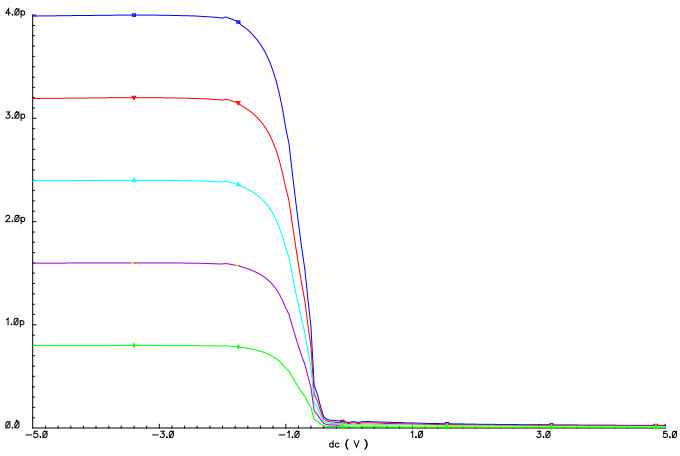

Figure 7. Plots of parametric *C-V* simulations for different values of dielectric thickness in extended bias range. The model behaves naturally as expected.

V. Verilog-A Code

Below we list an excerpt of the Verilog-A code of our model showing the computation of the surface potential and the continuous description of the intrinsic charge.

```
//Surface potential expressions
if (xg < -margin) begin
//accumulation and depletion reqions
SP_S_ysub  = -1.25 * xg * inv_xi;
SP_S_eta   = 0.5 * (SP_S_ysub + 10 -
             pow(((SP_S_ysub - 6.0) *
             (SP_S_ysub - 6.0) + 64.0),0.5));
SP_S_temp   = -xg - SP_S_eta;
SP_S_a    = SP_S_temp * SP_S_temp;
SP_S_c      = 2.0 * SP_S_temp;
if(Vgs<(-2.0+VFBO+0.55)) begin
SP_S_tau = -0.955*SP_S_eta +
           0.979*ln(SP_S_a * inv_G02);
end
if((Vgs>=(-2.0+VFBO+0.55))&&(Vgs < (-1.75 + VFBO +
    0.55))) begin
SP_S_tau    = -1.022*SP_S_eta + 1.02 *
              ln(SP_S_a * inv_G02);
end
if((Vgs>=(-1.75+VFBO+0.55))&&(Vgs < (-1.0 + VFBO +
    0.55))) begin
SP_S_tau    = -0.002 * SP_S_eta + 0.9875 *
              ln(SP_S_a * inv_G02);
end
if((Vgs>=(-1.0+VFBO+0.55))&&(Vgs < (-0.65 + VFBO +
    0.55))) begin
SP_S_tau    = -1.84*SP_S_eta + 1.5*ln(SP_S_a *
              inv_G02);
end
if(Vgs>=(-0.65 + VFBO + 0.55)) begin
SP_S_tau    = -1.94*SP_S_eta + 1.5*ln(SP_S_a *
              inv_G02);
end
nu    =  SP_S_a + SP_S_c;
x_s   =  -(SP_S_eta +SP_S_a * SP_S_tau / nu);
if((Vgs>=(-1.75 + VFBO + 0.55))&&(Vgs < (-1.0 +
    VFBO + 0.55))) begin
x_s   =  -(0.04*SP_S_eta + SP_S_a * SP_S_tau/nu);
end
if((Vgs>=(-1.0 + VFBO + 0.55))&&(Vgs < (-0.65 +
    VFBO + 0.55))) begin
x_s   =  -(1.15*SP_S_eta + SP_S_a * SP_S_tau/nu);
end
if(Vgs>=(-0.65 + VFBO + 0.55)) begin
x_s   =  -(1.3*SP_S_eta + SP_S_a * SP_S_tau/nu);
end
end
else begin
//inversion and depletion regions
SP_S_bx   = xn_s + 3.0;
SP_S_eta  = 0.5*(xg + SP_S_bx - pow(((xg -
            SP_S_bx)*(xg - SP_S_bx)+(5.0)),0.5));
SP_S_temp = xg - SP_S_eta;
SP_S_a    = SP_S_temp * SP_S_temp;
SP_S_c    = 2.0 * SP_S_temp;
SP_S_tau  = xn_s - SP_S_eta + 0.5*ln(SP_S_a/G02);
nu        = SP_S_a + SP_S_c;
if(Vgs<(-0.5+VFBO+0.55)) begin
x_s  =  1.7*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
if(Vgs>=(-0.5 + VFBO + 0.55)) begin
x_s  =  1.5*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
if(Vgs>(-0.45 + VFBO + 0.55)) begin
x_s  =  0.6*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
```

```
if(Vgs>(-0.4 + VFBO + 0.55)) begin
x_s  =  0.5*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
if(Vgs>(-0.3 + VFBO + 0.55)) begin
x_s  =  0.6*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
if(Vgs>(-0.2 + VFBO + 0.55)) begin
x_s =  0.7*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
if(Vgs>(VFBO + 0.55)) begin
x_s =  0.92*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
if(Vgs>(0.15 + VFBO + 0.55)) begin
x_s =  0.938*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
if(Vgs>(0.25 + VFBO + 0.55)) begin
x_s =  0.94*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
end
//Calculation of the intrinsic charge//
temp      =  1.0 / (2.0 + x_s * x_s);
xi0s      =  x_s * x_s * temp;
delta_1s  = exp(x_s);
Es        =  1.0 / delta_1s;
delta_1s  =  delta_ns * delta_1s;
Dm   = delta_1s - delta_ns * (x_s + 1.0 + xi0s);
Pm   =  x_s - 1.0 + Es;
Xgm  =  G0 * pow((Dm + Pm),0.5);
Voxm =  xgm * phit;
COX  = `EPSO * EPSROXO * W * L / TOXO;
Qg   =  Voxm * COX;
```

CONCLUSION

The MOS capacitor behavior of high-*k* HfO_2-Ta_2O_5 layer stack was studied proceeding from the surface potential description embedded in the intrinsic charge PSP model. The model was coded in Matlab for fitting purposes. The curves are fitted to the experimental data published in [7] with highly accurate matching – below 3% error; the curves also meet the natural asymptotic expectations. The optimized code was then programmed in Verilog-A to integrate with the Spectre simulator of Cadence Design Framework CAD tool.

In addition to the simulation results themselves the model realization represents a straightforward example of an all-purpose methodology for coding compact model equations in a portable, open-source environment applicable to various simulation platforms.

ACKNOWLEDGMENT

This paper is prepared in the framework of Contract No. ДТК – 02/50/17.12.2009.

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