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Compact Model of HfO_2-Ta_2O_5 capacitor in Verilog-A

George Vasilev Angelov

Abstract - **A circuit simulation compact model of a MOS capacitor made of high-*k* HfO_2–Ta_2O_5 stack layers is coded in Verilog-A. The model is based on the BSIM3v3 core. *C–V* and *I–V* characteristics are simulated in Cadence Spectre circuit simulator and validated against experimental measurements of the HfO_2–Ta_2O_5 stack structure.**

Keywords–**Compact model, high-*k* gate dielectric, Verilog-A**

I. Introduction

Significant challenges arise when bulk CMOS devices are scaled into the sub-100 nm regime following the Moore's law. The scaling of gate dielectric itself also poses a great challenge. As the physical thickness of the SiO_2 gate dielectric (T_{ox}) is scaled beyond 1.2 nm, quantum mechanical tunneling current from the gate into the channel becomes significant [1]. Further reduction in T_{ox} results in large static leakage current and large power consumption even when the device is turned off. Therefore at around the 45 nm technology node, a gate dielectric with high permittivity (high-*k* dielectrics) is often used to scale down the effective oxide thickness (EOT) without increasing the gate tunneling current. Besides high gate tunneling leakage current, the problems of polysilicon (poly-Si) gate depletion, high gate resistance, and boron penetration into the channel region also become more severe as the channel length and gate-oxide thickness are aggressively reduced. Therefore, there is vast interest in alternative high-*k* gate dielectrics [2].

Prospective candidates for alternative high-*k* dielectrics are the multicomponent gate stacks based on a combination of metal oxides. Ta_2O_5 is one of the most promising high-*k* materials for storage capacitors in nanoscale dynamic random access memories (DRAMs) while HfO_2 appears to be the respective candidate for nano-MOSFETs [3], [4], [5]. The electrical characteristics prove that the structure composed of HfO_2–Ta_2O_5 mixed layer on Si performs as a high-k layer in terms of permittivity, level of leakage current, and appropriate oxide interface properties [6].

In this paper we present a compact model of the high-k MOS capacitor HfO_2–Ta_2O_5 mixed layer structure from [6]. The model is implemented in Verilog-A HDL code based on the BSIM3v3 model equations. Capacitance–voltage (*C–V*) and current–voltage (*I–V*) characteristics are validated versus real measurements.

II. Verilog-A Model and Parameter Extraction

Our model has the following input parameters – gate area, oxide thickness, and relative dielectric permittivity, substrate doping concentration (N_{SUB}) and in the channel (N_{ch}), flatband voltage (V_{FB}) and interface trap level density (D_{it}).

Two MOS stacks are fabricated with thicknesses of the HfO_2–Ta_2O_5 layer of 10 and 15 nm. Their *C-V* and *I-V* characteristics are measured in [6], which allows the modeling of two physical quantities: capacity and leakage current between the gate and bulk electrodes. The *C-V* measurements are given in Fig. 1. Frequency range of 50 kHz ÷ 100 kHz is selected in order to minimize the effects of the equivalent series-parallel circuit – at lower frequencies the role of the parallel shunting resistance is increasing while at higher frequencies the series substrate resistance is becoming an important factor [7].

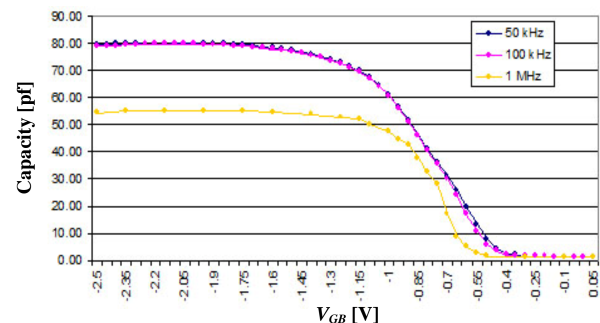

Figure 1. *C-V* characteristics measured at 50 kHz, 100 kHz, and 1 MHz.

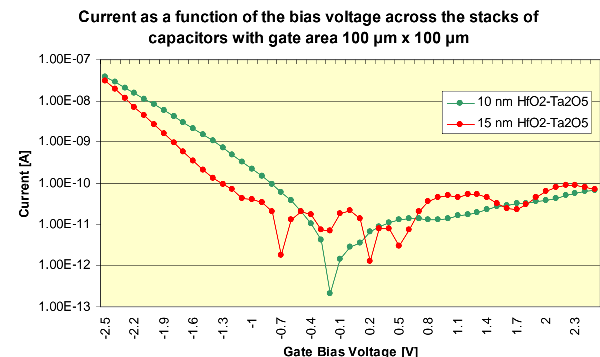

Figure 2. *I-V* characteristics measured by across 10 nm and 15 nm HfO_2-Ta_2O_5 capacitor stacks.

The model is based on the analytic compact model of BSIM3v3. Although BSIM3v3 is known for its extremely complicated intrinsic capacitance model we used it as base for our model equations because our technology design kit is using BSIM3v3 for the embedded models. Besides BSIM3v3 model allows relatively easy applicability across different technologies.

Below we provide an excerpt of the Verilog-A code of the model we developed.

```
// Device Parameters //
   parameter real L      = 100.0e-6;
   parameter real W      = 100.0e-6;
   parameter real TYPE   = 1.0;
   parameter real TOX    = 100.0e-10;

   real     acde, tox, cox, nch, tnom, vgs, Vgs;
   real     l, w, delta_3_1, delta_3_2;
```

G. Angelov is PhD, assistant professor with the Dept of Microelectronics FETT, Technical University of Sofia, 8 Kliment Ohridski blvd., 1797 Sofia, Bulgaria
e-mail: gva@ecad.tu-sofia.bg

```
   real      Vtm0, T0, T1, T2, T3, tmp;
   real      nsub, gamma2, k1, vfb, ldeb;

// Charge model related variables
   real      qgate, Qgate, Qsub0;
   real      cqgate;
   real      Vfb, CoxWL, Qac0, Vfbeff;
   real      Cox, V3, Tox, Coxeff, CoxWLcen, Tcen,
             Ccen, LINK, V4;

// Leakage model related variables
   real      igate, a1, b1;

// Calculation of the charge in accumulation //
Tox  = 1.0e8 * tox;
T0   = (Vgs - vfb) / Tox;
tmp  = T0 * acde;
Tcen = ldeb * exp(tmp);
LINK = 1.0e-3*tox;
V3   = ldeb - Tcen - LINK;
V4   = exp(0.5*ln(V3*V3 + 4.0 * LINK * ldeb));
Tcen = ldeb - 0.5 * (V3 + V4);
Ccen = `EpsSi / Tcen;
T2   = Cox / (Cox + Ccen);
Coxeff   = T2 * Ccen;
CoxWLcen = CoxWL * Coxeff / Cox;
Qac0 = CoxWLcen * (Vfbeff - vfb);

// Calculation of the charge in depletion //
T0   = 0.5 * k1;//ok119
T3   = Vgs - Vfbeff;
if (T3 < 0.0)
  begin
        T1 = T0 + T3 / k1;
  end
  else
  begin
        T1 = exp(0.5*ln(T0 * T0 + T3));
  end

Qsub0 = CoxWLcen * k1 * (T1 - T0);

// The following statements replace Qac0 with
                 Qsub0 for the depletion region //
if((vfb-vgs)<=-0.15)
  qgate = Qsub0;
else
  qgate=Qac0;

// Expressing the current as first
                     derivative of the charge //
Qgate  = qgate;
cqgate = TYPE * ddt(Qgate);
I(gate, bulk)  <+  cqgate;


// IV model //
if (tox < 12.5e-9)
  begin
        a1 = `A1;
        b1 = `B1;
  end
else
  begin
        a1 = `A2;
        b1 = `B2;
  end

if((vfb-Vgs)  >=  -0.25)
igate  =  a1*exp(-b1*Vgs)*w*l/(100e-6*100e-6);

if ((vfb-Vgs)  <  -0.25)
igate  =   (`a2 + `b2*Vgs)*w*l/(100e-6*100e-6);

I(gate, bulk)  <+  igate;
```

To adjust the model all parameters need to be properly extracted from measurement data. The developed model has the following input parameters – gate oxide area, thickness of dielectric, and type of bulk conductivity (P- or N-type). Other important parameters are the effective permittivity, substrate doping concentration, and flat band voltage. The effective permittivity is analyzed in [6] where it is extracted as $\varepsilon_{eff} \approx 9$ from the 100 kHz *C*–*V* curve. The methodology, described in [9], provides an easy way for calculation of the doping concentration and the flat band voltage. The substrate doping concentration (N_{SUB}) is related to the slope of the $1/C^2$ curve versus the V_G bias voltage [9]. The flat band voltage and doping concentration profile were not explicitly extracted from measurements due to the low accuracy of the method for bigger values of the interface trap density ($0.5 \div 1\times10^{12}$ $cm^{-2}eV^{-1}$ according to [7]). These parameters were fitted in the model according to the measurements.

III. Parameter Fitting

The initial model should be fitted in order to minimize the error with respect to the measurements. An accurate assessment of the fitting is given by calculating the integral error which is calculated as an average of the errors inside each interval.

Analyzing the model equations it turns out that the following parameters need to be fitted:

`acde` – influence in accumulation and depletion regions.

`nch` – influence in accumulation and depletion regions.

`delta_3_1` – influence in depletion region by changing the slope of the curve (visible for `nch` > 10^{16} cm^{-3}).

`Vfb` and `delta_3_2` – these parameters shift the curve across the *x*-axis (i.e. the applied bias voltage), therefore they have influence in depletion region.

The fitting starts with flat-band voltage (`Vfb`). Then the surface doping concentration (`nch`) is fitted in accumulation region together with the `acde` parameter. Further fitting of the slope in depletion region is done by varying `delta_3_1` and `delta_3_2` only. The fitting parameters in the corresponding regions of the *C*–*V* curve are depicted in Fig. 2.

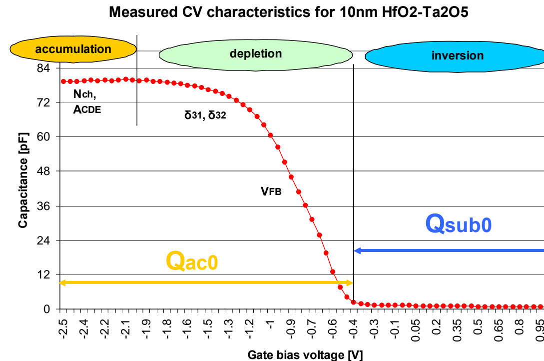

FIGURE 2. *C*–*V* CHARACTERISTICS SPLIT IN FITTING REGIONS.

The fitted parameters values are given in Table I. The *C*–*V* measurements fit very well with the simulation results for `Qsub0` for bias voltage greater than – 0.4 V. Therefore the expressions of the charge `Qac0` can be replaced with the expressions of `Qsub0` for $V_{GS} \geq V_{FB} + 0.15$.

TABLE 1. FITTED PARAMETER VALUES DESCRIBING THE C-V CHARACTERISTICS

Parameter	**Value**	**Bias Voltage Range [V]**
`Vfb`	– 0.55 V	(–∞, +∞)
`nch`	1.25×10^{18} cm^{-3}	(–∞, +∞)
`delta_3_1`	0.02 V	< (V_{FB} – 1.2)
`delta_3_1`	0.028 V ÷ 0.048 V	(V_{FB} – 1.2) ÷ (V_{FB} – 0.05)
`delta_3_1`	0.038 V ÷ 0.016 V	(V_{FB} – 0.05) ÷ (V_{FB} – 0.11)
`delta_3_1`	0.01 V	> (V_{FB} – 0.11)
`delta_3_2`	0.02 V	< (V_{FB} – 1.45)
`delta_3_2`	0.24 V	> (V_{FB} – 1.45)

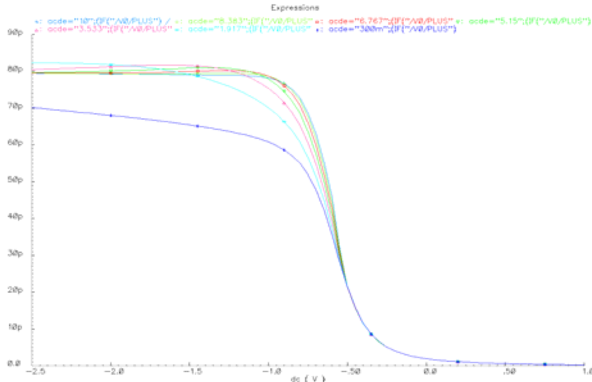

FIGURE 3. *C–V* CHARACTERISTICS AT DIFFERENT `acde` AND `nch` = 1.25×10^{17} CM^{-3}.

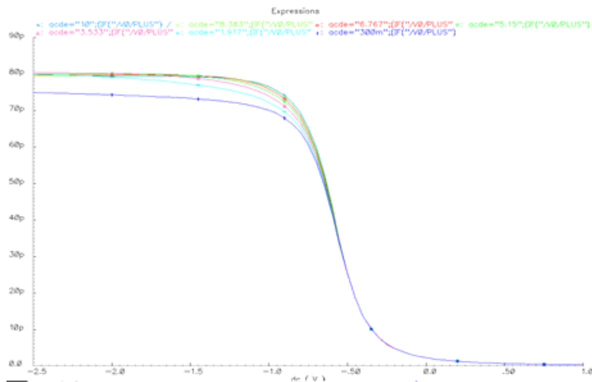

FIGURE 4. *C–V* CHARACTERISTICS AT DIFFERENT `acde` AND `nch` = 1.25×10^{18} CM^{-3}.

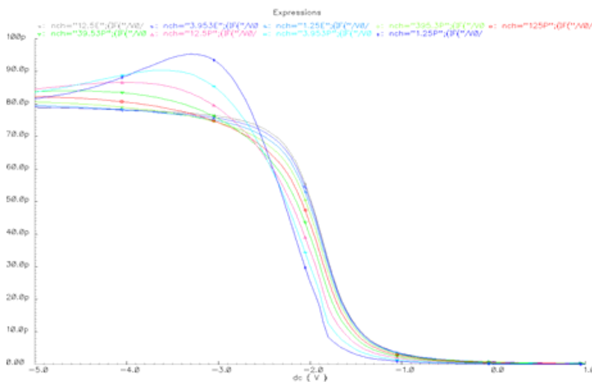

FIGURE 5. *C–V* CHARACTERISTICS AT DIFFERENT `nch`.

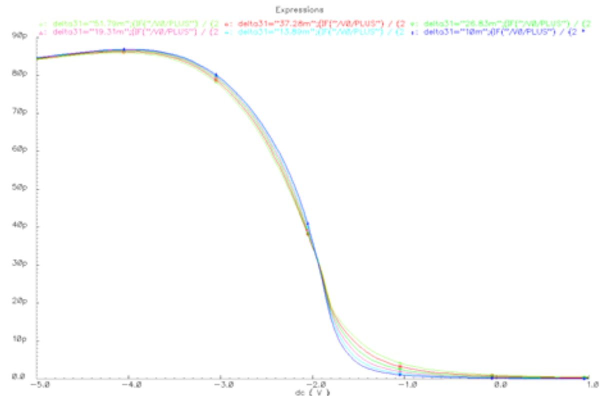

FIGURE 6. *C–V* CHARACTERISTICS AT DIFFERENT `delta_3_1` AND `nch` = 1.25×10^{16} CM^{-3}.

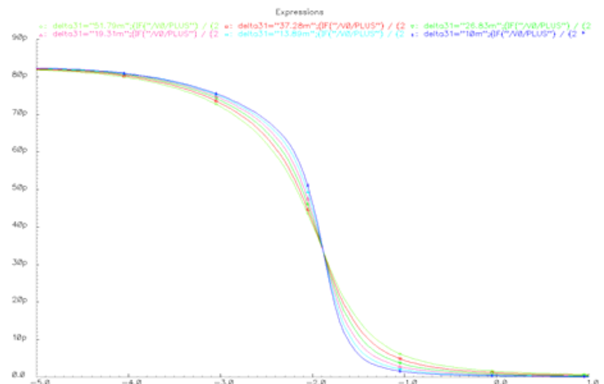

FIGURE 7. *C–V* CHARACTERISTICS AT DIFFERENT `delta_3_1` AND `nch` = 1.25×10^{17} CM^{-3}.

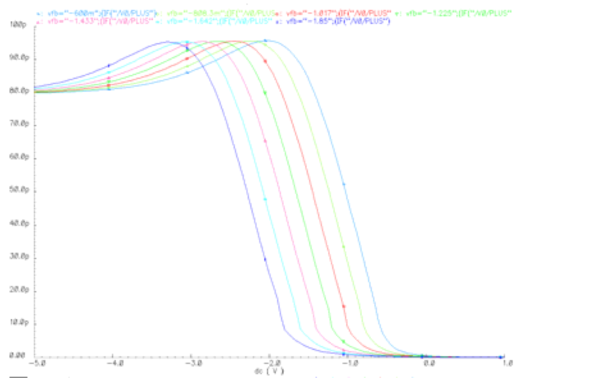

FIGURE 8. *C–V* CHARACTERISTICS AT DIFFERENT `Vfb`.

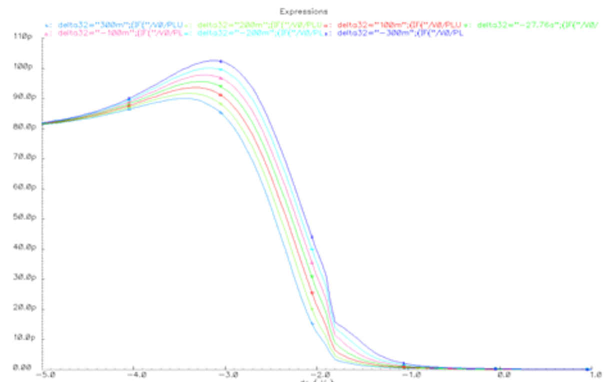

FIGURE 9. *C–V* CHARACTERISTICS AT DIFFERENT `delta_3_2`.

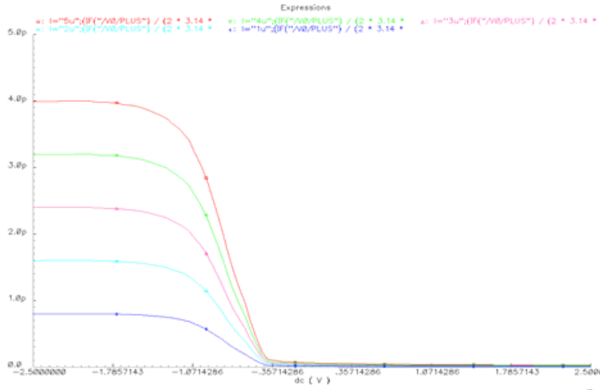

FIGURE 10. *C–V* CHARACTERISTICS AT DIFFERENT GATE LENGTHS `l`.

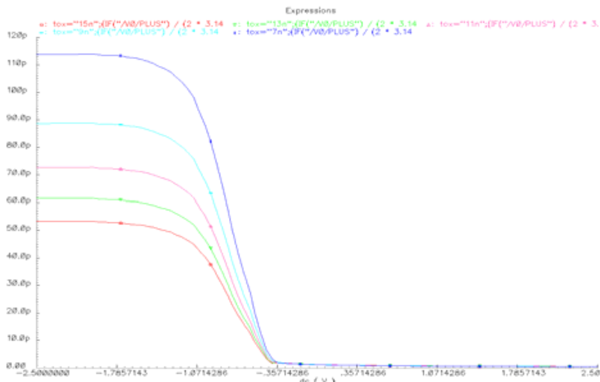

FIGURE 11. *C–V* CHARACTERISTICS AT DIFFERENT OXIDE THICKNESSES `Tox`.

The results of the influence of `acde` and `nch` parameters on the *C–V* characteristics are shown on Fig. 3, 4, 5, 6, 7, and 8. The influence of parameters `delta_3_1` and `Vfb` is given in Fig. 9 and 10.

For *C–V* characteristics the average integral error between the simulations and measurements curves was calculated to be erravg = 3.35 %.

The *I–V* characteristics are split in two regions with separate current density *J* equations: 1) accumulation and depletion region for $V_{GS} \leq V_{FB} + 0.25$ where the current density follows exponential dependence on the applied bias voltage ($J(V_{GS}) = a_1 e^{-b_1 V_{GS}}$) and 2) inversion region for $V_{GS} > V_{FB} + 0.15$ where the current density follows linear dependence on the bias voltage ($J(V_{GS}) = a_2 + b_2 V_{GS}$). The fitted parameters are in Table 2.

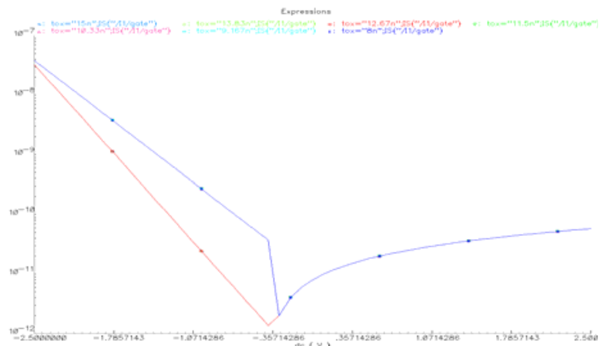

FIGURE 12. *I–V* SIMULATION AT DIFFERENT OXIDE THICKNESSES.

TABLE 2. FITTED PARAMETER VALUES DESCRIBING THE C-V CHARACTERISTICS

Coefficient	10 nm thickness	15 nm thickness
a_1	1.0×10^{-11}	2.0×10^{-13}
b_1	3.3	4.8
a_2	8.0×10^{-12}	
b_2	2.0×10^{-11}	

Afterwards the *I–V* model is validated by parametric analysis versus thickness (Fig. 12). The average integral error between the simulations and measurements for the *I–V* characteristics is erravg = 8.83 %.

IV. CONCLUSION

A compact model of a high-*k* HfO_2–Ta_2O_5 stack capacitance structure was developed in Verilog-A proceeding from the BSIM3v3 model core. The model was implemented in Cadence Spectre circuit simulator.

The Verilog-A compact model of the HfO_2–Ta_2O_5 mixed layer showed very good agreement to the experimental measurements for both the *C–V* and *I–V* characteristics. This proves the applicability of the model to state-of-the-art circuit design tools.

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