Design of 1T DRAM Memory Cell Using Verilog-A Model of High-*k* MOS Capacitor in Cadence

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Abstract – **A Verilog-A model of high-*k* MOS capacitor made of HfO_2-Ta_2O_5 stack is simulated in an 1T DRAM cell circuit in Cadence circuit simulator Spectre. Read and write operations of the 1T DRAM circuit with high-*k* and standard Cpoly capacitors are compared to each other. The high-*k* capacitor shows better performance and applicability to memory cell circuits.**

Keywords – **High-*k* gate dielectric, HfO_2-Ta_2O_5, DRAM, compact model, circuit simulation.**

I. Introduction

Microelectronic memories have wide application for data storage in computing devices. Being one of the major sectors in microelectronic industry, memory integrated circuits also follow the Moore's law. So the need is to produce memories with higher data capacitance, smaller sizes, higher density, lower consumption, higher reliability, faster performance. And all these requirements have to be met at low cost.

Device scaling results in extremely reduced oxide thickness of MOS structures. This implies unwanted physical effects such as leakage currents, tunneling, etc. A workaround to this problem is the implementation of alternative gated dielectrics which dielectric constant (high-*k*) is higher than the one of SiO_2 which means that we can obtain oxides with larger thickness that electrically behave like SiO_2 with lower thickness – i.e. with lower effective oxide thickness (EOT).

In this paper we simulate a high-*k* MOS capacitor in one transistor (1T) DRAM memory circuit [1]. The MOS capacitor is modeled in Verilog-A HDL proceeding from BSIM3v3 model equations [2]. To validate the model correctness the *C*–*V* and current and *I*–*V* characteristics are compared versus experimental measurements of a laboratory sample manufactured in the Institute of solid State Physics at the Bulgarian Academy of Sciences [3].

II. Circuit description and Simulations

The MOS structure was fabricated in two different dielectric thicknesses – 10 nm and 15 nm respectively to measure its *C*–*V* and *I*-*V* characteristics [3]. The high-*k* gate stack is a mixed layer of HfO_2-Ta_2O_5 under Al gate. Doping of Ta_2O_5 with the appropriate metals as well as mixing it with a new HfO_2 high-*k* dielectric expands the applicability of Ta_2O_5 as a memory material. Capacitors with doped Ta_2O_5 or mixed oxide (HfO_2:Ta_2O_5) have better parameters than those based on "pure" Ta_2O_5: higher dielectric constant, lower leakage current (under 10^{-10} A/cm^2), better electrical and thermal stability after stress at constant voltage, and constant current.

The advantages of the high-*k* HfO_2-Ta_2O_5 capacitor are given in [3]. Figures 1 and 2 present the *C*–*V* characteristics of the standard Cpoly capacitor within AMS 0.35 µm design kit and the high-*k* capacitor, respectively. Cpoly has practically constant capacitance of 784 fF between –3 V to 3 V while high-k capacitor drops from 8 pF to 0 in the same voltage range.

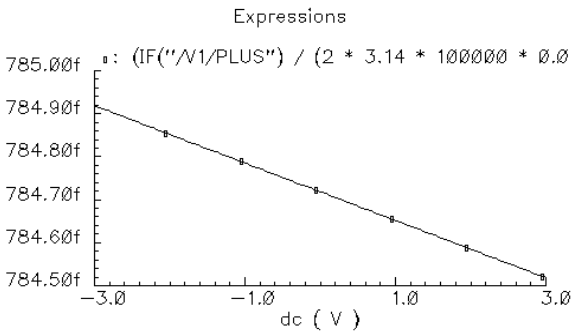

FIGURE 1. *C-V* CHARACTERISTIC OF CPOLY CAPACITOR.

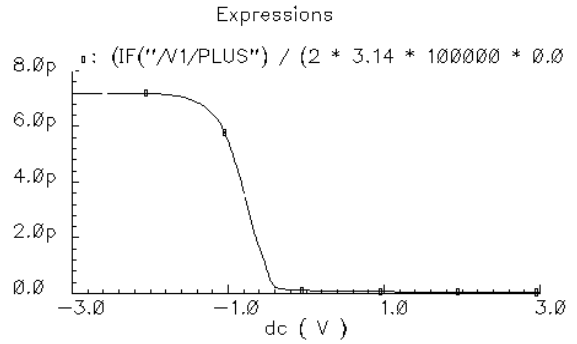

FIGURE 2. *C-V* CHARACTERISTIC OF HIGH-K CAPACITOR.

The high-*k* capacitor model is developed in ECAD Laboratory at the Technical University of Sofia. The Verilog-A code is implemented in Cadence Spectre circuit simulator as an external model [2].

Figure 3 shows 1T DRAM cell memory circuit with the high-k capacitor. The purpose is to simulate just one memory cell behavior. The memory cell consists of several block: a recharge circuit, an equalizer (PE), and a latch-type CMOS sense amplifier (SA) that are all connected to a bit

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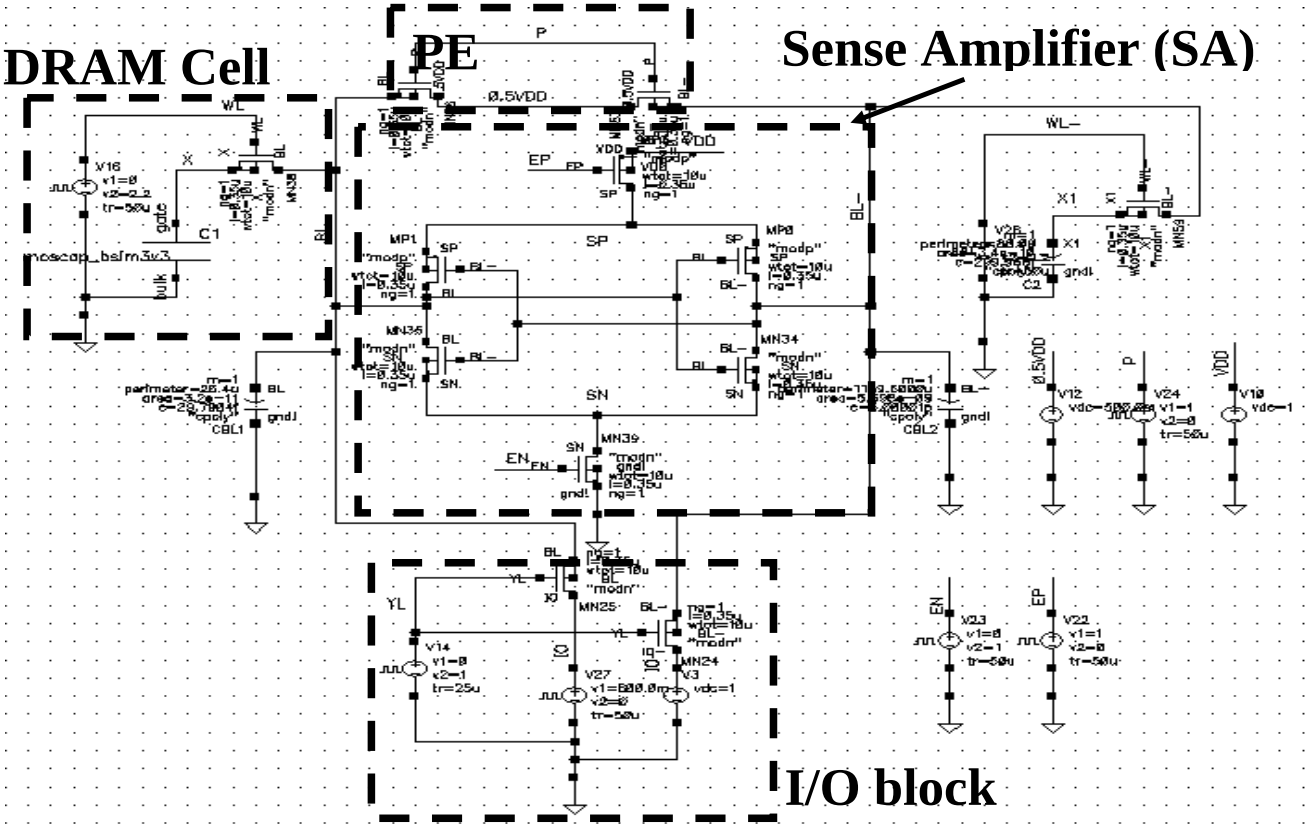
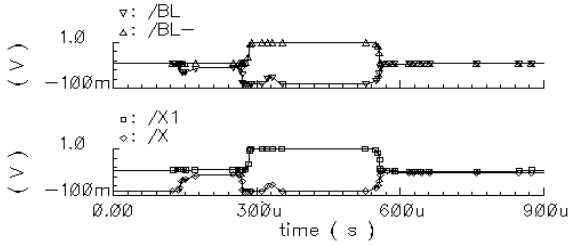


FIGURE 3. DRAM ARRAY AND DATA LINE CONFIGURATION WITH HIGH-K CAPACITOR

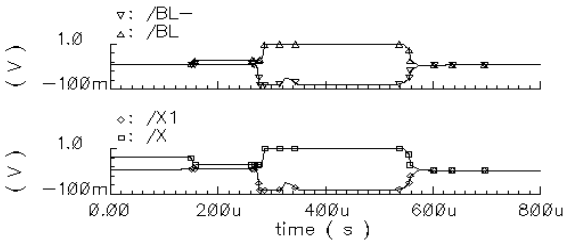
TABLE 1. PARAMETER SET FOR READ AND WRITE OPERATIONS.

Name	Parameters	Default value for read	Default value for write	Dimension
P	V1	1	1	V
	V2	0	0	V
	Delay time	100	100	µS
	Rise time	50	50	µS
	Fall time	50	50	µS
	Pulse width	350	350	µS
	Period	700	700	µS
0.5VDD	Vdc	0.5	0.5	V
WL	V1	0	0	V
	V2	2.2	2.2	V
	Delay time	130	130	µS
	Rise time	50	50	µS
	Fall time	50	50	µS
	Pulse width	370	370	µS
	Period	700	700	µS
VDD	Vdc	1	1	V
EP	V1	1	1	V
	V2	0	0	V
	Delay time	250	250	µS
	Rise time	50	50	µS
	Fall time	50	50	µS
	Pulse width	300	300	µS
	Period	700	700	µS

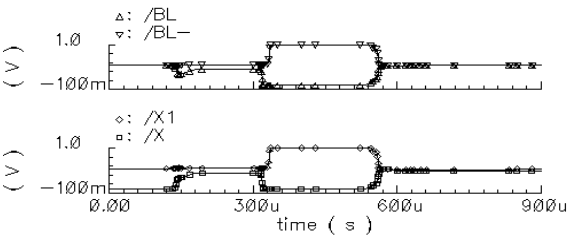
Name	Parameters	Default value for read	Default value for write	Dimension
EN	V1	0	0	V
	V2	1	1	V
	Delay time	250	250	µS
	Rise time	50	50	µS
	Fall time	50	50	µS
	Pulse width	300	300	µS
	Period	700	700	µS
YL	V1	0	0	V
	V2	1	1	V
	Delay time	300	400	µS
	Rise time	25	25	µS
	Fall time	25	25	µS
	Pulse width	225	125	µS
	Period	700	700	µS
IO	V1	0.8	1	V
	V2	0	0	V
	Delay time	300	350	µS
	Rise time	50	50	µS
	Fall time	50	50	µS
	Pulse width	200	200	µS
	Period	700	700	µS
IO-	VDC	1	1	V



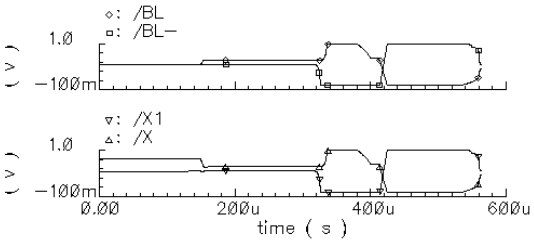
A) OPERATION READ OF 0 WITH HIGH-K CAPACITOR



B) OPERATION READ OF 1 WITH HIGH-K CAPACITOR



C) OPERATION WRITE OF 0 WITH HIGH-K CAPACITOR.



D) OPERATION WRITE OF 1 WITH HIGH-K CAPACITOR

FIGURE 4. THE READ/WRITE OPERATIONS OF THE HIGH-K CAPACITOR.

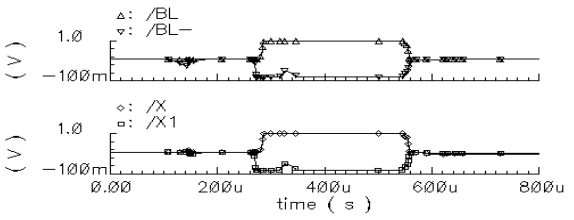
line (BL) (and a bit line with opposite signals $\overline{BL}$). All the blocks communicate with input/output lines. The 1T cell operation includes read, write, and refresh operations.

The *C–V* and *I–V* characteristics are simulated with AMS 0.35 µm CMOS technology with supply voltages V_{DD} = 1 V and V_{SS} = 0 V. The respective voltage levels of the sense amplifier, charge/recharge chain, and the input/output circuit are set according to the values in Tables 1 and 2.

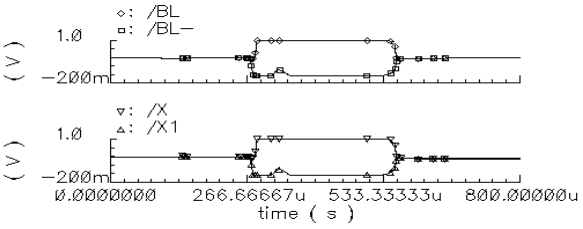
The simulation results are in Figure 4. Bit line parasitic capacitance C_{BL} is set to be greater than the cell storage capacitance C_S. because in a real DRAM memory there are a lot of cells which contribute to large value of C_{BL}.

We can discriminate between read and write operations by setting different input/output signals to the bit line. The write 0 operation is always preceded by a read operation. Hence, the old cell data are replaced by the new data [1].

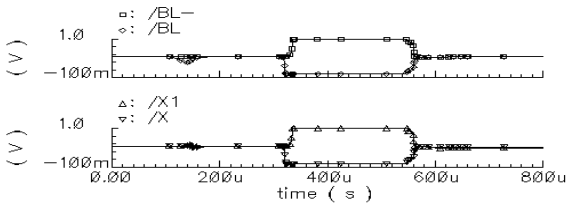
Operation read of 0 is given in Figure 4 a). When voltages V_{DD} = 1 V to V_{SS} = 0 V are applied the capacitance of the high-*k* capacitor (with L = 30 µm, W = 30 µm) changes from 67 fF to 110 fF. The capacitance of the capacitor in the second cell, connected to $\overline{BL}$ is C2 = 300 fF. The parasitic capacitance of bit line C_{BL1} = 30 fF and C_{BL2} = 5 pF.



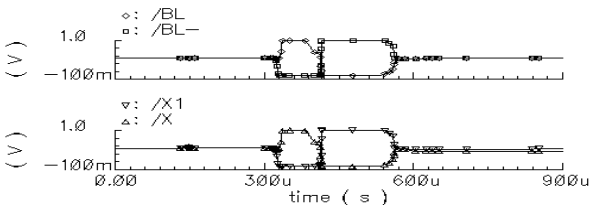
A) OPERATION READ OF 0 WITH CPOLY CAPACITOR.



B) OPERATION READ OF 1 WITH CPOLY CAPACITOR



C) OPERATION WRITE OF 0 WITH CPOLY CAPACITOR.



D) OPERATION WRITE OF 1 WITH CPOLY CAPACITOR.

FIGURE 5. THE READ/WRITE OPERATIONS OF THE WITH CPOLY CAPACITOR.

In order to change from read of 0 to read of 1 operation we have to swap places of IO and $\overline{IO}$ levels. Read of 0 operation begins with voltage on the capacitor (X) V_X = 5.684 mV then it reaches V_X = 390.3 mV and finally it drops to V_X = 0 V. In read of 1 operation shown on Figure 4 b) the capacitor's bulk is connected to the word line WL and the gate is grounded.

TABLE 2. PARAMETERS FOR COMPARISON OF CAPACITORS.

Capacitor	Type material of insulating layer	thickness of the insulating layer tox (nm)	Length / width of the layer (μm)
High-k	HfO_2-Ta_2O_5	10 nm	30/30 μm
Cpoly	S_iO_2	40 nm	30/30 μm

The capacitances are: C_2 = 300 fF, C_{BL1} = 5 pF and CBL2 = 5 pF. Capacitor voltage starts from 800 mV, goes up to 606 mV reaches 1 V (= V_{DD}) and finally goes to 0.5V.

In the write of 0 operation shown on Figure 4 c) the capacitances of the capacitor and the bit line are as follows: C_2 = 300 fF, C_{BL1} = 30 fF, C_{BL2} = 5 pF. The IO signal is applied to bit line BL and $\overline{IO}$ signal is applied to the bit line $\overline{BL}$. The voltage on the capacitor (X) starts from 5.684 mV, raises to 389 mV, reaches 0 V (= V_{SS}) and then goes to 0.5V.

In write of 1 operation we turn over the capacitor again and connect the gate to ground and bulk to the transistor source. We also change the signals applied to BL and $\overline{BL}$, this time connecting IO to BL. Capacitor's voltage starts from 800 mV, decreases to 606 mV and goes up to 1 V. Then it drops abruptly to 0 V to let the appropriate level be stored in the memory cell. The capacitor parameters are listed in Table 1.

Figure 5 shows the operations of an 1T DRAM memory cell performs using the standard capacitor Cpoly (again with L = 30 μm, W = 30 μm) from the AMS 0.35 μm CMOS technology design kit instead of the high-k capacitor.

In Figure 5 a) the of read of 0 operation is depicted. The capacitances are set as follows: C_1 = 300 fF, C_2 = 90 fF, C_{BL1} = 30 fF, C_{BL2} = 5 pF. The IO signal is applied to bit line BL. The parameters' values are also listed in Table 1. The voltage level of the Cpoly capacitor (X) starts at 441.7 mV, reaches 494 mV drops to 0 V and finally goes to 0.5 V (0.5 V is the voltage level at which the capacitor (X) voltage goes when the word line signal is over).

To show the read of 1 operation (Figure 5 b)) we change the places of IO and $\overline{IO}$. The capacitances are set to the following values: C_1 = 90 fF, C_2 = 300 fF, C_{BL1} = 3 pF and C_{BL2} = 5 pF. The voltage level of the Cpoly capacitor decreases from 539.7 mV to 504.7 mV then goes up to 1 V (= V_{DD}) and finally reaches 0.5 V.

In write of 0 operation shown on Figure 5 c) capacitances values are set as follows: C_1 = 300 fF, C_2 = 90 fF, C_{BL1} = 30 fF and C_{BL2} = 5pF. The IO signal is applied to bit line BL and the $\overline{IO}$ signal to $\overline{BL}$ (V_{DD} = 1 V). The voltage level of the Cpoly capacitor starts at 442.3 mV, climbs up to 494 mV and then goes back down to 0 V and finally raises to 0.5 V.

The parameters in write of 1 operation (Figure 5 d)) are set as follows: C_1 = 50 fF, C_2 = 300 fF, C_{BL1} = 5 pF and C_{BL2} = 3 pF. Write operation is always preceded by the reading operation. We observe voltage levels on the Cpoly capacitor of 562 mV to 504 mV and finally reaches 999.8 mV.

Comparing the circuits with the two capacitors we observe that due to the Cpoly's linear *C–V* characteristic we cannot see the well pronounced shape of increased voltage on Cpoly capacitor (X) like in the case of the high-*k* capacitor (Figures 4 a) and c) versus Figures 5 a) and c)).

III. CONCLUSION

Standard one transistor (1T) DRAM cell circuit was simulated in Cadence Spectre simulator using standard Cpoly capacitor with SiO_2 gate dielectric from AMS 0.35 μm design kit and using high-k capacitor with HfO_2-Ta_2O_5 gate stack implemented in Cadence with external Verilog-A model.

The simulated *C–V* and *I–V* characteristics allow to correctly predict the high-*k* DRAM circuit behavior. The results showed that the high-k capacitor has lower leakage currents, less losses, and less area. We also observed the greater capacitance of the high-*k* capacitor. Due to the nonlinear form of the high-*k* capacitor *C–V* characteristic and its larger capacitance the read and write operations have more pronounced and distinct voltage levels.

The use of high-*k* capacitor in the 1T DRAM cell proved to be fully applicable to memory circuits. In addition, it leads to improvements such as higher capacitance, lower leakage and smaller area of the capacitor.

ACKNOWLEDGEMENT

This paper is prepared in the framework of Contract No. ДУНК-01/03 dated 12.2009.

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