the relevance of the developed mathematical model for studying the processes of signals sampling in presence of timing jitter. The model plays major role for the analytical study and description of the problem given in [1].

3. The proposed algorithm helps the easy application of the method wherever the timing jitter causes problems with the accuracy, stability and statistics of the signal sampling based measurements with results in frequency domain.
4. The application of the method has an immediate economical effect by:
   - Shortening the product qualification and its production test by lowering the time needed for tests' correlation and industrialization
   - Helps the constant over time high quality of the IC production, significantly improving the quality determinative statistical indicators
   - Saves rejecting of functional ICs in case of test results distribution' marginal to the test limits
   - Does not engage additional computing and hardware resources

This paper presents a new developed DSP based test method for measurement in presence of timing jitter and application algorithm based on the identification of the amplitude peaks in a predefined frequency range of the sampled signal spectrum.

The method's powerful effect of suppressing the σ value at very low level independently of the jitter quantity increase is demonstrated graphically.

Experimental results of testing a lot of 150 ICs in an industrial environment are presented, using traditional DSP and the proposed method in turn, proving the high effectiveness of the last one in improving the statistics results of the tests.

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CONTINUOUS WORKBENCH OF SIMULATION & DESIGN SOFTWARE TOOLS FOR EDUCATIONAL APPLICATIONS

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The state-of-the-art MOS models for simulation and device simulators are depicted. The design workflow from process via device to circuit simulation is shown. Comparison between the simulation results of the device simulator Minimos-NT and the circuit simulator Spectre are provided. On the example of a ring oscillator circuit the coherence between these simulators is demonstrated. The existence of such continuous workbench is beneficial for both educational and industrial purposes.

I. INTRODUCTION

Device feature sizes have been reducing over the years and now crossed below 100 nm at the mass-production level. The ultra-deep submicron and nanometer CMOS ULSI technologies imply the use of complex multilevel development paradigms where ECAD and TCAD methodologies play the major role. The challenging demand is to utilize the available technology to the utmost, while reducing design margins. A key modeling goal is to set up a consistent modeling infrastructure from process through device/circuit to systems design level. Adequate modeling and simulation are integral parts of such an infrastructure. The particular simulation tool or a combination of tools should be chosen in accordance with the design complexity, the desired accuracy, and the available human and time resources.

Traditionally, technology developers and circuit designers are largely separate entities loosely linked by a set of layout files and SPICE model parameters. In the context of shrinking ULSI technologies the need for consistent modeling flow requires a continuous workbench of simulation and design tools.

II. ADVANCED SPICE MODELS

Nowadays, SPICE (initially developed by University of California at Berkeley (1972)) is the most well known and a de facto standard for circuits simulation. Lots of circuit simulators are available on the market: PSPICE (OrCad, Cadence Design Systems), Spectre (Cadence Design Systems), Eldo (Mentor Graphics), HSPICE (Synopsis), Saber (Analogy), TSPICE (Tanner Research), SmartSPICE (Silvaco), Smash (Dolphin Integration), APLAC (APLAC Solutions), etc.

Initially, analytical models were built with the intent to create an understanding of transistor behavior, rather than elemental models for a circuit simulation. Later with the development of SPICE, these models were used as elemental models of the

transistors. Downscaling device sizes calls for more corrections describing the wider variety of small geometry effects. Efforts have been made to include physical effects in the device models of the major commercial simulators [1]. Accurate fitting of device data from different technologies is the most challenging task facing SPICE models.

The major industry models today are BSIM 3v3/4, MM9/11, and EKV v2.6. The most popular model, BSIM3v3 [2], is an advanced submicron model that emphasizes physical formulation, computational efficiency, and ability to accommodate a variety of technologies. EKV v2.6 is oriented towards use in low-voltage, low-power analog and mixed design and simulation with very small number of parameters. Models such as BSIM3/4 and MM9/11 (Philips) are based on threshold voltage (V_{Th}) formulation. A disadvantage of this approach is the use of approximate expressions of I_{DS} in the weak- and strong-inversion regions, tied by a smoothing function. In result, the description of I_{DS} in the moderate inversion region is neither physical nor accurate (moderate inversion region becomes increasingly important in analog and RF design). To enlarge the physical content, model developments focus on charge sheet models based on surface potential (φ_s) formulation (e.g. SP2001) [3]. These models allow an inherently single-equation and accurate calculation of I_{DS}, and could serve as basis for the next sub-100nm generation of compact models [4].

In the present work, the Cadence Spectre simulator was used to demonstrate how industrial design software compares to TCAD simulation software, particularly to Minimos-NT.

III. DEVICE SIMULATORS

The continuously increasing computational power of computer systems allows the use of TCAD tools on a very large scale. Several commercial device simulators (such as APSYS, ATLAS, BIPOLE3, DESSIS, G-PISCES, and MEDICI), company-developed simulators (like FIELDAY and NEMO), and university-developed simulators (such as DEVICE, FLOODS, GALENE, Minimos, nextnano3, PISCES, and PROSA) have been successfully employed for device engineering applications (for detailed review see [5]). These simulators differ considerably in dimensionality, in choice of carrier transport model (drift-diffusion, energy-transport, or Monte Carlo statistical solution of the Boltzmann transport equation), and in the capability of including electro-thermal effects. The drift-diffusion transport model is by now the most popular model used for device simulation. With down-scaling of the feature sizes, non-local effects become more pronounced and they must be accounted for by applying an energy-transport model. Quantum mechanical effects gain increased importance with the scaling of the feature size.

The device simulator PISCES developed at Stanford University incorporates modeling capabilities for various devices and includes harmonic balance for large-signal simulation. MEDICI from Synopsys, which is based on PISCES, offers hydrodynamic simulation capabilities and rigorous modeling of carrier generation

and recombination processes. DESSIS from ISE offers extensive trap modeling. The density-gradient method is used to model quantum effects.

At the quantum level a one-dimensional Schrödinger-Poisson solver. NEMO, based on non-equilibrium Green's functions is offered for sub-100 nm structures. The program SIMBA links one-dimensional Schrödinger solver with a two-dimensional Poisson solver. Quasi-two-dimensional approaches using a simplified one-dimensional current equation are demonstrated by several simulators (among others BIPOLE3 from BIPSIM). A similar approach which couples a full hydrodynamic transport model with a Schrödinger solver has been developed at the University of Leeds. A software interface between the device model and the compact Root large-signal model within the Microwave Design System has been offered by Agilent.

Several critical modeling issues are addressed in the device/circuit simulator Minimos-NT [6], which we used for preparing the following examples.

IV. SIMULATION RESULTS

The continuous workbench of simulation and design software includes process simulation (TSUPREM4), device/circuit simulation (Minimos-NT) and circuit simulation (Spectre). The two-dimensional device simulator is equipped with an extensive mixed-mode circuit capability including modeling of distributed devices [7]. This allows insight into the performance of devices under realistic dynamic boundary conditions imposed by a circuit. Spectre [8] is an advanced circuit simulator that uses direct methods to simulate analog and digital circuits at the differential equation level. Its basic capabilities are similar in function and application to those of SPICE.

IV.1 Technology and Device Simulation

The process simulation (Fig. 1) starts from the blank wafer to the final device and reflects real device fabrication as accurately as possible. The implant profiles are calibrated to one-dimensional SIMS profiles. Process and device calibration is completed when the threshold voltage–gate length characteristic (V_{Th}–L_g) obtained by device simulation (Fig. 2) matches experimental data which indicates that the simulation includes advanced device behavior such as the reverse short channel effect and other short-channel effects [9].

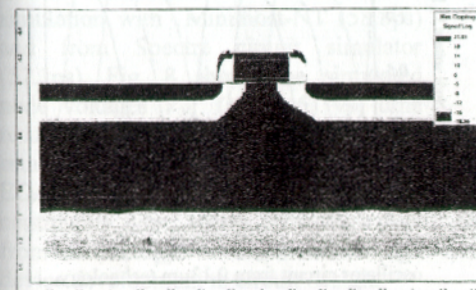

Fig. 1. Net doping concentration [cm^{-3}] in 0.35μm NMOS.

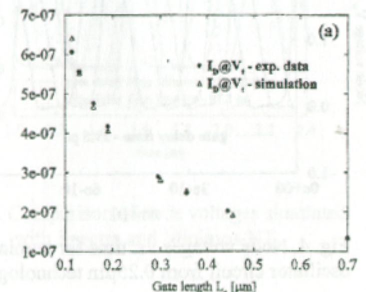

Fig. 2. Calibration of the drain current [A/μm] at threshold voltage.

The physical models in Minimos-NT are well calibrated [10], especially for silicon-based devices. There are only a few technology dependent model parameters that can be used for calibration purposes. One parameter is the gate workfunction difference which depends on the interface charges at the Si/SiO$_2$ interface and the properties of the polysilicon gate. Other parameters are used to model the surface mobilities, which strongly depend on the quality of the Si/SiO interface and on the electric field distribution in the channel.

IV.2 Circuit Simulation

High-speed operation is a key challenge for lots of novel devices. In CMOS digital circuits with static logic, the average gate delay time of a simple inverter chain provides a useful metric for the overall circuit speed. In our example a ring oscillator circuit, consisting of five inverter chains with the output fed to the input, is used. By determining the oscillation frequency f of such a ring circuit the average gate delay time t_d of one inverter stage can be calculated using $t_d = 1/(2nf)$ with n — number of stages (here $n = 5$).

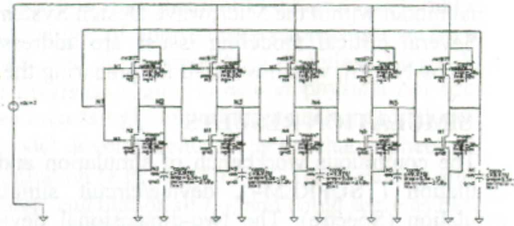

Fig. 3. Circuit diagram of a five stage ring oscillator.

Minimos-NT can handle various sub-micron technologies. Simulation results for 0.25μm and 0.13μm technologies are presented in Fig. 4 and Fig. 5, respectively, which are in good agreement with experimental data [9]. Opposite to that, the Spectre model available in our Cadence Design software is calibrated for 0.35μm technology and higher, and therefore, can be applied according to this constraint. Simulation results for devices with two different gate-widths from the 0.35μm technology are presented in Fig. 6 and Fig. 7, respectively.

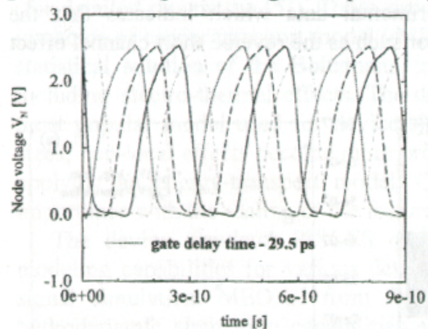

Fig. 4. Node voltages vs. time for nominal oscillator circuit from 0.25μm technology.

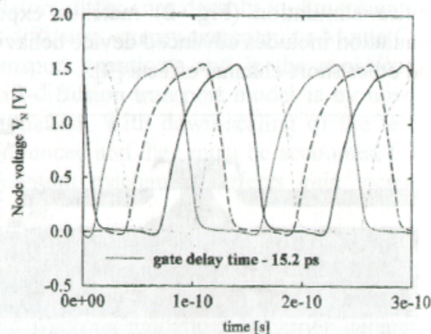

Fig. 5. Node voltages vs. time for nominal oscillator circuit from 0.13μm technology.

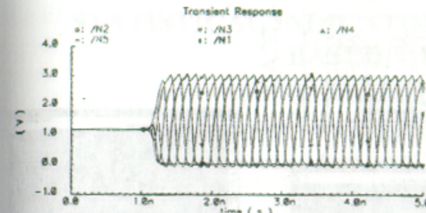

Fig. 6. Node voltages vs. time for oscillator circuit from 0.35μm technology (Wg=20μm).

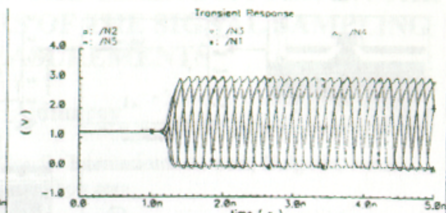

Fig. 7. Node voltages vs. time for oscillator circuit from 0.35μm technology (Wg=10μm).

IV.3 Comparison of results

The gate length L_g, gate width W_g, and applied voltage V_{DD} for the investigated technologies are summarized in Table I, together with simulation results for the ring circuit average gate delay time obtained with both simulators.

TABLE I — Simulation results of Minimos-NT and Spectre

Simulator	No.	L_g [um]	W_g [um]	V_{DD} [V]	C_L [fF]	Δ [ps]	$f = 1/Δ$ [GHz]	t_d [ps]
Minimos-NT	1	0.35	30	3.0	10	588	1.70	**58.8**
	2	0.25	20	2.5	5.4	295	3.39	29.5
	3	0.13	10	1.5	3.8	152	6.58	15.2
Spectre	1	0.6	30	3.0	10	1140	0.88	114.0
	2	0.6	20	3.0	10	1163	0.86	116.3
	3	0.6	10	3.0	10	1339	0.75	133.9
	4	0.35	30	3.0	10	573	1.74	**57.3**
	5	0.35	20	3.0	10	590	1.69	59.0
	6	0.35	10	3.0	10	640	1.56	64.0

Since our Spectre model is calibrated for 0.35 μm technology and higher, we were able to explicitly compare these results only. As can be seen from Table I, comparable average gate delays per stage t_d are obtained from device/circuit simulation with Minimost-NT (58.8ps) and from Spectre circuit simulator (57.3ps). Fig. 8 shows the simulated node voltages V_N (N=1…5) vs. time resulting from the two simulators. The established setup allows combination of ECAD and TCAD simulation tools in continuous flow, which provides a link from technology development through device development to circuit design.

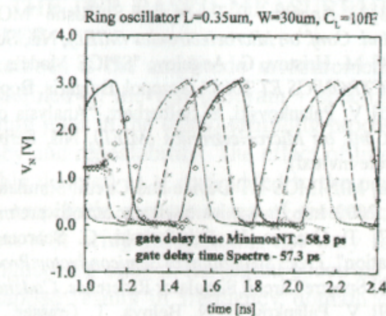

Fig. 8. Comparison of node voltages simulated with Spectre and Minimos-NT.

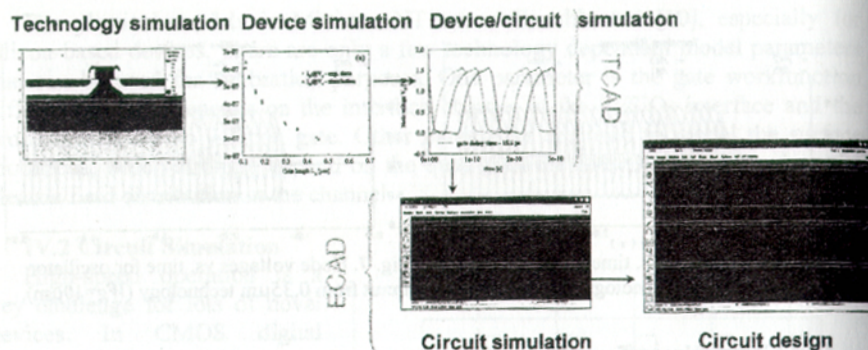

Fig. 9. Continuous simulation workflow including TCAD and ECAD tools.

V. CONCLUSION

A brief overview of the state-of-the-art SPICE models and simulation tools for MOS devices was given. The coherence between the simulators Spectre (Cadence) and Minimos-NT (TU Vienna) was demonstrated by a circuit simulation example. A continuous simulation workflow was established in our laboratory (Fig. 9). We believe the new setup can be beneficial for future scientific investigations and for demonstrations with educational purposes.

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STUDY OF THE IMPACT OF THE TIMING JITTER ON THE STATISTICAL INDICATORS OF THE SIGNAL SAMPLING BASED MEASUREMENTS

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Keywords – timing jitter, digital signal processing, statistical indicators, test results distribution.

This paper presents the results of a study focused on the impact the timing jitter has on the statistical indicators of the signal sampling based tests.

1. INTRODUCTION

The statistical indicators of the quality tests in production have crucial importance for the overall quality and cost of the new produced integrated circuits (IC) [8, 9]. The process of qualification of the new developed IC goes through the detailed investigation of the statistical indicators - *Cp*, *Cpк* and standard deviation – σ *of all tests* in the product specification [6, 8, 9]. Lower values of *Cp* and *Cpк* might lead to prolonged industrialization process of the IC, quality loss and cost increase as well as longer *time-to-market* period.

This paper presents the results of a study focused on the impact the timing jitter has on the statistical indicators of the digital signal processing (DSP) based tests. It is presented the mathematical model of the process of signal sampling in the presence of timing jitter. It is given the analytical equation describing the relation between the standard deviation and the timing jitter quantity.

2. STATISTICS PROBLEMS OF THE DSP BASED MEASUREMENTS IN THE PRESENCE OF TIMING JITTER

In the base of the DSP based test methods is the amplitude measurement of a known spectrum component of interest defined in the test program - spectral bin, frequency of interest. The presence of timing jitter in the signal sampling process has severe impact on the measurement accuracy and repeatability. The effect of jitter can be associated with a random timing variable denoted as tj, and added to the period T of the sampled signal. The result of the amplitude measurement of frequency bin corresponding to the frequency of interest will bring information not only for the spectral bin of interest but also for the neighboring ones in the signal spectrum. This is easily seen in fig. 1, where the overlapped results in frequency domain of the several times repeated measurement of a sampled signal with timing jitter is presented.