SPICE Modeling of MOSFETs in Deep Submicron

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Abstract

As the mainstream MOS technology is scaling into nanometer sizes, the development of physical and predictive models for circuit simulation that cover geometry, bias, temperature, DC, AC, RF, and noise characteristics becomes a major goal. The paper addresses the scaling trends and their limiting factors and follows through the evolution of the three MOSFET model generations of SPICE: from the Berkeley Levels 1, 2, 3 to the latest BSIM3v3, BSIM4, MM11, EKV, and SP2001. MOSFET models are examined emphasizing on device physics and mathematical techniques for numerical calculation.

Introduction

The key in the evolutionary progress, leading to today's computers and communication systems with superior performance, reduced cost per function, and reduced physical size, is the steady downscaling of transistor dimensions over the past decades. The mainstream VLSI technology comprises CMOS devices because of their unique characteristic of minimal standby power that allows for the integration of tens of millions of transistors on a single chip. As the device dimensions are scaled to the nanometer sizes, MOSFETs are approaching the fundamental physical limitation of the nanometer regime [1], [2].

Inseparably bound up with these advancements goes the evolution of device models and simulators to assist the VLSI ICs design at various levels of abstraction. Requirements for circuit simulations are rising. A hierarchy of simulators and algorithms, together with generations of device models, has been developed. Device models play very important role in the advancement of CMOS technology and they appear everywhere from fabrication technology development to IC design and manufacturing. It is essential to maintain a physically correct modeling of the real effects that govern the function of the MOSFETs when simulating circuit operations. MOSFET models should consist of simple, continuous, and accurate expressions that are valid in the whole inversion regime of operation (weak, moderate, and strong) [3], [4].

Device Modeling

The purpose of device modeling is to describe device performances in mathematical terms. A model can be derived from theoretical or empirical considerations, or both. Typically, models are initially developed by analytically applying basic physical principles and then empirically modifying the resulting mathematical expressions to improve agreement between theoretical and experimental results. Ideally, only a few parameters should be required to describe the model, and a simple and consistent characterization procedure should be devised.

Tradeoffs are often made between the quality of approximation and its complexity. The required accuracy and intended use of the model are factors the engineer considers when making these tradeoffs. A very simple model is generally necessary to provide insight for design and facilitate symbolic hand manipulations whereas a more accurate and correspondingly more sophisticated model is generally preferred for computer simulations of circuits employing these devices. Besides, different interest groups use the model for different purposes and thus, push for different priorities in model developments. For example, a physicist or device engineer normally wants the model to be physical so that all the device physics are represented. On the other hand, circuit designers set higher priority for simplicity and efficiency in computation.

Initially analytical models were built with the intent to create an understanding of FET behavior, rather than elemental models for a circuit simulation. Later with the development of SPICE, these models were used as elemental models of the FETs. Downscaling device geometries further and further calls for more corrections to be added to describe the wider variety of small geometry effects. Model focus shifted from the physically based analytical description of device behavior to a structure which would provide the best results for a circuit simulation. Efforts have been made to add all kinds of physical effects (in the following section we address some of the most important of them) to device models and implement them in the major commercial simulators.

Downscaling Trends and Limiting Factors

Downscaling has been manifested by the four main IC technology generations that formed up: micron, submicron, deep submicron and very deep submicron. At the same time plenty of limiting factors, as short-channel and quantum effects, accompany this technology evolution and strongly affect the device operation since numerous characteristics and measurable parameters of the MOSFET (such as the surface potential, the drain current, the transconductances and the transcapacitances, etc.) change. All these effects directly reflect the complexity of device models causing numbers of physical, mathematical and computational problems.

Lithography is one of the key technologies that enable Moore's law. Continued improvements in optical projection lithography have enabled the printing of ever finer features, the smallest feature size decreasing by about 30% every two years. The deep submicron technology started in 1995 with the introduction of lithography better than 0.35 μm and the very deep submicron technology concerns lithography below 0.1 μm. In 2007, the lithography is expected to decrease down to 0.07 μm.

A. Short-Channel Effects

In the coming years, following the Moor's law, Si MOSFETs will continue to scale down, but the scaling limits are becoming more apparent. Yet the traditional submicron MOSFETs (channel length > 0.35 μm) suffer the "classical" *velocity saturation* effect: the drifting carriers between the transistor's source and drain. The result is reduced electron mobility (μ_n) and thus an increased channel's effective sheet resistance. Another short-channel effect is the *threshold voltage* (V_{Th}) *reduction* as transistor channel length (L_{gate}) decreases and as drain-to-source voltage (V_{DS}) increases; the result is an increase in drain current and thus a decrease in the MOSFET's output resistance. The *drain-induced-barrier lowering* (DIBL) is the cause, and its origin is the lateral-electric field contribution. *Substrate current induced body effect* (SCBE) is a result of the hot carries causing impact ionization and generating a substrate current; this takes place for electric fields greater than 10^7 V/m. The origin of the *reverse short-channel* (RSC) effect is a substrate impurity pileup at the surface near the source/drain contacts.

Reduction of the *source/drain junction extensions* (SDE) is limited by the increase in its parasitic resistance. The International Technology Roadmap for Semiconductors predicts that the SDE junction depth will downscale to around 10 nm to maintain acceptable short channel performance. Reducing junction depth below 30nm, however, degrades drive current and may lead to a high series resistance problem threatening the ultimate device performance. The series resistance might be a serious limiting factor for CMOS downscaling into nanometer regime [9].

B. Gate-Oxide Leakage

To minimize short channel effects when scaling into nanometric sizes, the transistor lateral-to-vertical aspect ratio must be preserved from one technology generation to the next. This requires the gate oxide thickness (t_{ox}), the junction depth, and the depletion depth to all scale down by 30% per generation. As t_{ox} is downscaled to the orders of atomic layers (CMOS devices with $L_{gate} \approx 100$ nm, need $t_{ox} \approx 3$ nm), the electrical barriers in the device begin to lose their insulating properties and the oxide becomes a subject to direct band-to-band quantum tunneling. The latter gives an exponential rise to a *gate leakage current* – the gate current is no longer negligible but it still remains small compared with the on-state current of the device. In results, an increase of the chip standby power is observed, thus limiting the integration and the switching speed [5]. Assuming the active gate area per chip is of the order of 0.1 cm^2, the maximum tolerable gate leakage current will be of the order of 10 A/cm^2. This sets a lower limit of $t_{ox} \geq 1.0$ nm. DRAMs are subject to more rigorous leakage requirements and therefore have a higher minimal gate-oxide thickness [6].

C. Depletion Effects

The reduced thickness of the gate oxide, along with the use of highly doped channel and polysilicon gate, is the reason for the loss of inversion charge and therefore transconductance due to inversion-layer quantization and depletion effects in the polysilicon-gate (polydepletion). With regard to *quantization*, it is necessary to discriminate between physical and electrical oxide thickness. The physical oxide thickness ($t_{ox,ph}$) is the actual grown thickness of the oxide, and the electrical thickness ($t_{ox,e}$) is the effective oxide thickness for inversion charge calculations, i.e. that fits best to the measured data. In classical analysis charges are assumed to concentrate right on the oxide–semiconductor interface, i.e. $t_{ox,ph} = t_{ox,e}$ (this is adopted in BSIM3, see Eq. (**8**)). Quantum mechanics states that the maximum probability of carrier distribution (the peak of the electron density) occurs at distance about 1 nm below the interface.

This effectively reduces the gate-oxide capacitance and consequently the inversion charge to those of an equivalent oxide thickness ($t_{ox,e}$) approximately 0.4 nm greater than the physical oxide thickness ($t_{ox,ph}$) [7]. (BSIM4 model recognizes the difference between $t_{ox,ph}$ and $t_{ox,e}$, see Eq. (9)).

Likewise, *depletion effects* occur in poly-Si (after entering the strong inversion in the bulk Si) in the form of a thin space-charge layer near the oxide-semiconductor interface which reduces the gate capacitance and inversion-charge density for a given gate drive. Accounting the above two effects, the scaling limit of the electrical oxide thickness ($t_{ox,e}$), appears to be 1.5–2.0 nm [8].

D. Power supply and threshold voltage

Supply voltage (V_{DD}) will continue to reduce each technology generation contributing to lower power dissipation. It is observed that V_{DD} has not been decreasing at a rate proportional to the channel length; therefore the field has been rising over the generations with 100 nm < L_{gate} < 1 µm. Thinner oxides are more reliable at higher fields and thus allow MOSFET operation at the reduced (but non-scaled) supply voltages. As V_{DD} reduces, *threshold voltage* (V_{Th}) have to reduce at the same rate to maintain enough gate overdrive and allow circuit performance to improve 30% each generation. Lower V_{Th} causes the MOSFET subthreshold (off-state) leakage current (I_{OFF}) to rise exponentially (I_{OFF} would further increase by about 10 times for every 0.1-V reduction of V_{Th}). For a chip with an integration level of 10^8 transistors, the average leakage current of turned-off devices should not exceed 10^{-8} A; this restriction holds $V_{Th} \geq 0.2$ V.

Power dissipation is increasing due to higher operating frequencies and transistor integration. Although supply voltage will continue to reduce, its contribution to the overall power reduction is not enough. The active power of high-end microprocessors today is already in the range of 30–100 W. To contain this trend power-efficient micro-architectures are required and the die size and frequency growth may need to be contained. Expensive packaging solutions will soon be needed to dissipate the heat generated by the chip.

Finishing our quick scaling outlook, we will mention that planar CMOS transistors with extremely downscaled sizes have already been reported. One of the smallest experimental MOSFETs realized to date, operates a physical gate length of 30nm [10].

SPICE Models

Nowadays, SPICE (initially developed by University of California at Berkeley (1972)) is the most well known and widely adopted tool (a de facto standard) for simulation of electrical circuits. Some of the major commercial circuit simulators are HSPICE (Synopsis), PSPICE (OrCad, Cadance Design Systems), SPECTRE (Cadence Design Systems), Eldo (Mentor Graphics), Saber (Analogy), TSPICE (Tanner Research), SmartSPICE (Silvaco), Smash (Dolphin Integration), APLAC (APLAC Solutions), etc.

SPICE is made up of two distinct parts: SPICE simulator and SPICE device models [7]. The simulator is the mathematical instrument to perform numerical analyses. The device models that the various simulators include are the core of the simulation program. Below we will follow through the most popular SPICE models of the past decades till today.

A. First Generation

The First model generation is comprised of Level 1, Level 2, and Level 3 models (they constitute the original release of Berkeley SPICE). These models express the original intent of a physically based analytical MOSFET model, with all geometry dependent included in the model equations, rather than focusing on the mathematical representation.

LEVEL 1 (1972) implements Shichman-Hodges model (1968) [11]. Simplifications such as gradual channel approximation and the square law for the saturated drain current are employed. The only geometry effect that is included is the channel length modulation (CLM). The model is applicable to devices with gate length L_{gate} > 10 µm.

For the linear region ($V_{GS} > V_{Th}$ and $V_{DS} < V_{DS}^{sat} = (V_{GS} - V_{Th})$) the drain current is:

$$I_{DS} = KP\frac{W}{L_{eff}}\left[(V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2}\right](1 + \lambda V_{DS}) \quad (1)$$

λ is the channel length modulation parameter, KP is the transconductance parameter ($KP = \mu_n C_{ox}$), L_{eff} is the reduced channel length due to the lateral diffusion. The threshold voltage is

$$V_{Th} = V_{Th0} + \gamma\left(\sqrt{2\phi_F - V_{SB}} - \sqrt{2\phi_F}\right). \quad (2)$$

For the saturation region ($V_{GS} > V_{Th}$, $V_{DS} > V_{DS}^{sat}$)

$$I_{DS} = KP\frac{W}{L_{eff}}\frac{(V_{GS} - V_{Th})^2}{2}(1 + \lambda V_{DS}) \quad (3)$$

Altogether there are five electrical parameters that characterize the model: KP, V_{Th}, γ, $2\phi_F$ and λ.

LEVEL 2 comes as an advanced version of Level 1; implements Meyer's model [12]. It is a physical semi-empirical model that includes a more detailed description of the depletion region, the threshold region and the mobility degradation by the vertical field. A model for V_{DS}^{sat} reduction by the velocity saturation and a subthreshold current model are also

added. Level 2 presents a better model but with less simplifications than Level 1. Applicable to very long-channel devices (L_{gate} ~ 10 μm).

LEVEL 3 (1978) is developed to overcome the observed shortcomings of Level 2. This is a semi-empirical model that places more emphasis on parameter extraction, while its structure is basically similar to Level 2. Include some new physical effects such as DIBL and mobility degradation by the lateral field. The basic difference between Level 2 and 3 is that Level 3 model is more efficient mathematically, and at least as accurate as Level 2. Applicable to long-channel devices (L_{gate} ~ 2 μm).

B. Second Generation

The Second generation shifts the focus to circuit simulation and parameter extraction. Thus, the quality of final model becomes heavily dependent on parameter extraction. The equations are subject to extensive mathematical conditioning. Individual device parameters are introduced and an entirely separate parameter structure to describe the geometry dependence is created. In result, empirical parameters without clear physical meanings appear.

BSIM1 (Berkeley Short-Channel IGFET Model), (1985) puts the emphasis upon mathematical conditioning for circuit simulation – relies on empirical parameters and polynomial equations to various physical effects. Improved descriptions of the threshold voltage and the mobility are implemented. In addition, a more detailed subthreshold current model is introduced. Overall, BSIM1 is an improved digital model. It has 39 parameters (in SPICE3) and is applicable to short-channel device with L_{gate}~1.0 μm.

The threshold voltage is calculated by [13]

$$\begin{aligned} V_{Th} &= V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F + V_{SB}} \\ &- K2(2\phi_F + V_{SB}) - ETADB \cdot V_{DS} \end{aligned} \quad (4)$$

$K2$ — drain/source depletion charge-sharing coefficient, $ETADB$ — DIBL related parameter.

The drain current in the linear region is

$$I_{DS} = \frac{\mu_Z}{1+U0_Z(V_{GS}-V_{Th})} \frac{C'_{ox}(W_{eff}/L_{eff})}{\left(1+\left(U1_Z/L_{eff}\right)V_{DS}\right)} \times\left[(V_{GS}-V_{Th})V_{DS} - \frac{a}{2}V_{DS}^2\right] \quad (5)$$

μ_Z – zero-bulk-bias mobility, $U0_Z$ – zero-bias transverse-field mobility degradation coefficient, $U1_Z$ – zero-bias velocity saturation coef., a – variable.

In saturation the drain current is

$$I_{DS} = \frac{\mu_Z}{1+U0_Z(V_{GS}-V_{Th})} \frac{C'_{ox}(W_{eff}/L_{eff})}{2aK}(V_{GS}-V_{Th})^2 \quad (6)$$

BSIM2 (1990) comes as extension to BISM1. It adds further effects on short channel devices. BSIM2 makes extensive modifications to the BSIM1 description of mobility and drain current, including a new subthreshold current model that gives better accuracy and convergence. An output conductance model is added, enabling analog design application. BSIM2 uses more than 30 electrical and 90 geometry-dependent parameters. Applicable to L_{gate} ~ 0.2 μm.

MODIFIED BSIM (HSPICE Level 28) is a proprietary model developed by Meta-Software. The model is empirically structured, suitable for analog design through extensive mathematical conditioning. All that result in a heavy reliance on parameter extraction. The model is applicable to submicron devices with L_{gate} ~ 0.3 – 0.5 μm.

C. Third Generation — Advanced Models

Third model generation returns to a simpler model structure with a reduced number of parameters; the parameters are physically based rather than empirical. Models employ smoothing functions to obtain a single-equation describing the *I-V* and *C-V* characteristics and continuity of *I-V* and *C-V* characteristics.

BSIM3 is the most popular submicron MOSFET model. It features include the high-field and short-channel effects such as mobility reduction, carrier velocity saturation, DIBL, CLM, substrate current, SCBE, RSC, subthreshold current, parasitic resistance effects, as well as improved convergence properties. BSIM3v3 (1995) has approximately 120 parameters and is applicable to L_{gate} ~ 0.18 μm. It adopts a single equation (via smoothing functions) for describing device properties for all operation regions to eliminate the discontinuity in *I-V* and *C-V* characteristics. [14]. Full exact equation listing find in [7], [15].

The general form of the I_{DS} equation is given by

$$I_{DS} = \frac{I_{DS,0}}{1+\dfrac{R_{DS}I_{DS,0}}{V_{DS}^{\text{eff}}}}\left(1+\frac{V_{DS}-V_{DS}^{\text{eff}}}{V_A}\right), \quad (7)$$

where V_A is the Early voltage generated by the MOSFET resistance model. $I_{DS,0}$ is

$$I_{DS,0} = \frac{W_{eff}\mu_{eff}C'_{ox}V_{GST}^{eff}}{L_{eff}\left[1+\frac{V_{DS}^{eff}}{\varepsilon_{sat}L_{eff}}\right]}\left[1-\frac{A_{bulk}V_{DS,eff}}{2\left(V_{GST}^{eff}+2\frac{kT}{q}\right)}\right]V_{DS}^{eff} \quad (8)$$

C'_{ox} – oxide capacitance per unit area, V_{DS}^{eff} – effective drain-to-source voltage, V_{GST}^{eff} – effective saturation voltage, A_{bulk} – bulk-charge coefficient.

BSIM3 capacitance model uses unified charge based model, corresponding to the Ward-Dutton model [16]. It avoids the discontinuities at threshold and at saturation of the earlier models BSIM1 and BSIM2. The transition to saturation is defined in terms of two voltages, one corresponding to the velocity saturation voltage, and the other closer to the long-channel pinch-off voltage.

BSIM4 is the latest addition to the BSIM family (2000). Many improvements are made over BSIM3 in *I-V* modeling of the intrinsic transistor, noise modeling, extrinsic parasitics, quantum charge thickness, gate tunneling current, holistic thermal noise, substrate resistance, etc. The quantum mechanical model accounts for the finite inversion/accumulation layer thickness and significantly improves the accuracy of the *C-V* characteristic [14].

The difference between physical ($t_{ox,ph}$) and electrical oxide ($t_{ox,e}$) thicknesses is accounted into the BSIM4 drain current equation: its form is identical with the BSIM3's (Eq. (7)) but the expression for the $I_{DS,0}$ is changed [7]:

$$I_{DS,0} = \frac{W_{eff}\mu_{eff}C_{ox}'^{eff}V_{GST}^{eff}}{L_{eff}\left[1+\frac{V_{DS}^{eff}}{\varepsilon_{sat}L_{eff}}\right]}\left[1-\frac{A_{bulk}V_{DS,eff}}{2\left(V_{GST}^{eff}+2\frac{kT}{q}\right)}\right]V_{DS}^{eff} \quad (9)$$

BSIM4 has improved its intrinsic channel resistance model together with the addition of electrode resistances. In addition, BSIM4 fixes the asymmetry problem of previous BSIM models, by introducing a dynamic reference approach.

MOS MODEL 9 (MM9) is developed by Philips Semiconductors. The model equations are very clean and simple. To achieve continuity in device characteristics, smoothing functions are used. The number of parameters is about 50 [17].

MOS MODEL 11 (MM11) (2000) includes physical phenomena such as mobility reduction, bias-dependent series resistance, velocity saturation, conductance effects (CLM, DIBL, etc.), gate leakage current, gate-induced drain leakage, gate depletion, quantum-mechanical effects, etc. [18]. MM11 is a surface-potential-based model that also utilizes smoothing function to the *I-V* characteristic [17].

EKV MODEL is developed at the Swiss Federal Institute of Technology in Lausanne (EPFL). The most popular version EKV v2.6 (1997) is a scalable, charge-based model. It adopts a physical model that exploits the inherent symmetry of the device by referring all the voltages to the bulk. In 2000 EKV v3.0 has been announced.

The current in moderate inversion region is modeled by an appropriate interpolation function resulting in a continuous expression valid from weak to strong inversion. I_{DS} is normalized through a specific current I_S:

$$I_{DS} = I_F - I_R = I_S(i_f - i_r) \equiv 2n\beta\varphi_T^2(i_f - i_r) \quad (10)$$

where i_f and i_r are the normalized forward and reverse currents, n is the electron concentration and $\varphi_T = kT/q$ is the thermal voltage [4].

SP2001 model, developed at The Pennsylvania State University (2001) uses the bulk as a voltage reference and thence it is symmetric to source-drain interchange. Provides accurate and continuous description of all the regions of interest (that are physically modeled) [19], [20]. SP2001 requires up to 28 parameters; if scaling is included the parameter number rises to 68 of which only 35 are needed for a typical/mature fabrication process.

SP proceeds from Brews' charge-sheet model [21] and employs analytical computation of the surface potential (ϕ_s) [22]. The drain current is

$$I_{DS} = \beta\frac{(q_{im}+\alpha\phi_t)\phi}{r_L+\delta_0\phi/V_c} \quad (11)$$

where $\beta = \mu(W/L)C_{ox}$ is the gain factor, q_{in} is the inversion charge, and α, V_c, r_L, δ_0 — parameters

Models Outlook

The most challenging task to device models is the high accuracy fitting of device data from different technologies. It is an essential feature of an industrial "standard" model and represents the final test of the practicality of the model. However, the quality of fitting is not the only criterion for choosing the right model. Ease of parameter extraction, correlation of parameters, number of parameters, redundancy of parameters, etc. should also be considered.

The first generation models are nowadays obsolete. However, they can still be of use. Level 1 model is too approximated with the number of fitting parameters too small (just 5). As such it is good in quick and rough estimate of the circuit performance. The benefit from Level 2 is small. Level 3 has higher accuracy and requires less time for calculations.

Contemporary models such as BSIM3v3 and MM9 are based on the threshold voltage formulation. A disadvantage of this approach is that it makes use of approximate expressions of the channel current (I_{DS}) in weak-inversion region (i.e. subthreshold) and in strong inversion region. These approximate equations are tied together using a mathematical smoothing function, resulting in neither a physical nor an accurate description of I_{DS} in the moderate inversion region (i.e. around the threshold). Besides, lots of nonphysical parameters are introduced to allow adjustment of simulated characteristics.

To increase the physical content, especially in the moderate inversion region, the model development shifted from threshold-voltage-based models (V_{Th}-models) to charge sheet models based on the surface potential formulation (ϕ_s-models). These physics-based models allow an inherently single-piece and accurate calculation of the drain current. The relatively small number of the fitting parameters is a consequence of the increased physical content of the model. However, a major drawback of the ϕs-models is that the surface potential is formulated by an implicit relation and thus, requires an iterative solution.

The recent progress in the development of ϕs-based models overcomes the problem with iterative solutions and devaluates the historical advantages of simpler model (V_{Th}-based) structures. Different analytical solutions have been proposed in models like MM11 and SP2001. SP2001 model [19] proposes new closed-form analytical approximation for ϕs based on symmetric linearization method.

Conclusion

With feature sizes ranging from 180 to 90 nm, today's very deep submicron technologies pose new modeling challenges including power dissipation, leakage management, short channel effects in deep submicron transistors, increasing capacitive and inductive noise in interconnect and platform integration issues. With this regard device models are constantly developed, elaborated and refined to achieve best description and prediction of the downscaling devices. Deep understanding of the underlying physical phenomena is required as well as competent use of mathematical techniques to settle efficient and accurate modeling methodologies that encompass constantly downscaling technologies. Now a huge emphasis is placed on obtaining physics-based, simple and highly accurate analytical device models.

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