MOSFET Models at the Edge of 100-nm Sizes

George Angelov, Tihomir Takov, and Stojan Ristic

Abstract — The paper reviews the mainstream MOSFET advanced models with their physical relevance and mathematical techniques. The basics of the respective modeling approaches are discussed showing the principle advantages of the surface potential based approach for describing sub-100-nm devices. Major short-channel and quantum effects in the models are outlined. Emphasis is set upon the latest compact models: BSIM3/4, MOS Models 9/11, EKV, SP2001. Selected characteristics (such as inversion model basis, core reference, drain current and threshold voltage equations, short-channel and quantum effects, number of model parameters) of the models examined are compared as well as comments on model virtues and shortcomings are given.

I. INTRODUCTION

A model is a mental image of reality – many different images of the same reality may exist. The fundamental goal in device modeling is to describe the intrinsic physical and electrical properties of the device modeled (for the MOSFET such are charge conservation, source-to-drain symmetry, etc.). The growing demand for accurate modeling is determined by the requirement for a sufficient simulation accuracy and applicability for any technology. The technology trend towards downscaling of MOSFETs into the sub-100-nm sizes, low voltages, high frequencies, and system integration on chip brings device physics and modeling before new challenges. Silicon MOSFETs will continue to scale down for some time, but the physical limits of scaling are coming closer. The sub-100-nm regime of operation is increasingly affected by various quantum and short-channel effects. They restrict and even compromise the operation of conventional MOSFETs, based on the drift and diffusion motions of electrons. Adequate modeling of geometry-reduced devices is becoming more complex as technology scales into sub-100-nm dimensions.

II. MODELING AT THE 100-NM SIZES

MOSFET compact models must account for the changes observed in the device characteristics. They need to be physical, simple (compact), accurate, and technology independent. Fitting of device data from different technologies across the industry with high accuracy is the most challenging task. Models like BSIM3/4 achieve it by introducing lots of fitting parameters to adjust the simulated characteristics. This has led to a trend, similar to Moore's law, of increasing the number of model parameters along with model complexity (Figure 1).

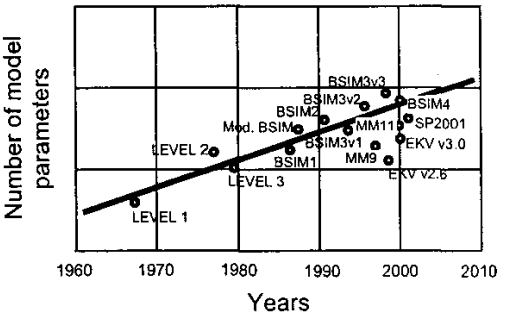

Fig 1. Number of DC model parameters vs. the year of the model introduction.

State-of-the-art MOS technology is in deep submicron sizes (0.13 μm, 100 nm). These sizes affect the device operation and directly reflect device models complexity, causing numbers of physical, mathematical and computational problems. All deep submicron MOSFETs suffer the conventional short-channel effects: channel-length modulation (CLM), carrier velocity saturation, drain-induced-barrier lowering (DIBL), reverse short-channel (RSC) effect, substrate current induced body effect (SCBE), etc. When MOSFET dimensions are scaled down, both the voltage level and the gate oxide thickness must also be reduced. Since the electron thermal voltage (kT/q) is constant for room-temperature electronics, the ratio between the operating voltage and the thermal voltage shrinks. This leads to higher source-to-drain leakage currents stemming from the thermal diffusion of electrons. Simultaneously, the gate oxide thickness has been scaled down to a few atomic layers, where quantum tunneling gives rise to a sharp increase in gate leakage current. Moreover, the use of highly doped channel and polysilicon gate, leads to depletion in the poly-Si gate (polydepletion) and quantization effects in the channel. Polydepletion occurs after entering strong inversion in the bulk silicon. Quantum effects (QM) relate to the emergence of quantized carrier states in the inversion layer. The principal outcome of their presence is that the peak of the carrier density distribution is shifted away from the surface, which is not the case for its classical counterpart.

G. Angelov and T. Takov are with the Dept. of Microelectronics, Faculty of Electronic Engineering and Technology, Technical University of Sofia, Kl. Ohridski 8, 1797 Sofia, Bulgaria.
e-mail: gva@ecad.tu-sofia.bg, tihomirtakov@yahoo.com

Stojan Ristic is with the Faculty of Electronic Engineering, University of Nis, Beogradska 14, 18000 Nis, Serbia and Monte Negro. e-mail: sristic@elfak.ni.ac.yu

0-7803-8166-1/04/$17.00 © 2004 IEEE

III. Modeling Approaches

The basic equations for describing the MOS device characteristics are the Poisson's equation, the continuity equations, and the current-density equations [1]. The three well-known approaches to modeling MOS devices [2] are examined below.

III.1. Regional Approach

Regional models describe MOSFET operation in the linear and saturation regions with separate equations under the drift approximation. They use bulk and inversion charge linearization, whereat symmetry between source and drain is lost. The transistor channel current takes the following simplified form

$$I_{DS}=\begin{cases} KP\dfrac{W}{L}\left[(V_{GS}-V_{Th})-\dfrac{1}{2}(1+\delta)V_{DS}\right]V_{DS}\,, & V_{DS}<V_{DS}^{\text{sat}} \\ KP\dfrac{W}{L}\dfrac{(V_{GS}-V_{Th})^2}{2(1+\delta)}, & V_{DS}\geq V_{DS}^{\text{sat}} \end{cases}, \quad (1)$$

KP – transconductance parameter, V_{Th} – threshold voltage and δ – bulk-charge factor accounting for the amount of the bulk charge variation with the channel-to-bulk bias.

A fundamental problem is the discontinuity of d^2I_{DS}/dV_{DS}^2 at V_{DS}^{sat}. To ensure numerical robustness, the derivatives of second higher orders must be continuous at all voltages. A single, continuous equation of I_{DS} is achieved by introducing a *smoothing function* to interpolate the *I-V* characteristic between linear and saturation regions. The smoothing function – effective drain-to-source voltage V_{DS}^{eff} – is defined (in BSIM3) as [3]:

$$V_{DS}^{\text{eff}}=V_{DS}^{\text{sat}}-\frac{1}{2}\left(V_{DS}^{\text{sat}}-V_{DS}-\Delta+\sqrt{(V_{DS}^{\text{sat}}-V_{DS}-\Delta)^2+4\Delta V_{DS}^{\text{sat}}}\right). \quad (2)$$

The value of Δ (it is a BSIM3 model parameter) determines the smoothness of transition. Substituting V_{DS} in **(1)** with V_{DS}^{eff} from **(2)**, we obtain the single equation of I_{DS}:

$$I_{DS}=KP\frac{W}{L}\left[(V_{GS}-V_{Th})-\frac{1}{2}(1+\delta)V_{DS}^{\text{eff}}\right]V_{DS}^{\text{eff}}\,. \quad (3)$$

Regional models have moderately simple implementation into simulation tools and are widely present in public domain (BSIM3/4, MM9). A key advantage is that model equations are explicit functions of applied voltages. A disadvantage is the use approximate expressions of I_{DS} in the weak- and strong-inversion regions, tied together by smoothing functions. A big number of parameters is introduced for smoothing and to add new effects. The result is an inaccurate description of the channel current in moderate inversion, which becomes increasingly important in modern analog and RF designs. Such artificial modeling is insufficient for sub-100-nm technologies, where process variations must be accounted for to ensure reliability of circuit simulations. Next generation modeling approaches should provide a simpler way of implementing new features.

III.2. Surface Potential Based Approach

To enlarge the physical content, model developments focus on charge sheet models based on surface potential (ϕ_s) formulation. These models allow an inherently single equation and accurate calculation of I_{DS}. At the core of the ϕ_s-based approach is the drift-diffusion approximation of I_{DS}; under the Brews charge-sheet approximation [4]:

$$I_{DS}=\mu\frac{W_{eff}}{L_{eff}}\left\{\begin{array}{l} C_{ox}\left((V_{GS}-V_{FB})(\phi_{sL}-\phi_{s0})-\dfrac{1}{2}\left(\phi_{sL}^2-\phi_{s0}^2\right)\right) \\ -\dfrac{1}{3}qN_AL_D2^{\frac{3}{2}}\left[(\beta\phi_{sL}-1)^{\frac{3}{2}}-(\beta\phi_{s0}-1)^{\frac{3}{2}}\right] \\ +qN_AL_D2^{\frac{1}{2}}\left[(\beta\phi_{sL}-1)^{\frac{1}{2}}-(\beta\phi_{s0}-1)^{\frac{1}{2}}\right] \end{array}\right\} \quad (4)$$

Eq. **(4)** is continuous in all bias conditions. The surface potentials at the source (ϕ_{s0}) and drain side (ϕ_{sL}) are the key quantities calculated by iteratively solving the Poisson equation. Under strong inversion condition $\phi_{s0}\approx 2\phi_F$ and $\phi_{sL}\approx 2\phi_F+V_{DS}$, which greatly simplifies **(4)** (ϕ_F is the Fermi potential). All transistor characteristics are described as functions of ϕ_{s0} and ϕ_{sL}. The discontinuities are eliminated without introducing smoothing parameters. Therefore, ϕ_s-models are simple and comprehensible. They give most accurate results. The major disadvantage is the need for iterative procedures to compute ϕ_{s0} and ϕ_{sL} as functions of applied voltages (no analytical solution). Another drawback is the relatively complex implementation and slow execution time. The recent progress of ϕ_s-based models, however, overcomes these difficulties (e.g. MM11 [5], [6] and SP2001 [7]), indicating that ϕ_s-models could serve as basis for the sub-100 nm compact models.

III.3. Hybrid Approach

An alternative to purely ϕ_s-models is the hybrid approach that combines the advantages of both presented approaches. The surface potential at the source side is usually described analytically, and the drain side potential is approximated by V_{DS}^{sat}, given by a definition analogous to **(2)**. The EKV model adopts such method of introduction of empirical mathematical formulations [8], [9], [10], [11].

IV. Advanced MOSFET Models

IV.1. BSIM3, BSIM4, and MM9

BSIM3 (**B**erkeley **S**hort-Channel **I**GFET **M**odel), developed at the University of California at Berkley, emphasizes physical formulation, computational efficiency and ability to accommodate a large variety of technologies. BSIM3 features include major high-field and short-channel effects: velocity saturation, CLM, DIBL, SCBE, RSC effect, subthreshold current, parasitic resistance effects. BSIM3v3 (1995-1998) is the most recent release [12].

BSIM4 (2000) improves *I-V* modeling of the intrinsic transistor, noise modeling; incorporates extrinsic parasitics, etc. It maintains compatibility with BSIM3v3 while introducing several advanced effects to cope with the rapidly shrinking MOSFETs: QM charge thickness model, gate tunneling current model, holistic thermal noise model, substrate resistance model, etc. To fix the asymmetry problem, a dynamic reference approach is introduced [12].

BSIM3 threshold voltage is approximated by

$$V_{Th} = V_{Th0} + K1\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right) + \\ + K2 \cdot V_{SB} + K1\left(\sqrt{1+\frac{NLX}{L_{eff}}} - 1\right)\sqrt{2\phi_F} - \Delta V_{Th} \quad (5)$$

V_{Th0} – long-channel threshold voltage at zero V_{SB}, $K1$, $K2$ – body effects coefficients, NLX – RSC coeff., ΔV_{Th} – the threshold voltage reduction due to short-channel effects. For full exact listing of BSIM3 equations see [3], [13].

BSIM3 and BSIM4 use the same general form of I_{DS}:

$$I_{DS} = \frac{I_{DS,0}}{1+\frac{R_{DS} I_{DS,0}}{V_{DS}^{\text{eff}}}}\left(1+\frac{V_{DS}-V_{DS}^{\text{eff}}}{V_A}\right). \quad (6)$$

In BSIM3 $I_{DS,0}$ is [3]:

$$I_{DS,0} = \frac{W_{eff}\mu_{eff}C'_{ox}V_{GST}^{\text{eff}}}{L_{eff}\left[1+\frac{V_{DS}^{\text{eff}}}{\varepsilon_{sat}L_{eff}}\right]}\left[1-\frac{A_{bulk}V_{DS,eff}}{2\left(V_{GST}^{\text{eff}}+2\frac{kT}{q}\right)}\right]V_{DS}^{\text{eff}}, \quad (7)$$

V_A – Early voltage, V_{DS}^{eff} – smoothing function of V_{DS}, V_{GST}^{eff} – smoothing function of $(V_{GS} - V_{Th})$, C'_{ox} – oxide capacitance per unit area, A_{bulk} – bulk-charge coefficient.

The key difference between BSIM3 and BSIM4 is that in BSIM3 $I_{DS,0}$ is proportional to C'_{ox}, whereas in BSIM4 $I_{DS,0}$ is proportional to $C'_{ox,eff}$. The difference arises out of the two types of gate oxide thickness that are introduced in BSIM4: ① physical thickness ($t_{ox,ph}$) – the actual grown thickness, and ② electrical thickness ($t_{ox,e}$) – the thickness that fits best to the measured data. In classical analysis charges are assumed to concentrate right on the oxide–bulk interface, i.e. $t_{ox,ph} = t_{ox,e}$. In reality, the maximal probability of carrier distribution occurs at some distance below the interface. Basically C'_{ox} in BSIM3 is the BSIM4 electrical capacitance $C'_{ox,e} = \varepsilon_{ox}/t_{ox,e}$ and BSIM4 $C'_{ox,eff}$ is related to the physical thickness $t_{ox,ph}$.

MOS Model 9 (MM9), developed by Philips Semiconductors in the early 1990s, is regional model that also implements smoothing functions to achieve continuity in device characteristics. The model exhibits good behavior in circuit simulations [14].

IV.2. SP2001, MM11, and EKV

SP2001 (surface potential) is developed at the Pennsylvania State University (2001). The model is physics based, symmetric and uses the inherent MOS device symmetry by referring all voltages to the substrate. Provides accurate description of all transistor operation regions with no d^2I_{DS}/dV_{DS}^2 singularity. The QM and polydepletion effects are embedded via ϕ_s-based corrections [7], [15]. SP2001 does not contain iterative loops or channel segmentation. Free from unphysical behavior, the model contains a relatively small number of parameters owing to the increased physical content.

SP2001 proceeds from Brews' charge-sheet model [4] and utilizes analytical computation of ϕ_s via symmetric linearization [16]. Following a small-geometry version of the symmetric linearization concept, the drain current is

$$I_{DS} = \beta\frac{(q_{im}+\alpha\phi_t)\phi}{r_L+\delta_0\phi/V_c}, \quad (8)$$

$\beta = \mu(W/L)C_{ox}$ – gain factor, q_{in} – normalized inversion charge, r_L, α, V_c, δ_0 – parameters.

MOS Model 11 (MM11) (2000) is a symmetrical, ϕ_s-model that employs smoothing function to interpolate the *I-V* characteristic. It includes effects, such as velocity saturation, bias-dependent series resistance, conductance effects (CLM, DIBL, SCBE, etc.), gate leakage current, gate depletion, QM effects, etc. [5], [6], [14].

MM11 channel current is split up in two: $I_{DS} = I_{drift} + I_{diff}$. The drift and diffusion components are functions of the gate bias (V_{GB}) and the surface potential at the source and drain sides. Thus, I_{DS} can be accurately described using one equation for all operating regions. ϕ_s (in the model it is denoted with ψ_s) can be calculated from [14]:

$$\left(\frac{V_{GB}-V_{FB}-\phi_p-\phi_s}{k_0}\right)^2 = \phi_s + \varphi_T\left[\exp\left(\frac{\phi_s}{\varphi_T}\right)-1\right] + \\ \varphi_T\cdot\exp\left(\frac{\phi_B-2\Phi_F}{(1+m_0)\varphi_T}\right)\cdot\left[\exp\left(-\frac{\phi_s}{(1+m_0)\varphi_T}\right)-1\right], \quad (9)$$

where Φ_F – quasi-Fermi potential, $\varphi_T = kT/q$ – thermal voltage, ϕ_B – surface potential in strong inversion, k_0 ($\equiv KP$ in other models), m_0, ϕ_p – parameters. Eq. **(9)** provides an implicit relation of ϕ_s to V_{GB} and Φ_F. So, ϕ_s can only be calculated numerically using an iterative solution. That is why in MM11 an explicit approximation of the surface potential is used.

EKV model, developed at the Swiss Federal Institute of Technology in Lausanne (EPFL), is physics based model that uses bulk as a reference. Though being charge based, the model employs an empirical approach to achieve continuity, which relies on conductances rather than on currents. EKV v2.6 (1997) is continuous model valid for all bias conditions [17]. In 2000, EKV v3.0 has been announced [18].

The current in moderate inversion region is modeled by interpolation function. I_{DS} is normalized through a specific current I_S:

$$I_{DS} = I_F - I_R = I_S(i_f - i_r) \equiv 2n\beta\varphi_T^2(i_f - i_r) \quad (10)$$

i_f, i_r – normalized forward and reverse currents, n – electron concentration [8].

TABLE I
COMPARISON OF THE MOST POPULAR ANALYTICAL COMPACT MODELS

MODEL	Number of parameters	Inversion model	Drain current	Model core reference	Symmetry	QM effects
BSIM3v3	≈ 85 (190*)	V_{Th}-based	Drift	Source	No	Yes
BSIM4	(259*)	V_{Th}-based	Drift	Source	Yes	Yes
MM9	≈ 50 (113*)	V_{Th}-based	Drift	Source	No	No
MM11	≈ 60	ϕ_s-based	Drift & Diff.	Bulk	Yes	Yes
EKV v2.6	27 (41*)	Hybrid	Drift	Bulk	Yes	Yes
EKV v3.0	n.a.	Hybrid	Drift	Bulk	Yes	Yes
SP2001	≈ 35	ϕ_s-based	Drift & Diff.	Bulk	Yes	Yes

* number of parameters in HSPICE (Star-Hspice Manual, Release 2001.2, June 2001, http://www.ece.cmu.edu/~ee762/hspice-docs/)

V. COMPARISON OF THE MODELS

TABLE I presents selected features of the models examined. Comparison of the time needed for parameter extraction between BSIM3, SP2001 and EKV shows the EKV model is the quicker than BSIM3 and SP2001. Parameter extraction on a standard 0.13 mm technology, takes a few hours for EKV, two days for SP2001 and five days for BSIM3 [19]. Such a big difference is due to the fact that BSIM3 model has large number of parameters with strong correlation between many of them while EKV has far fewer parameters with low correlation between them. As far as DC fitting of device data is concerned, SP2001 fits best and BSIM3 fits better than EKV (EKV has fewer parameters than BSIM3). However, BSIM3 model is very sensitive to carefully choosing the model parameters, otherwise it gives erroneous characteristic curves; SP2001 and EKV models are well behaved and have no such problems. BSIM3 suffers from bad intrinsic MOSFET capacitance modeling, which results in non-physical or spurious description in many areas of capacitance behavior; EKV and SP2001 show none of these problems.

It could be judged that EKV is the easiest model to use, SP2001 and MM11 are most physical, and the most popular models – BSIM3v3/4 – are most comprehensive for the mainstream technologies.

VI. CONCLUSION

Scaling down to 100-nm channel lengths, the mainstream MOS technology faces physical limiting factors that worsen the device performance. It is expected that in nanometer designs the process effect on system performance will be larger as the nanotechnology variations will be more significant. Accordingly, much more modeling efforts are needed to comply with the increased design complexity. The goal is to develop physics-based, simple, and accurate MOSFET models and methodologies that make the best use of the available technology while downscaling design margins. A simpler analytical formulation of the surface potential utilizing the drift diffusion approximation proves to be both physical and practical for the near future technologies.

REFERENCES

[1] S.M. Sze, "*Physics of Semiconductor Devices*", Wiley, 1981.

[2] N.D. Arora, "Modeling and characterization of ultra deep submicron CMOS devices," *IEICE Trans. Electron.*, vol. E82-C, pp. 967-975, 1999.

[3] W. Liu, "*MOSFET Models for SPICE Simulation, including BSIM3v3 and BSIM4*", John Wiley & Sons, 2001.

[4] J.R.Brews, "A charge-sheet model of the MOSFET", *Solid-St. Electron*, Vol. 21, pp. 345-355, Feb. 1978.

[5] D.B.M. Klaassen, R. van Langevelde, A.J. Scholten et al., "The MOS model, level 11", Philips Research Laboratories, 2002.

[6] A.J. Scholten, H.J. Tromp et al., "Accurate thermal noise model for deep-submicron CMOS," *IEDM Tech. Dig.* pp. 155–158, Dec. 1999.

[7] T.L. Chen, G. Gildenblat, "Analytical approximation for the MOSFET surface potential", *Solid-State Electronics*, Vol. 45, pp. 335-339, 2001.

[8] C.C. Enz, F. Krummenacher, and E.A. Vittoz, "An analytical MOS transistor model valid in all regions of operation," *Analog Integrated Circuits Signal Process*, vol. 8, pp. 83–114, 1995.

[9] M. Bucher, C. Lallement, C.C. Enz et al., "The EPFL-EKV MOSFET Model, Version 2.6", Technical Report, 1999.

[10] M. Bucher, C.C. Enz, F. Krummenacher et al., "The EKV 3.0 Compact MOS Transistor Model: Accounting for Deep-Submicron Aspects", *Techn. Proc. of the MSM 2002 Inter. Conf.*

[11] C. Lallement, J.M. Sallese, M. Bucher, W. Grabinski, P. Fazan, "Accounting for quantum effects and polysilicon depletion from weak to strong inversion, in a charge based design-oriented MOSFET model", *IEEE Trans. Electron Devices*, 2003.

[12] BSIM Homepage: http://www-device.eecs.berkeley.edu/~bsim3/

[13] D.Foty, "*MOSFET Modeling with SPICE: Principles and Practice*", Prentice-Hall, 1997.

[14] Philips Semiconductors MOS Models: http://www-us.semiconductors.com/Philips_Models/mos_models/

[15] G. Gildenblat, T.L. Chen, "Overview of an Advanced Surface-Potential-Based MOSFET Model", *Technical Proc. of the Fifth International Conference on Modeling and Simulation of Microsystems*, pp. 657-661, 2002 (invited).

[16] T.L.Chen, G.Gildenblat, "Symmetric Bulk Charge Linearization of Charge-Sheet MOSFET Model", *Electronics Letters*, Vol. 37, pp. 791-793, 2001.

[17] M. Bucher, Ch. Lallement, Ch. Enz, F. Theodoloz, Fr. Krummenacher, "The EPFL-EKV MOSFET Model Equations for Simulation", Technical Report, *EPFL-DE-LEG*, 1999.

[18] EPFL-EKV v2.6 MOSFET Model: http://legwww.epfl.ch/ekv/

[19] P. Bendix, "Detailed Comparison of the SP2001, EKV, and BSIM3 Models", *Modeling and Sim. of Microsys.*, 2002.