SPICE MODELS FOR MOSFETS: TOWARDS THE NANOTECHNOLOGY ERA

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Abstract*. The paper follows through the evolution of SPICE models for MOSFETs placing the emphasis upon the latest compact model generation (BSIM3v3, BSIM4, MM11, EKV, SP). The MOSFET models are examined following the trend of shrinking technology sizes, low voltage and low power design. The principles of the mainstream modeling approaches are outlined. Major physical effects arising from technology downscaling towards sub-100-nm and their implementation in the models are addressed. Comparison between models reviewed is provided as well as general comments for model applicability. The prospective directions of model developments have been pointed out*

I. INTRODUCTION

Over the past 30 years the progress in the performance of Si VLSIs has been fueled by the remarkable downscaling of Si device feature sizes to less than 100 nm and their denser integration on a single chip (Fig. 1). Due to these parallel ongoing developments requirements for circuit simulations are rising; accordingly, device modeling is becoming increasingly rigorous. The most important modeling issue is to ensure sufficient simulation accuracy and applicability for any technology. A major modeling goal in the downscaling CMOS VLSI technology is to set up a coherent modeling infrastructure from process through device/circuit to systems level. Finding an optimal tradeoff between model complexity and simulation time is another modeling goal.

In this context the development of physics-based models for circuit simulations that cover geometry, bias, temperature, DC, AC, RF, and noise characteristics becomes a major goal. For achieving this task it is necessary for the physicists, electronic engineers and circuit designers to have a good knowledge of the existing diversity of models and the spurs of their development.

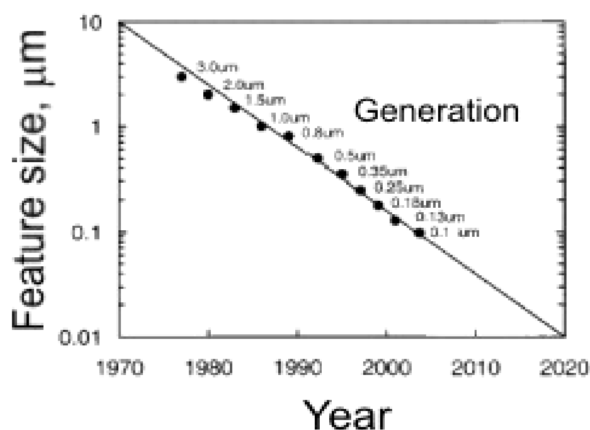

Fig. 1. Technology feature size trend.

II. MOSFET MODELING APPROACHES

MOSFET compact models must account for the changes observed in device characteristics. Models are supposed to be simple (*compact*) and highly accurate. To find an optimal compromise between these contradictory requirements, different approaches are used: regional, surface-potential-based, hybrid.

REGIONAL APPROACH — MOS transistor operation in the linear region and in saturation is described by two separate equations. A fundamental problem of regional models is that though I_D and dI_D/dV_{DS} are continuous at V_{DS}^{sat}, d^2I_D/dV_{DS}^2 is not. Continuity is ensured by means of smoothing functions; besides, a single equation for the drain current is obtained. Model equations are *explicit* functions of applied voltages and have moderately simple implementation into simulation tools. Scalability is improved by binning. Problematic is the large number of nonphysical parameters introduced for smoothing which induce additional parameters. In result, the total number of parameters easily exceeds 150 (BSIM3/4) [1].

SURFACE POTENTIAL BASED APPROACH gives most accurate results with the models valid for all regions of transistor operation. Discontinuities are eliminated without smoothing parameters. The drain current is described with the surface potentials at the source side, ϕ_{s0}, and at the drain side, ϕ_{sL}. They are the key quantities calculated by *iteratively* solving the Poisson equation. A drawback is the need for iterative computation of ϕ_{s0} and ϕ_{sL} as functions of applied voltages (no analytical solution). Additional problem is the relatively complex implementation and slow execution time. However, solutions to overcome these difficulties have been proposed in recent models like MM11 [2], [3] and SP [4].

HYBRID APPROACH combines advantages of both presented approaches. Here the charge linearization method is utilized. The surface potential at the source side is described analytically, and the drain side potential is approximated by V_{DS}^{sat}. The EKV model adopts such method [5], [6], [7].

All MOSFETs downscaled to the sub-100-nm suffer lots of unwanted short-channel and quantum effects: channel-length modulation (CLM), velocity saturation resulting, drain-induced-barrier lowering (DIBL), reverse short-channel (RSC) effect, substrate current induced body effect (SCBE), source-to-drain and gate leakage currents, polydepletion, etc. These effects restrict or even compromise conventional MOSFET operation.

III. THE EVOLUTION OF SPICE MODELS

SPICE is widely adopted tool (a de facto standard) for simulation of electrical circuits. It is made up of two distinct parts: simulator and device models. The simulator is the mathematical instrument for numerical analyses. Device models represent the device in mathematical terms; they are at the core of the simulation program.

Historically SPICE MOSFET models have formed up into three generations. First model generation is comprised of Level 1, Level 2, and Level 3 models that constitute the original release of Berkeley SPICE. They are physically based models, trying to include all geometry dependency in the model equations, rather than focusing on their mathematical representation. Second generation consists of BSIM (**B**erkeley **S**hort-Channel **I**GFET

Model), BSIM2, and modified BSIM. It shifts the focus to circuit simulation and parameter extraction. The equations are subject to extensive mathematical conditioning. Third generation returns to a simpler analytical model structure with reduced number of physically based parameters. Models rely on smoothing functions to obtain single-equations for the *I-V* and *C-V* characteristics and. To third generation belong BSIM3/4, MM9, EKV v2.6 as well as MM11, EKV 3.0, SP and other new models.

o **BSIM3** is a physical model based on a coherent quasi two-dimensional analysis of the MOSFET structure, taking into account the effects of device geometry and process parameters. As such, scalability is inherently incorporated. BSIM3 includes major high-field and short-channel effects: mobility reduction owing to vertical field, carrier velocity saturation, DIBL, CLM, substrate current, SCBE, subthreshold current, parasitic resistance effects. *BSIM3v3* (1995) is the latest physical based, deep submicron model that is applicable to L_{gate} ~ 0.18 μm; its most recent variation is BSIM3v3.2 (1998) [8].

The general form of the drain current equation is given by

(1) $$I_{DS} = \frac{I_{DS,0}}{1 + \frac{R_{DS} I_{DS,0}}{V_{DS}^{\text{eff}}}} \left(1 + \frac{V_{DS} - V_{DS}^{\text{eff}}}{V_A} \right),$$

where V_A is the Early voltage generated by the MOSFET resistance model. $I_{DS,0}$ is

(2) $$I_{DS,0} = \frac{W_{eff} \mu_{eff} C'_{ox} V_{GST}^{\text{eff}}}{L_{eff} \left[1 + \frac{V_{DS}^{\text{eff}}}{\varepsilon_{sat} L_{eff}} \right]} \left[1 - \frac{A_{bulk} V_{DS}^{\text{eff}}}{2 \left(V_{GST}^{\text{eff}} + 2 \frac{kT}{q} \right)} \right] V_{DS}^{\text{eff}},$$

C'_{ox} — oxide capacitance per unit area, V_{DS}^{eff} — effective drain-to-source voltage, V_{GST}^{eff} — effective smoothing function of (V_{GS} – V_{Th}); A_{bulk} is the bulk-charge coefficient.

o **BSIM4** is the latest addition to the BSIM family (2000). Improvements are made in *I-V* modeling of the intrinsic transistor, noise modeling, incorporated are extrinsic parasitics, etc. Includes quantum mechanical (QM) charge thickness model, gate tunneling current model, holistic thermal noise model, substrate resistance model, etc. To fix the asymmetry problem, a dynamic reference approach is introduced [8].

The general drain current equation is the same as in BSIM3 (Eq. (**1**)) with the expression for the $I_{DS,0}$ changed

(3) $$I_{DS,0} = \frac{W_{\text{åôô}} \mu_{\text{åôô}} C'_{ox,eff} V_{GST}^{\text{eff}}}{L_{eff} \left[1 + \frac{V_{DS}^{\text{eff}}}{\varepsilon_{sat} L_{eff}} \right]} \left[1 - \frac{A_{bulk} V_{DS,eff}}{2 \left(V_{GST}^{\text{eff}} + 2 \frac{kT}{q} \right)} \right] V_{DS}^{\text{eff}}$$

The difference is in the effective capacitance per unit area $C'_{ox,\text{eff}}$ which replaces C'_{ox} of Eq. (**2**). Two types of gate oxide thickness are introduced in BSIM4: ① physical oxide thickness ($t_{ox,ph}$) — the actual grown thickness, and ② electrical thickness ($t_{ox,e}$) — the oxide

thickness that fits best to the measured data. This modifies the expression for the overall gate capacitance: $C'_{ox} \to C'_{ox,\mathrm{eff}}$ [1].

- **MOS Model 9** (**MM9**) is a threshold-voltage-based (V_{Th}-based) model with very clean and simple model equations developed by Philips Semiconductors in the early 1990s. To achieve continuity in device characteristics smoothing functions are used. The model exhibits good behavior in all regions of transistor operation. It is intended for use in both digital and analog circuits [9].
- **MOS Model 11** (**MM11**) (2000) is suitable for digital, analog and RF circuit design. It includes all the physical phenomena important in modern and future CMOS technologies, such as mobility reduction, bias-dependent series resistance, velocity saturation, conductance effects (CLM, DIBL, etc.), gate leakage current, gate-induced drain leakage, gate depletion, QM effects, bias-dependent overlap capacitances, etc. [2], [3], [9]. MM11 is a symmetrical, surface-potential-based model that utilizes smoothing function to interpolate the *I-V* characteristic. The channel current is split up in a drift, I_{drift}, and a diffusion, I_{diff}, component, $I_{DS} = I_{drift} + I_{diff}$, which are a function of the gate bias V_{GB} and ϕ_s. The surface potential ϕ_s is implicitly related to the gate bias V_{GB} (Eq. (**4**)) and the quasi-Fermi potential Φ_F, and can only be calculated numerically using an iterative solution, rather than analytically. That is why in MM11 an explicit approximation of the surface potential is used. ϕ_s (in the model it is denoted with ψ_s) can be calculated from [9]

(4) $$\left(\frac{V_{GB} - V_{FB} - \phi_p - \phi_s}{k_0}\right)^2 = \phi_s + \varphi_T\left[\mathrm{e}^{\frac{\phi_s}{\varphi_T}} - 1\right] + \varphi_T \cdot \mathrm{e}^{\frac{\phi_B - 2\Phi_F}{(1+m_0)\varphi_T}} \cdot \left[\mathrm{e}^{-\frac{\phi_s}{(1+m_0)\varphi_T}} - 1\right] ,$$

$\varphi_T = kT/q$ — thermal voltage, ϕ_B — surface potential at the onset of strong inversion, m_0, k_0 (denoted with *KP* in other models), ϕ_p — parameters.

- **EKV model**, developed at the Swiss Federal Institute of Technology in Lausanne (EPFL), adopts a physics-based approach that exploits the inherent symmetry of the device by referring all the voltages to the substrate (not the source). This allows the source and drain to be treated symmetrically. *EKV v2.6* (1997) is a scalable continuous compact model valid for all bias conditions [7]. The model is well suited for statistical circuit simulation and enables the simulation of ultra deep submicron CMOS integrated systems, from DC to RF. In 2000, EKV v3.0 has been announced [10]. The current I_{DS} is normalized through a specific current I_S:

(5) $$I_{DS} = I_F - I_R = I_S(i_f - i_r) \equiv 2n\beta\varphi_T^2(i_f - i_r)$$

i_f, i_r — normalized forward and reverse currents, n — electron concentration.

- **SP** (surface potential) model is a physics-based compact MOSFET model developed at the Pennsylvania State University (2001). It is symmetric and uses substrate as a reference. Provides accurate description of all transistor operating regions with no d^2I_{DS}/dV_{DS}^2 singularity. The QM and polydepletion effects are embedded through ϕ_s-based corrections. The DC, QS and NQS models are consistent as well as the noise models [4], [11]. SP proceeds from Brews' charge-sheet model [12] and employs analytical (*non-iterative*) computation of ϕ_s from

accumulation to inversion via symmetric linearization [13]. Following the *symmetric linearization concept*, the drain current is

(6)
$$I_{DS} = \mu \frac{W}{L} C_{ox} \frac{(q_{im} + \alpha\phi_t)\phi}{r_L + \delta_0 \phi / V_c}$$

q_{in} — normalized inv. charge, ϕ — effective surface potential, r_L, α, V_c, δ_0 — parameters.

IV. COMMENTS ON THE MODELS

Fitting of device data from different technologies across the industry with high accuracy is the most challenging task facing compact models. Models such as BSIM3/4, MM9 are based on V_{Th} formulation. A disadvantage of this approach is the use of approximate expressions of I_{DS} in the weak- and in strong-inversion regions which are tied by a smoothing function. The result is neither physical nor accurate description of I_{DS} in the moderate inversion region which becomes increasingly important in analog and RF design since MOSFETs are typically biased in moderate inversion. To enlarge the physical content, model developments focus on charge sheet models based on ϕ_s formulation. These models allow an inherently single-equation and accurate calculation of I_{DS}. The recent research indicates that ϕ_s-based models could serve as basis for the next sub-100-nm generation of compact models.

Table 1. Comparison of the Fist and Second generation models.

Model	**Year**	**Number of parameters**		**Applicable to L_{gate}**
		HSPICE (†)	SPICE3 (‡)	
Level 1	1972	5	n.a.	L_{gate} > 10 μm
Level 2	1976	20 (7 basic)	n.a.	L_{gate} ~ 10 μm
Level 3	1978	22 (6 basic)	42	L_{gate} ~ 2 μm
BSIM1	1985	97 (10 basic)	77	L_{gate} ~ 1.0 μm
BSIM2	1990	92	133	L_{gate} ~ 0.2 μm
Mod. BSIM	n.a.	93	n.a.	L_{gate} ~ 0.3 – 0.5 μm

(†) Star-Hspice Manual, Release 2001.2, June 2001, http://www.ece.cmu.edu/~ee762/hspice-docs/
(‡) SPICE3 User Guide, http://newton.ex.ac.uk/teaching/CDHW/Electronics2/userguide/

Table 2. Comparison of the most popular analytical compact models.

MODEL	**Num. of param.**	**Inversion model**	**Drain current**	**Model core ref.**	**Sym-metry**	**Quantum effects**
BSIM3	≈ 85 (190*)	V_{Th}-based	Drift	Source	No	Yes
BSIM4	(259*)	V_{Th}-based	Drift	Source	Yes	Yes
MM9	≈ 50 (113*)	V_{Th}-based	Drift	Source	No	No
MM11	≈ 60	ϕ_s-based	Drift&Diff.	Bulk	Yes	Yes
EKV v2.6	27 (41*)	Hybrid	Drift	Bulk	Yes	Yes
EKV v3.0	n.a.	Hybrid	Drift	Bulk	Yes	Yes
SP2001	≈ 30	ϕ_s-based	Drift&Diff.	Bulk	Yes	Yes

* number of parameters in HSPICE

Comparison of the three generation models is presented in Table 1 and Table 2. The major industry models today are BSIM 3v3/4, MM9/11, and EKV v2.6. The most popular model, BSIM3v3, is an advanced submicron model that emphasizes physical formulation, computational efficiency and ability to accommodate a variety of technologies. Philips MM9 and MM11 are the primary non-Berkeley models available for public use. EKV v2.6 is oriented towards use in low-voltage, low-power analog and mixed design and simulation with very small number of parameters. SP2001 is a promising ϕ_s-based model that does not contain iterative loops. It is free from unphysical behavior and contains a relatively small number of parameters owing to the increased physical content of the model.

V. CONCLUSION

Deep submicron and sub-100-nm MOSFETs need much more modeling efforts to comply with the increased design complexity. In the nanometer VLSI era, conventional approaches to circuit design and modeling have to be revised and modified. The major effort is focused on the development of physics-based, simple and highly accurate models and methodologies that make the best use of the available technology while downscaling design margins. Efforts are being made to add all kinds of nanometer effects to the state-of-the-art models and implement them in the major commercial simulators. This is, however, a nontrivial task due to the complexity of the problems as well as the maturity of existing simulators and device models.

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