Methods and Techniques for real-time audio data streaming to and from high capacity local DSP SDRAM memory

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Abstract - **One of the most popular tasks for DSP performance is digital audio processing. This task requires a real-time data streaming to and from internal for DSP architecture high capacity memory. The quality of streaming is important for audio quality at all. At present, much special purpose, integral circuits named CODECs are used for analog-to-digital and digital-to-analog conversion of stereo audio signal to serial synchronous digital interface.**

Keywords – **DSP, Codec, SHARC, Blackfin, UDA1380**

I. INTRODUCTION

The real time processing requires well designed and supported by software dual-direction data transfer of audio types of serial data to and from high capacity RAM. In most applications, this type of RAM is located internally in the DSP. The size of internal memory is limited by the application code size that is located in the same memory space. For many applications, such as Active Noise Control and Audio Effects Generator, a larger quantity of memory is required. In these applications, an external SDRAM device is suitable for temporary saving of large capacity audio data. This paper describes and compares two types of DSP architectures especially designed for digital audio processing using external SDRAM.

II. REAL-TIME AUDIO DATA TRANSFER TECHNIQUE

The suitable parameters settings of the audio codec are initialized by the DSP trough an I^2C interface once after the power is turned on according initialization procedure. The real time audio data can be streamed via DSPs-SPORT →DMA→EMI→SDRAM.

The fig.1 and fig.3 describe a streaming method of data path organization scheme in two types of DSP architectures. All of these peripheral devices must also be initialized in start-up procedure, but some of their parameters need to be updated after the complete of every single transfer. The main device that is used is

The SPORT is a dual channel synchronous serial port, which is used for serial data transfer (with I^2S interface).

The DMA is direct memory access system, used for high-speed data transfer between external peripheral devices and system memory without processor core. The memory can be located internally or externally. In case of external memory location such as SDRAM, the throughput of data must be organized via EMI-external memory interface.

Each SPORT in the DSP processor has two single direction channels for transmitting and receiving simultaneously via Tx and Rx data signals respectively. Each of these channels has particular TxCLK, RxCLK timing signals for bit-level synchronous data transfer. The additional signals -TxF and RxF are frame synchronization signals, which have two states – one for working with each channel.Thus the synchronization is on two levels - level bit and level package (frame).

For BF516, for digital audio processing the processor's serial port SPORT H is used. Fig.1 shows the path of serial data to and from DSP BF516. Fig.2 shows how the PORT H is connected to the Codec UDA1380. PORT H has two sets of independent transmit and receive pins, which enable eight channels of I^2S stereo audio.To realize two-way exchange of data between the codec and CPU serial port is used - SPORT H, which is a duplex that has the capability for simultaneous data transmission in both directions.

In case of SHARC processors, the data path (shown in fig.3) has same additional components: the codec is connected to the DAI (Digital Audio Interface) pins – for streaming and to the DPI (Digital Peripheral Interface) pins – for initialization. Each of these devices has an interrupt controller and a SRU - the signal routing unit assigns each pin to which the codec is connected the required function and direction of data transfer. SRU routs the data streaming thus forming the data path: UDA1380→DAI → DMA controller→SDRAM and vice versa. SRU2 – the initialization trough the TWI - fig.4 shows the connections between the DSP and the UDA1380 Codec. The DAI, the DPI and the DMA can cause an interrupt to occur.

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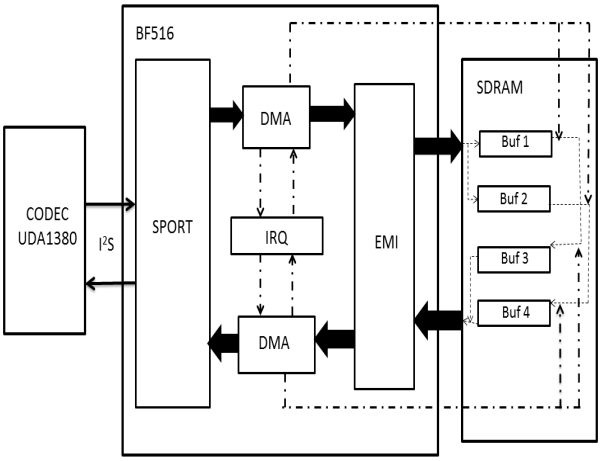


FIGURE 1. AUDIO DATA PATH FROM CODEC TO SDRAM VIA BLACKFIN PROCESSOR BF516

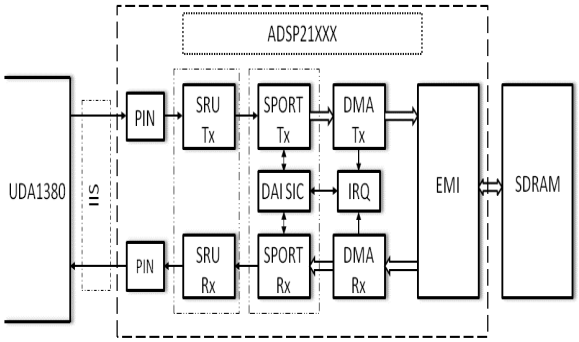


FIGURE 3. AUDIO DATA PATH FROM CODEC TO SDRAM VIA SHARC PROCESSOR ADSP-21489

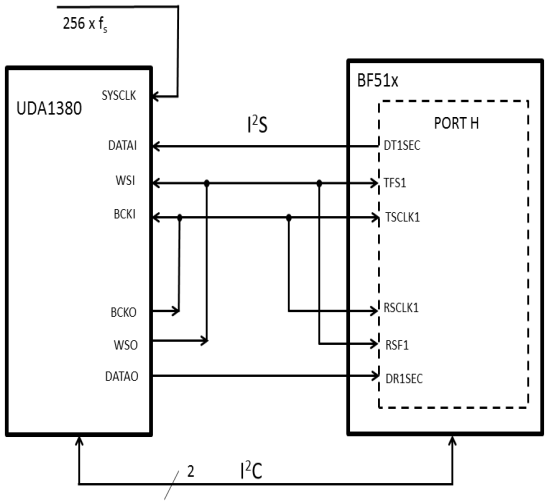


FIGURE. 2. EXTERNAL CONNECTION FOR AUDIO DATA PATH FROM CODEC TO BLACKFIN PROCESSOR BF516 FOR CONTROL AND DATA.

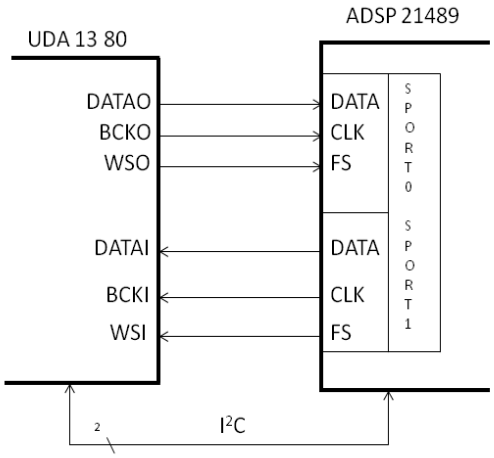


FIGURE. 4. EXTERNAL CONNECTION FOR AUDIO DATA PATH FROM CODEC TO SHARC PROCESSOR ADSP-21489 FOR CONTROL AND DATA.

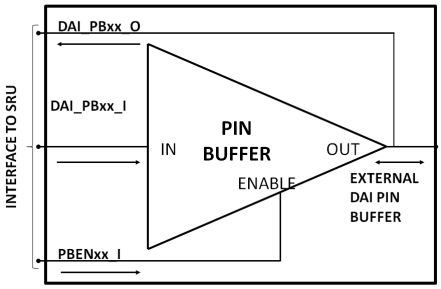
DSP PROCESSORS		BLACKFIN ADSP-BF516	SHARC ADSP-21489	
PIN	Program direction	GPIO	programmable	
	Program function	FIXED	programmable	
	Pull up / down	Only external	IPU/D - programmable	
PIN – To – Port Matrix	Program direction	-	programmable	
	Program signal	-	programmable	
	Rout signal	-	programmable	
	Logical constant	-	yes	
Serial Port	Signals PORT H (GPIO and Multiplexed Peripherals)	DTxPRI - Transmit Data Primary DTxSEC -Transmit Data Secondary TSCLKx -Transmit Clock TFSx -Transmit Frame Sync DRxPRI -Receive Data Primary DRxSEC - Receive Data Secondary RSCLKx - Receive Clock RFSx - Receive Frame Sync	SPORT7–0_CLK_I/O – Transmit/Receive Serial Clock SPORT7–0_FS_I/O – Transmit/Receive Frame Sync SPORT7–0_DA(DB)_I – Data receive channel A(B) SPORT7–0_DA(DB)_O – Data transmit channel A(B)	
	Audio Streaming Modes	1. Standard DSP serial mode 2. Multichannel (TDM) mode 3. I^2S mode 4. Packed I^2S mode 5. Left-justified mode	1. Standard DSP serial mode 2. Multichannel (TDM) mode 3. I^2S mode 4. Packed I^2S mode 5. Left-justified mode	
	Data width	1. 3-32 bits per channel 2. Channel : 0-15 Range of words : 8 -128 3. 3-32 bits per channel 4. 16 bits words 5. 3-32 bits per channel	1. 3-32 bits per channel 2. 3-32 bits per channel, up to 128 channels 3. 8-32 bits per channel 4. 3-32 bits 5. 3-32 bits per channel	
DMA + IRQ	Interrupt Vector	Fixed Program * Core interrupt (CEC have 3 register – ILAT ,MASK,IPEND) System interrupt Peripheral interrupt	Fixed Program * Core interrupt DAI/DPI interrupt System interrupt	
	Audio Buffer Modes	Linear Circular 1-D 2-D L/R	1. Standard 2. Chained (a set of multiple DMA operations, each autoinitializing the next in line; the IOP automatically loads new parameters from memory location, pointed by thet channel's chain pointer register) 3. Ping-pong (in this mode, the parameters have two memory index values – A and B ; the DMA starts the transfer with the memory indexed by A,when it is done as per the value in the count register, the DMA restarts with the memory location indexed by B) 4. Circular	
	IRQ Modes	Single Auto	Single Auto	
	Left / Right Audio Frame / Defame features	Frame sync Bit clock Word frame (L/R , L/L , R/R) by external clock	Frame sync Bit clock Word frame by rising edge of external clock	

TABLE 1. MAIN FEATURES OF BLACKFIN AND SHARC PROCESSORS FOR AUDIO STREAMING APPLICATIONS.

III. Figures and Tables

Figure 1 describes a data path for audio streaming technology to and from SDRAM, organized in Blackfin ADSP-BF516 processor.

Figure 2 describes external connections for CODEC UDA1380 to SPORT of BF516. There are two types of interfaces. The first one is TWI interface (compatible with I^2C) for control and status only. The second one is 4-wires I^2S interface for serial real-time data streaming transfer of audio data.

Figure 3 describes a data path for audio streaming technology to and from SDRAM, organized in SHARC ADSP-21489 processor. An additional SRU can be seen.

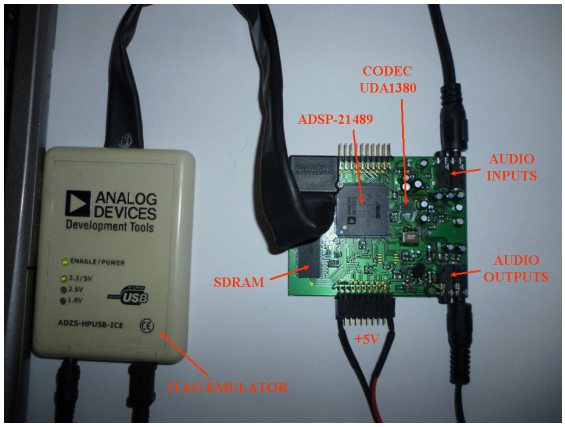
Figure 4 describes external connections for CODEC UDA1380 to SPORT of BF516. There are two types of interfaces. The first one is TWI interface (compatible with I^2C) for control and status only. The second one is 6-wires I^2S interface for serial real-time data streaming transfer of audio data.

Table 1 describes differences between audio transfer features of two types of DSP processors. The more flexibility of SHARC ADSP21489, based on SRU and DAI, can be seen. The additional benefits of this processors is

IV. Experimental Work

The two different modules based on the same codec UDA1380 are used for testing of methods for audio streaming via two processors to SDRAM memory. Figure 5 shows DSP module, based on ADSP-21489 and figure 6 shows DSP module, based on ADSP-BF516.

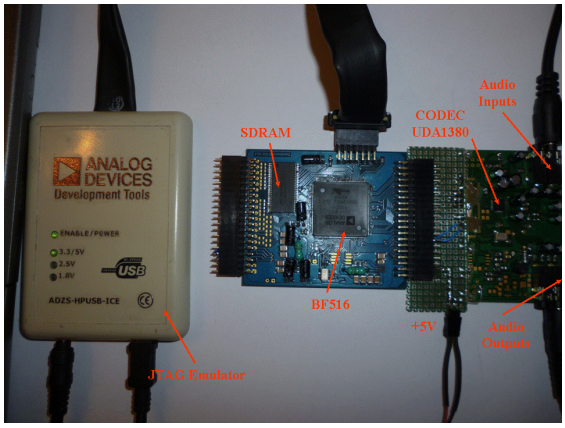
Figure 5. DSP module, based on ADSP-21489 for audio applications.



For two different processors, the same functions are written:

1. PLL_init - Initialization of internal PLL system for the core and peripheral clocking.
2. SDRAM_init - Initialization of EMI and internal SDRAM controller for program and DMA access to the external SDRAM.

Figure 6. DSP Module, based on ADSP-BF516 for audio applications.



3. UDA_init - Function for initialization of internal registers of UDA1380 accessible via TWI interface.
4. SPORT_init - Initialization of SPORT for I^2S mode, 16-bit per left and right audio data, external frame and clock synchronization from codec.
5. DMA_init - Initialization of DMA systems for data transfer to and from codec and system memory. The pointers of buffers are located in external SDRAM.
6. IRQ_init - Initialization of IRQ system for end-of-buffer interrupt event. The two buffers for in-data and two buffers for out-data are set alternatively in every IRQ event.

After execution of all procedures, the uninterruptible audio signal from audio input to audio outputs can be seen.

V. Conclusion

The two types of DSP processors are hardware optimized for audio streaming operation. The ADSP-21489 is more flexible according audio buffer support features. The additional benefits of ADSP-21489 are more then one SPORT that can be used for audio streaming simultaneously.

References

http://www.analog.com/en/processors-dsp/sharc/adsp-21489/products/product.html

http://www.analog.com/en/processors-dsp/blackfin/adsp-bf516/products/product.html

http://www.nxp.com/documents/data_sheet/UDA1380.pdf