Thermal Analysis of ESD Diode in FDSOI Technology using COMSOL Multiphysics

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Abstract – **Device simulators are well-established tools for behavior prediction of novel electronic structures. However, the developing process for electrostatic discharge (ESD) devices strongly relies on tape-out measurements and adjustments on well-known IPs, rather than on pure TCAD simulation results. Part of the reasons are concerns over accuracy when fast transient events are simulated and high temperatures are reached. This paper provides data on thermal analysis of ESD diode characteristics in fully depleted silicon on insulator (FDSOI) technology using an unorthodox simulation tool – COMSOL Multiphysics.**

Keywords – **COMSOL, ESD protection, Electrostatic discharge, FDSOI, thermal analysis.**

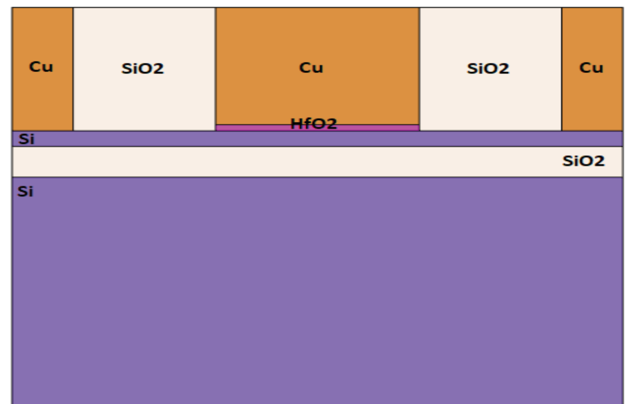
I. Introduction

FDSOI has emerged as superior successor to partially depleted SOI (PDSOI) technology. The reduced thickness of the thin silicon film matches the depth of the depletion zone and thus eliminates kink effect. It also provides great improvement on leakage currents and parasitic capacitance characteristics of the devices. Therefore, FDSOI is often implemented in applications where ultra-low power consumption and relatively high performance is required [1].

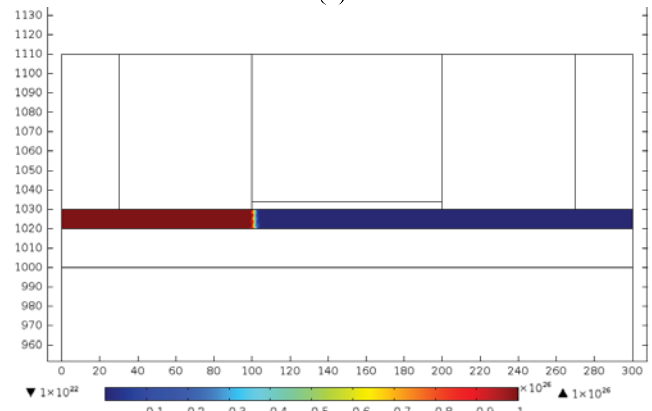
The thin silicon film is susceptible to local thermal heating generated in the channel due to the low thermal conductivity *k* of the buried oxide (BOX). From ESD perspective, this temperature increasement significantly degrade the maximum amount of current (It2) that the protection device can withstand. Therefore, efforts and researches has been made towards improving the heat dissipation capabilities of such structures – reducing BOX thickness, using SiO_2 replacement materials with higher *k*-value, altering terminal geometry, etc [2].

II. Device Structure

The device structure of interest is a gated ESD PIN diode. Fig. 1 shows basic cross-section of the device design and device doping profiles. In order to compare the simulation results obtained by COMSOL to an industry established TCAD simulator and draw conclusions, the geometry, material properties and doping levels are selected to match the results reported in [2]. The 2D model consist of Cu for anode, cathode and gate terminals, HfO_2 as thin dielectric layer beneath the gate, SiO_2 for BOX and STI and Si for active and substrate domains.



(a)



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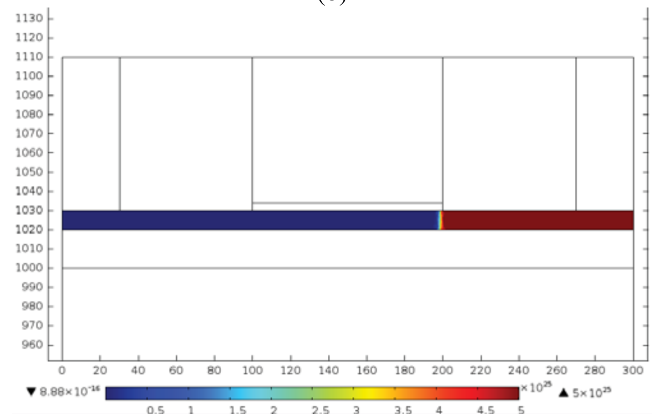

(c)

Fig. 1 (a) Basic schematic of PIN diode and used materials (b) acceptor's concentration [1/m^3] (c) donor's concentration [1/m^3].

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III. SIMULATION SETUP

COMSOL Multiphysics is a comprehensive simulation software environment for a wide array of applications. Available physics are structured in modules, which allows the user to create a simplified single physics model or an experimental design accounting for many different effects. The simulation setup described in this paper includes the *Semiconductor (semi)* and *Heat transfer in solids (ht)* modules.

The semiconductor node is set to use Fermi-Dirac carrier statistics since for high doping levels electrons are described as fermions, which obey Pauli exclusion principle. Also, bandgap narrowing effect is included using Jain-Roulston model. Again, this is due to high impurity concentrations, which reduces the distance between atoms of dopants and thus forming conduction band of their own. All donors and acceptors are assumed to be fully ionized at room temperature. Impact ionization generation and trap-assisted recombination using Shockley-Read-Hall model mechanisms are added. Semiconductor module is solving only for active diode region.

Heat transfer in solids node is used for all design domains, thus the thermal energy produced by the active domain can propagate throughout the entire structure. Left and right vertical walls are set to be thermally isolated, whereas top and bottom boundaries of the model are anchored at 300 K. Initial temperature value of all domains are also set to 300 K.

The design geometry has undergone custom meshing in order to acquire both good convergence and a reasonable simulation time. The mesh is optimized for Semiconductor module accuracy. Fig. 2 shows the test structure with the derived finite elements.

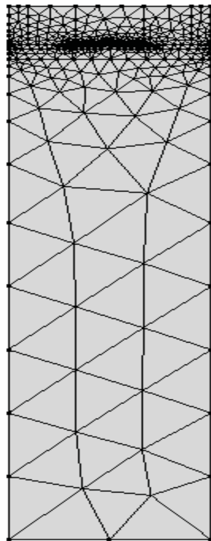


Fig. 2 The meshed 2D design geometry using 725 triangular elements covering 0.333 um^2 of area.

When dealing with transient multiphysics simulations and complex geometries, the solver can be incapable of reaching consistent initial conditions. For this reason, it is advisable to use a two-step approach. This setup uses a stationary study as initialization, results of which are then passed as a stable starting point to the main transient study. At steady state, the model is semi-coupled. It solves for multiple anode voltages (Va) close to 0 V at constant room temperature for all domains. The calculated dependent variables are then used to initiate a fully coupled transient analysis, where Va raises for a time span of 100 ns. Table 1. summarizes all simulation parameters.

Table 1. COMSOL simulation parameters used.

Name	Expression	Value	Description
Tsi	10[nm]	1.0000E-8 m	Active Region Thickness
Tbox	20[nm]	2.0000E-8 m	BOX Thickness
Tsub	1[um]	1.0000E-6 m	Substrate Thickness
Wm	30[nm]	3.0000E-8 m	Contacts Width
Lpl	100[nm]	1.0000E-7 m	Anode Region Width
Lpr	100[nm]	1.0000E-7 m	Intrinsic Region Width
Ln	100[nm]	1.0000E-7 m	Cathode Region Width
Tgox	4[nm]	4.0000E-9 m	Gate Dielectric Thickness
Tg	80[nm]-Tgox	7.6000E-8 m	Gate Stack Thickness
JuncDept	5[nm]	5.0000E-9 m	Junction Depth
P_Doping	1e20[1/cm^3]	1.0000E26 $1/m^3$	Anode Doping
I_Doping	1e16[1/cm^3]	1.0000E22 $1/m^3$	Intrinsic Doping
N_Doping	5e19[1/cm^3]	5.0000E25 $1/m^3$	Cathode Doping
T_0	300[K]	300 K	Starting Temperature
Khfo2	25	25	KfO2 Dielectric Constant
VaMax	3[V]	3 V	Function Max Anode Voltage
Va	2.5[V]	2.5 V	Anode Voltage
Vg	0[V]	0 V	Gate Voltage
Vc	0[V]	0 V	Cathode Voltage
Time	100[ns]	1.0000E-7 s	Max Transient Time

IV. SIMULATION RESULTS

Fig.3 shows the band diagram of the resulted doped structure. Fig.3(a) represents the energy levels without bandgap narrowing effect included. On the following diagram shrinkage of the bandgap occurs when the impurity concentration is particularly high causing shifts at the edges.

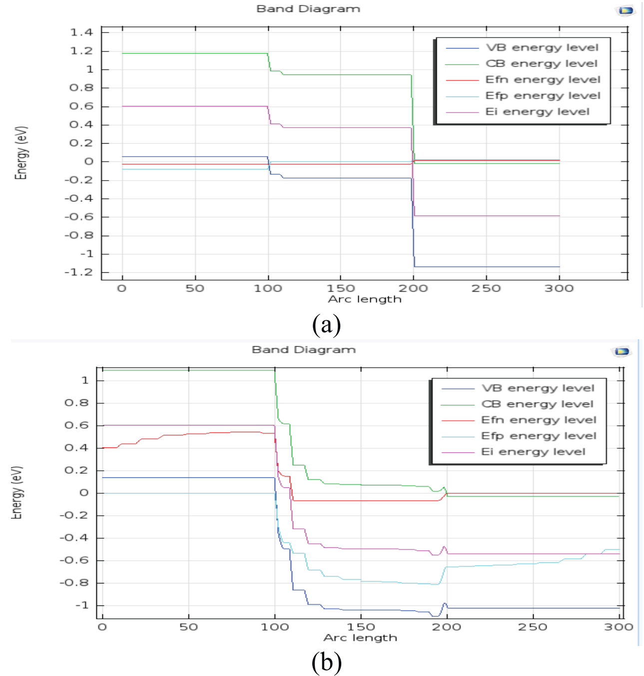


Fig. 3 Band diagrams of the diode: (a) without bandgap narrowing; (b) with bandgap narrowing effect added.

COMSOL tool provides two in-built models for this effect – Slotboom and Jain-Rouston. The latter was selected

due to higher accuracy reported for doping levels over 1×10^{20} cm^{-3} [3].

Fig. 4 represents contour plot of device temperature under transient anode voltage. Time study analysis is using stop condition, which interrupts the simulation if silicon melting point is reached.

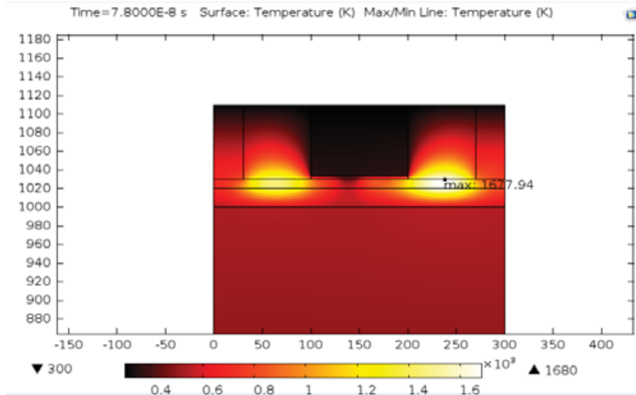
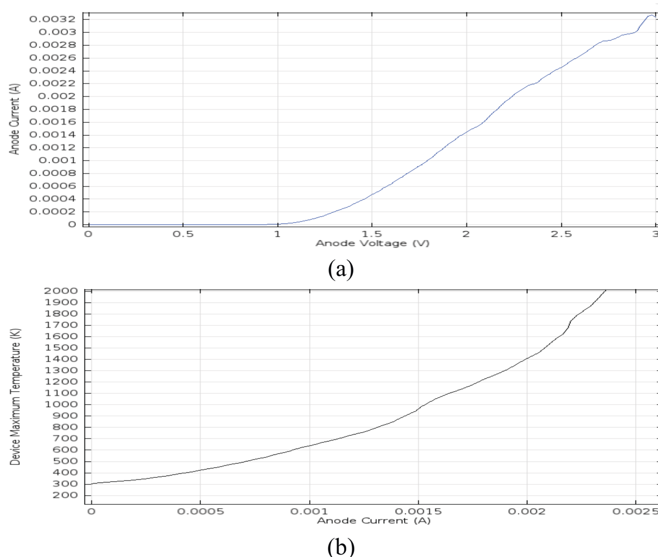


Fig. 4 Surface temperature plot under forward bias.

From Fig 4. can be observed that most of the heat is concentrated under STI regions, even though the current density between the anode and the cathode is pretty much uniform. This can be explained by the low thermal conductivity of the SiO_2 - 1.4 W/mK and the thickness of the isolation. Thus, hot spots are accumulated beneath them. This is also assisted by the fact that the gate dielectric material has thermal conductivity highly dependable on its dimensions [4]. For 4 nm, k is close to 0.5 W/mK. Because of this, the 20 nm thick HfO_2 layer allows a negligible amount of heat to escape through it but that is enough to form temperature gradient at the center. Below the active region, the BOX prevents more heat from reaching the substrate. It has been shown that reduction of BOX thickness and specially selected materials for both buried oxide and substrate can significantly improve the dissipation [2]. In this experimental setup, the majority of heat flux is directed through the anode and cathode copper metals, as they have relevantly high value for k.



(a)

(b)

Fig. 5 (a) Simulated I-V curve of the diode;
(b) simulated diode current in function of temperature.

Using thermal criteria [5], the failure current at 1000 K is 1.6 mA with anode voltage of 2.1 V and at silicon melting point – 2.3 mA and anode voltage of 2.3 V. The maximum current value for same structure simulated with TCAD and reported at paper [2] are 2 mA and 2.2 V at temperature of 1000 K.

COMSOL results yield 4.65% of voltage difference compared to the reference data at stop-temperature. For further calibration relevant tape-out measurements are required.

V. Conclusion

This paper presents a thermal analysis of FDSOI ESD *pin* diode preformed in COMSOL Multiphysics. The software tool provides broad spectrum of modules and in-built models. Mathematical description of all physical effects can be altered and even completely new relations can be added. This provides great flexibility to the user, but can be very time consuming for model optimization. The described here methodology shows applicability of COMSOL as device simulator. Results were obtained and compared with reported TCAD data. The acquired simulation values for the maximum current and voltage for forward biased structure are in decent agreement with the industry established device simulator.

Acknowledgment

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