MODELING NMOS SNAPBACK CHARACTERISTIC USING PSPICE

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***Abstract**: Gate-grounded NMOS is often used as ESD protection for circuit design. The ESD behavior of the NMOS transistor is based on the snapback action of its parasitic, lateral NPN BJT. Modeling this behavior of NMOS devices is very important for design of ICs, because there are no standard models, which can be used for describing high current regions in the NMOS snapback characteristic. In this paper an approach of modeling snapback characteristic of NMOS device, intended for use as ESD clamp in IC I/O cells, is proposed. The modeled snapback characteristic is simulated and evaluated using PSPICE.*

1. Introduction

The most commonly investigated and well-understood phenomenon is the ESD behavior of MOS transistors used as ESD protection devices to discharge the excess power. Depending on how these devices are physically implemented in the layout, the finally produced ESD clamps can be most susceptible to ESD damage, if they have a standard zener characteristic, or actually form robust self-protection devices, when they have a well expressed snapback characteristic. More often ggNMOS (gate-grounded NMOS) clamps are used, instead of ggPMOS (gate-grounded PMOS), because of their more expressed snapback region.

Therefore modeling behavior of ggNMOS devices is very important, especially when design RF ICs. This modeling approach greatly reduces time and effort required for circuit design while making use of ggNMOS as ESD protection, which is widely used for integrated circuits to protect IOs and power rails. The accurate models for these devises, representing properly their characteristic during an ESD event are still not widely available [1].

This paper presents an equivalent circuit for modeling snapback ESD behavior of ggNMOS or ggPMOS devices with or without snapback region. For simulating and evaluating the model, PSPICE program is used.

2. NMOS SNAPBACK

The purpose of this paper is to describe and model the behavior of ggNMOS snapback devices, where they operate as ESD protection structures. There are several different approaches to model snapback characteristic of clamp devices: with controlled voltage and current sources, with BJT, SCR, and etc, or with a combination of them. For example, a parallel combination of NMOS and NPN BJT are used for such modeling in [2], and is shown in Fig.1.

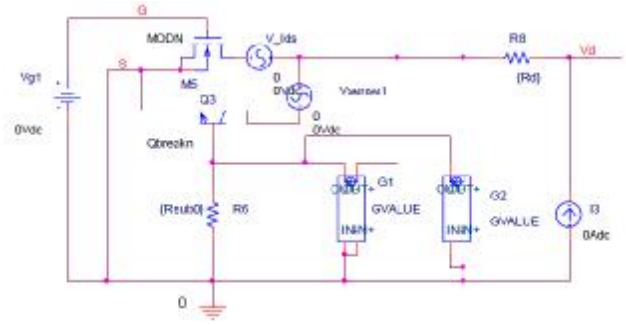

Fig. 1. Spice circuit model of MOSFET

The dimensions of ESD NMOS should be large enough to handle large ESD currents, so multiple fingers structure is used to implement ESD NMOS.

The clamps with ggNMOS devices have snapback behavior in its I-V characteristics. The key snapback element of ggNMOS as ESD protection device is the parasitic NPN bipolar transistor (fig.2).

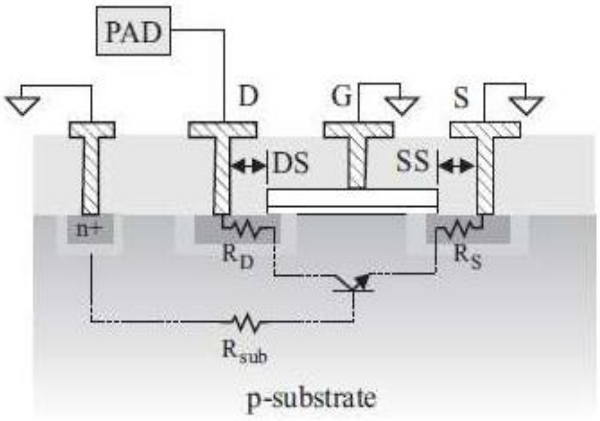

Fig. 2. Grounded gate NMOS transistor

Avalanche breakdown will occur at the drain-substrate junction once exceeds the breakdown voltage [1]. If the drain voltage increases beyond the saturation region, many electron-hole pairs ate generated by the avalanche multiplication. Electrons that occur due to impact ionizations flow to the drain (the collector of the parasitic transistor) and holes flow to the substrate (base) [3]. When ESD stress occurs, sufficiently large number of holes has collected in the substrate; voltage applied to the drain of ggNMOS rises rapidly. The parasitic bipolar transistor switches on and the drain current reaches the snapback region.

In Fig. 3 is presented a snapback characteristic of ESD protection device.

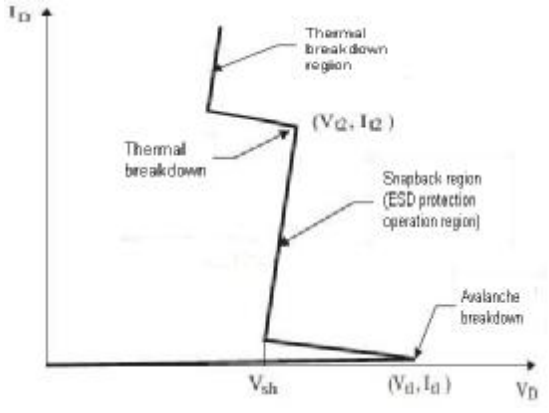

Fig. 3. Snapback clamp I-V characteristic

There are four different regions in snapback characteristic of NMOS. First two linear and saturation regions can be reached by standard MOS equations and modeled in SPICE. Region 3 is avalanche breakdown region, where the standard NMOS equations are no longer valid. Region 4 is the snapback region. [1] If the avalanche breakdown voltage of ESD protection devices is less than their thermal breakdown voltage, then the avalanche breakdown occurs before the thermal breakdown ESD stress will be released by the avalanche breakdown and the devices will not enter the thermal breakdown. If the avalanche breakdown voltage of ESD protection devices is grater than their thermal breakdown voltage, the avalanche breakdown will occur at a voltage higher than the thermal breakdown voltage. The devices will enter thermal breakdown and concentrate currents in a localized area due to negative temperature coefficients device will be destroyed. [4].The goal is to design a SPICE model of NMOS device in high current regions- region 3 and 4.

3. MODELING SNAPBACK CHARACTERISTIC

Clamps are widely used in IOs to protect gates of transistors and one of most known scheme of ESD protection is ggNMOS, which is a two terminal device. One of the approaches to model snapback characteristic of NMOS device is to treat it as a two terminal black box clamp.

To model this characteristic in PSpice a zener diode can be used. The zener diode is modeled as an area dependent ohmic resistance in series with an intrinsic diode and a voltage source. Positive current is the current flowing from the anode through the diode to the cathode. Zener diodes have a higher clamping ratio (the ratio between impulse clamping voltage and dc breakdown voltage). Heat dissipation of ESD at the p-n junction is slower, which increases the clamping voltage level. [5]

The output resistance of the zener diode $r_o=\Delta V/\Delta I$, is the slope of its I-V characteristic. It can be modeled using GTABLE (voltage-controlled current source) and ETABLE (voltage-controlled voltage source) devices (fig.4). GTABLE is a transconductance amplifier, while ETABLE is a voltage amplifier.

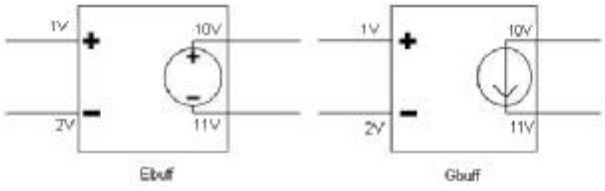

Fig. 4. E and G devices in PSpice

Using GTABLE device the operation of zener diode can be modeled in the firs two regions of I-V characteristic - when the current is 0A until reaching Vz and begin to increase due to certain voltage above Vz, when it is limited in the GTABLE.

To form the next part of the I-V characteristic with negative output resistance an ETABLE or an amplifier with negative gain coefficient (-k) is needed. This amplifier will decrease the amplitude of the zener voltage Vz and will model the curve with negative output resistance, where the voltage decreases with increasing the current. An ETABLE device is more appropriate instead of simple amplifier because it incorporates a limiter. A schematic of G devise controlled by an amplifier with negative gain is shown in Fig. 5.

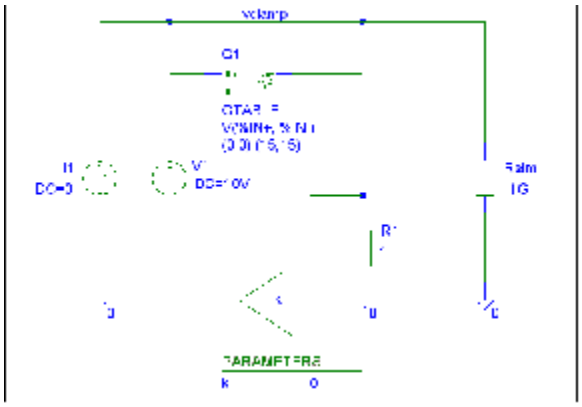

Fig. 5. GTABLE device controlled by amplifier

The circuit operates as follows. When the voltage vclamp is increased above the predefined value, set by the voltage source V1, the output current starts to flow via resistor R1. If the amplifier gain coefficient k is k=0 then the output resistance is inversely proportional to the transconductance G of the GTABLE:

$$r_o = \frac{1}{G} \qquad (1)$$

If k≠0, then we can write the following equations for the output resistance with the feedback r_{FB}:

$$r_{oFB} = \frac{\Delta Vclamp}{\Delta_{I1}} = \frac{\Delta_{I1} r_o + \Delta_{I1} R_1 k}{\Delta_{I1}} \qquad (2)$$

Thus:

$$r_{oFB} = r_o + R_1 k \qquad (3)$$

If the amplifier gain coefficient k is positive the output resistance is increased or:

$k>0, \quad r_{oFB} > r_o$ (4)

If the amplifier gain coefficient k is zero the output resistance is unchanged:

$k=0, \quad r_{oFB} = r_o$ (5)

If the amplifier gain coefficient k is negative the output resistance is reduced.

$k<0, \quad r_{oFB} < r_o$ (6)

When:

$$k = -\frac{r_0}{R_1}, \quad r_{oFB}=0 \qquad (7)$$

And when:|

$$k < -\frac{r_0}{R_1}, \quad r_{oFB}<0 \qquad (8)$$

When Eq. (8) is fulfilled, the output resistance is negative. A simulation of the output resistance r_{oFB} is shown in Fig.6.

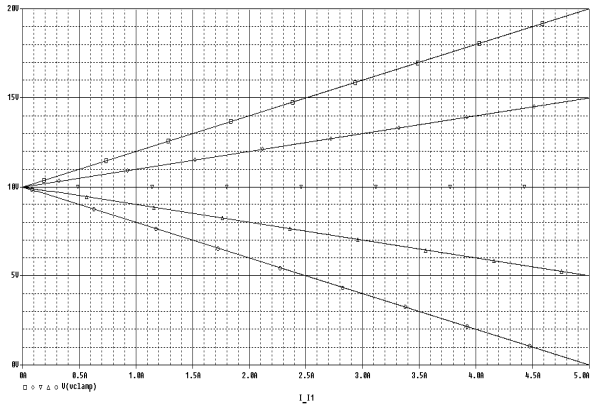

Fig. 6. Simulation of clamp I-V characteristic with controlled output resistance, k=1, 0, -1, -2, -3.

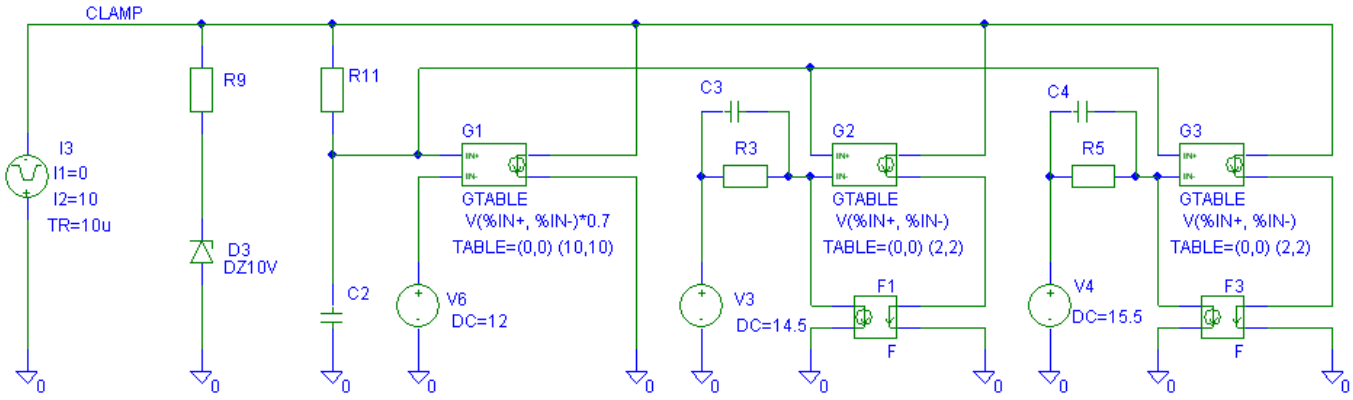

Fig. 7. Model circuit of NMOS snapback characteristic

Using described devices a snapback characteristic of NMOS device can be modeled as shown in Fig.7. Simulation result is shown in Fig.8

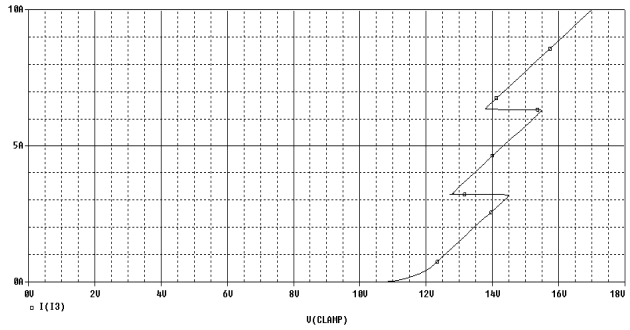

Fig. 8. Simulated snapback characteristic

For needs of this research the triggering voltage is 10V and is defined by the breakdown voltage of the zener diode D3. The snapback regions are limited by the voltage sources V6, V4, V3 and by the G and F device parameters, so the values of current and voltage can be modeled depending of different requirements.

4. Conclusion

NMOS and PMOS devices, which are used as ESD protection devices in RF IC design, have strong snapback characteristic. It is very hard to provide the behavior of those elements under ESD stress, because there are no standard models, which can be used for simulation during the design. The example given in this paper is model ggNMOS snapback characteristic, because this is widely used protection mechanism in IOs and power rails.

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