Simulation of LNA in 0.18µm CMOS Technology

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***Abstract* – In the paper an approach for redesign and simulation of narrow band LNA for UHF application is discussed. Several parameters, which are very important in design and verification of low noise amplifiers, are presented. These parameters can show how the amplifier is going to work after ESD structures being incorporated in the design. A low noise amplifier for future studying ESD protection structures are simulated in 0.35µm and 0.18 µm CMOS technologies.**

***Keywords* – LNA design, RF CMOS, simulation**

I. Introduction

CMOS technology is becoming a commercially viable manufacturing option. With the decrease of gate oxide thickness, CMOS circuits become more sensitive to stress from electrostatic discharge. The Low Noise Amplifier (LNA) is arguably the most critical building block in the receiver path of a transceiver system. The LNAs are very sensitive to ESD stress. The LNA should have a high sensitivity and be able to amplify the received signals with a very low level of amplitude without increasing the noise level. The ESD structures degrade LNA performance particularly for higher frequency applications.

The LNA is the first block in most receiver front-ends [1]. The LNA determines the signal to noise ratio of the whole receiver band [2]. A simplified block diagram of a basic architecture used in many RF receivers is shown in fig.1.

The simulated LNA in 0.18µm CMOS technology have gain over 20dB in the frequency range 2.2 to 2.7GHz. This is frequency range called UHF – ultra high frequency. UHF is widely used in two-way radio systems, telephones. Several public-safety and business communications are handled on UHF. UHF frequency is also used in GSM and UMTS cellular networks, GPS.

In smaller technologies (compared to the 0.6µm CMOS technologies and other) the main advantage is that the components occupy a smaller area. Accordingly gates capacity is less. Another advantage of these technologies is that the elements have lower threshold voltage, which in turn leads to the opportunity of working with lower voltages. This comes from fact, that in 0.35µm and 0.18µm the length channel is smaller than other CMOS technologies. This requires less voltage to form the channel.

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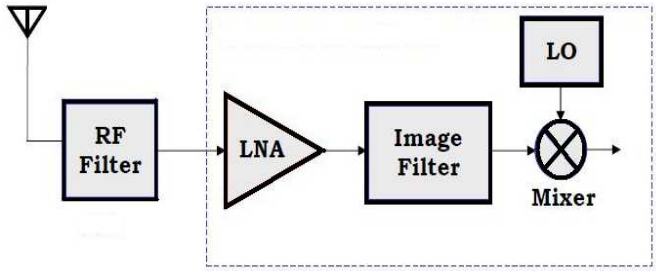


Fig.1. A typical RF receiver architecture

LNAs with gate length of 0.18µm or below open up the possibility of low power consumption compared to bipolar and BiCMOS technologies. CMOS LNAs must also equal and surpass the low noise figure of these technologies [3].

The designed LNA has been simulated using SpectreRF Simulator from Cadence Design System in standard 0.18µm CMOS technology. The goal was to redesign and simulate the LNA realized on 0.35µm CMOS technology [4], for further studying the influence of on-chip ESD protection structure over some typical LNA characteristics.

In the paper are analyzed the results of CMOS RF low noise amplifier designs typically do not take the on chip ESD structures into consideration during the design process. The goal of this research is to be compared results after ESD structures being incorporated in the LNA design for the both technologies.

II. LNA Simulation

In LNA design presents a considerable challenge because of its simulations requirement for high gain, low noise figure, good input and output matching and unconditional stability at the lowest possible current draw from the amplifier. The LNA is required to amplify incoming signals and extract them from the noisy environment, thus enabling signal processing by blocks further down the receiver chain. The gain provided by the LNA is generally defined in terms of the voltage gain (Av=Vout/Vin) or power gain (S21 = Pout/Pin) [5].

There are several parameters, which are very important in design and verification of low noise amplifiers and these parameters are simulated and presented below. These parameters can show how the amplifier is going to work after ESD structures being incorporated in the design. The chosen scheme of the LNA was simulated using Cadence. This scheme is shown on fig.2. Capacitor can be added in parallel with the Ld to make the gain and NF response more selective and narrow. Rd models the series resistance of ideal inductor.

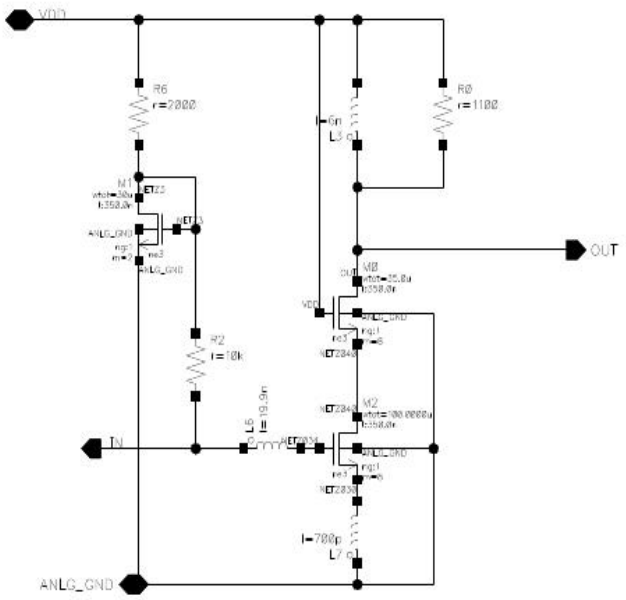


Fig.2. Schematic of LNA used for simulations

Fig. 3 shows the test bench for a single ended LNA structure used for simulations. The used values are Vdd = 3.3V, C1= 10nF, C2 = 10nF, CL = 500fF, respectively. The baluns used in the test bench are too-port devices.

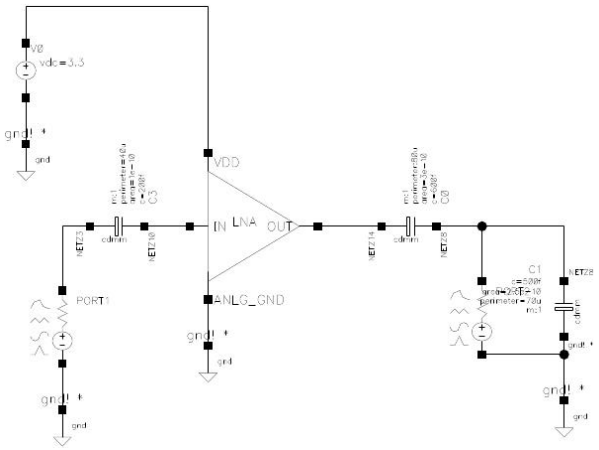


Fig.3. Test bench of LNA

The used approach in the redesign and simulation includes next steps:

- S-parameters simulation of the LNA scheme realized on 0.35µm CMOS technology;
- Drawing the same LNA scheme on 0.18µm CMOS technology
- S-parameters simulation of the LNA scheme realized on 0.18µm CMOS technology;
- Comparison the simulation results for the both technologies and analyzing influence of the LNA scheme elements on the received results
- Next change the element's values of the LNA scheme on 0.18µm CMOS technology for better matching the simulation results for the both technologies

Follow the indicated approach the simulated scheme structure in 0.18µm technology, initially was the same as chosen scheme [4], realized in 0.35µm CMOS technology. The same scheme, realized in 0.18µm CMOS technology, has to be redesigned (for better matching results from the carried out simulation of the both technologies). To achieve equal simulation results some models of transistors and components are selected. Simulations were made to examine the influence of components over the important parameters. For instance, the change of the transistor M2 width affects the S11 and S22 parameters. The numbers of the transistors M0 and M2 are made to be even, not odd. This applies for getting better matching topological parameters in the deployment of elements. Generally increasing the length of the transistor M0 leads to bed results of the studied parameters. But its width is made to be slightly greater than that of the scheme in 0.35µm technology due to its strong influence on S22 parameter. Changing the values of M1 shows their impact on S12 and S21 parameters. L6 inductance is 12nH in the scheme, realized in 0.35µm CMOS technology. In these, realized in 0.18µm with increasing (19.9nH, but not more than 20nH) the value of L6 results for S-parameters are getting better. To reach the values of S12 and S21 parameters as these in 0.35µm, it has to be changed the value of R0. This resistance has to be bigger (R0=1100Ω). The smaller value of R6 resistance worsens the simulated parameters, and for more than a given observed very slight change. For this reason remains the same.

After this redesign, the final simulations results of the LNA, realized in 0.18 CMOS technology, which are equal as these in 0.35 technologies, are as follows:

A. Matching parameters

The matching parameters of chosen LNA are S-parameters – S11, S12, S21, and S22. S11 and S22 have the meaning of reflection coefficients, and S12, S21, the meaning of transmission coefficients. The scattering parameter matrix of the single-ended LNA is given by matrix:

$$\begin{bmatrix} S_{11} S_{12} \\ S_{21} S_{22} \end{bmatrix}$$

Here S21 is the gain of LNA and the other reflection coefficients are indications of the quality of impedance matching at each port. S12 is the strength of the reverse signal.

The input impedance is excellently matched over a multi-GHz band: S11 lower than – 10dBm for all frequencies up to 4GHz [6]. For the simulated schematic S11 ≤ -22dBm. The impedance matching at the output up to 2.67GHZ is S22> -9dBm. The value of S12 must less then -20dB to have good isolation between output and input [7, 8]. In this paper is achieved less then -40dB.

Results for S-parameters are shown in fig.4a and 4b.

B. Gain

Three power gain definitions appear in the literature and are commonly used in LNA design:

- GT - transducer power gain

- GP - operating power gain
- GA – available power gain

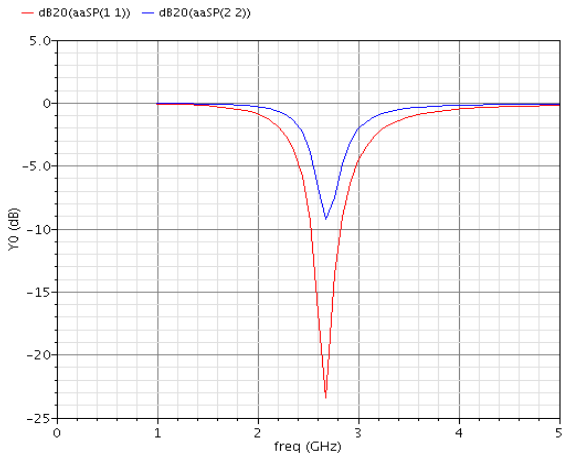


Fig.4a. Parameters S11 and S22

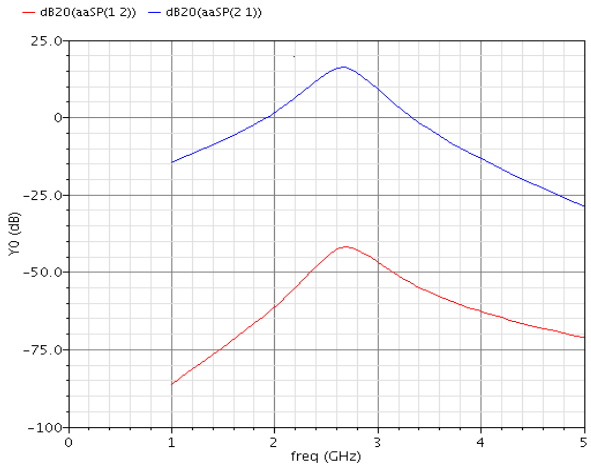


Fig.4b. Parameters S12 and S21

Transducer power gain is defined as the ratio between the power delivered to the load and the power available from the source.

$$G_T = \frac{1-|r_s|^2}{|1-s_{11}r_s|^2}|s_{21}|^2\frac{1-|r_L|^2}{|1-r_{out}r_L|^2} \qquad (1)$$

Operating power gain is defined as the ratio between the power delivered to the load and the power input to the network.

$$G_p = \frac{1}{1-|r_{in}|^2}|s_{21}|^2\frac{1-|r_L|^2}{|1-r_{22}r_L|^2} \qquad (2)$$

Available power gain is defined as the ratio between the power available from the network and the power available from the source.

$$G_A = \frac{1-|r_s|^2}{|1-s_{11}r_s|^2}|s_{21}|^2\frac{1}{1-|r_{out}|^2} \qquad (3)$$

The tree gain definitions of simulated LNA are shown in fig.5.

Because the power available from the source is grater than the power input to the LNA network, GP>GT. Similarly, because the power available from the LNA network is greater than the power delivered to the load, GA>GT [7].

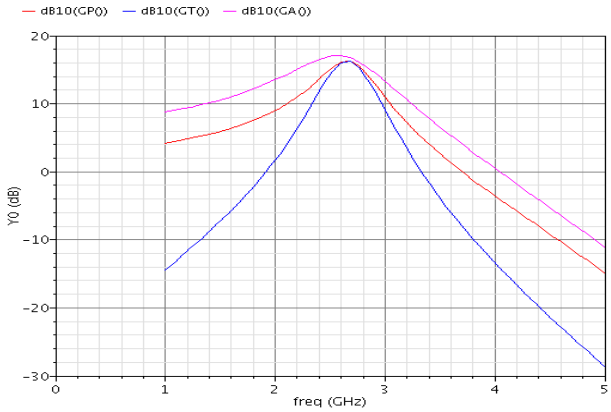


Fig.5. Power gain

C. Stability

In the presence of feedback paths from the output to the input, the circuit might become unstable for certain combinations of source and load impedances. A LNA design that is normally stable might oscillate at the extremes of the manufacturing or voltage variations, and perhaps at unexpectedly high or low frequencies.

Alternative stability factors are Kf and B1f.

$$Kf = \frac{1+|\Delta|^2-|s_{11}|^2-|s_{22}|^2}{2|s_{21}|\,|s_{12}|} \qquad (4)$$

where

$$\Delta = s_{11}s_{22}-s_{12}s_{21} \qquad (5)$$

When K>1 and B1f(Δ)<1, the circuit is unconditionally stable. That is, the circle does not oscillate with any combination of source and load impedances.

The unconditional stability requirements of a circuit are Kf>1 and B1f>0[8]. In this work, Kf is higher than 4 and B1f is higher than 0.6 over the frequency range of interest.

These stability parameters are shown in fig.6.

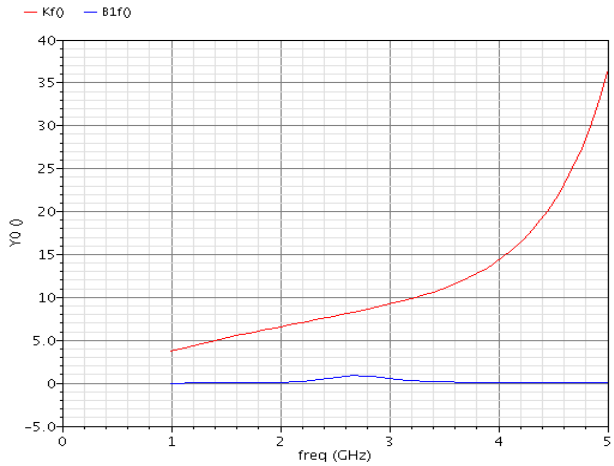


Fig.6. Stability factors Kf and B1f.

D. Noise figure

The overall noise figure is mainly determined by the first amplification stage, provided that it has sufficient gain (fig 7). NF is the practical noise figure of a practical RF network and NFmin is the ideal or a theoretical noise figure of a circuit, NF = NFmin+matched network factor.

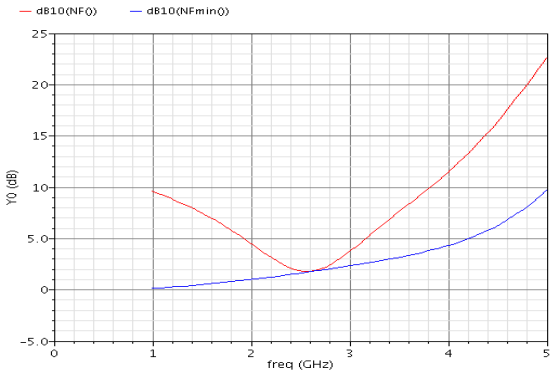


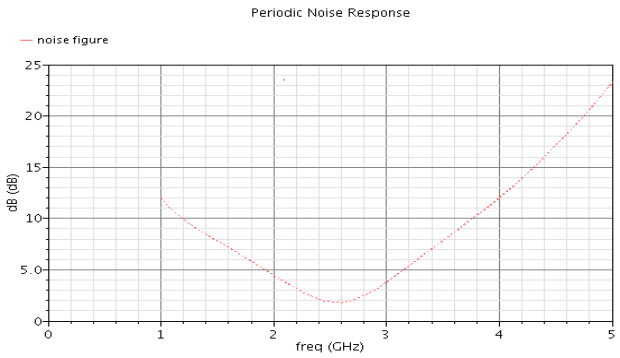
Fig.7. NF and NFmin parameters

H. Nf by Large signal Noise simulation (PSS and Pnoise Analysis)

The PSS and Pnoise analyses for large-signal and nonlinear noise analyses are used, where the circuits are linearized around the periodic steady-state operating point. As the input power level increases, the circuit becomes nonlinear, the harmonics are generated and the noise spectrum is folded. Therefore, we should use the PSS and Pnoise analyses. When the input power level remains low, the NF calculated from the Pnoise, PSP, Noise, and SP analyses should all match.

The Pnoise analysis summary shows the contributions of different noise sources in the total noise. This is very powerful to focus the effort to improve the noise performance of the device which contributes the maximum noise.

The results, using Pnoise analysis are shown in fig.8a, b.



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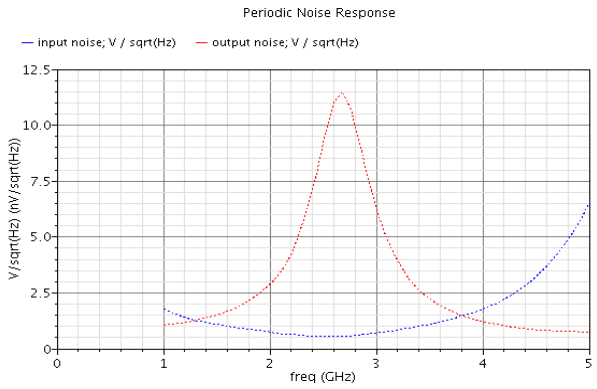

b

Fig.8. NF, Input and Output noise using Pnoise Analysis

III. Conclusion

An approach is presented for redesign in case of matching simulation results for the same narrow band LNA realized on two technologies 0.35µm and 0.18µm, respectively.

This work discusses LNA test bench setup, LNA design parameters, and how to simulate an LNA and extract design parameters. Some useful analysis tools for LNA design, such as SP, PSS, Pnoise, analyses are addressed. The results from the analyses are interpreted.

The LNAs, which are demonstrated in this paper, will be used for further simulations and studying ESD protection in RF CMOS.

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