A methodology for phase-frequency detectors testing based on Xilinx FPGA

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Abstract – **A methodology for phase and phase-frequency detector testing is developed and implemented on Xilinx FPGA programmable logic device. Several test setups and circuits for phase-to-amplitude response testing are proposed in this article. The circuits for test signals generation are discussed. The output pulses of the tested phase detectors are converted to a digital value in order to obtain the phase-to-amplitude response of the examined detectors. The variations of the circuits for the different phase detectors testing is discussed.**

Keywords – **digital phase synchronizers; FPGA; phase detectors; phase-to-amplitude; time-to-code.**

I. INTRODUCTION

Phase detectors are one of the main parts of phase locked loop (PLL) circuits. With the advancement of digital electronics, more and more entirely digital PLL circuits are designed [1]. For the purpose of circuit optimization, the parameters of the phase detectors must be measured. Most of the developed test setups for phase detectors to this moment are based on an analog integrator after the detector circuit. When designing an entirely digital PLL the use of analog stages in the test procedure is not optimal [2]. A testing procedure for digital phase detector circuits is developed and tested in this paper. The test setup is completely digital and is implemented entirely on a Field Programmable Gate Array (FPGA) logic device [3]. This gives flexibility for fast reconfiguration of the different examined phase detectors. A functional equivalent is developed and tested for the analog integrator used in the standard PLL circuits [4]. A circuit for generating test signals with adjustable duty cycle and phase shift is proposed and tested. A digital module called time-to-code converter is proposed for digital code formation based on the duty cycle of the pulses at the output of the tested phase detectors [5]. On the basis of this code the phase-to-amplitude response of the detectors is built. Using the results from the testing we can choose the proper phase detector for the developed digital phase synchronizer [6].

II. STRUCTURE OF THE TEST SETUP

In order to choose the optimal phase detector for the digital PLL system, the different available phase detectors should be tested. For the test setup we need a test signal generator and a time-to-code converter [7]. As the phase detectors have two inputs for the two signals which are being compared, we need a generator which can generate two pulse trains with adjustable phase difference and duty cycle. At the output of the phase detector the signal is in the form of pulses with variable duty cycle depending on the phase difference between the compared signals [8]. In order to quantify the output pulses, they need to be converted to digital code. For this purpose, the time-to-code converter is proposed. It converts the width of the input pulses to binary code [9]. The block diagram of the test setup is presented in Fig.1.

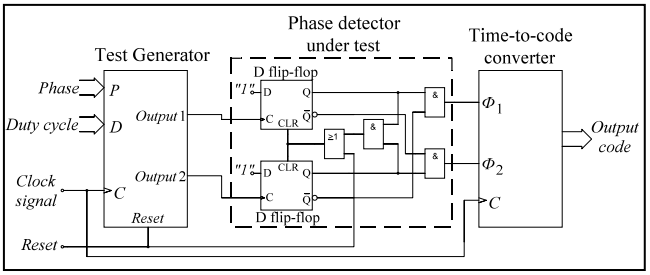

Fig. 1. Phase detector test setup – block diagram

The displayed phase-frequency detector has two outputs Φ_1 for positive and Φ_2 for negative phase difference. For this reason, the time-to-code converter has two inputs. When a pulse is applied at the Φ_1 input, the output value is increased and if a pulse is applied at the Φ_2 input – the output value is decreased. In order to have a dynamic range in the positive and negative direction, the initial value of the converter equals the half of its range. The test generator and the time-to-code converter need a clock signal. In this case we use one clock signal for both modules in order to eliminate the potential error from clock signal frequency variations. The generated test signals frequencies depend on the clock frequency.

III. STRUCTURE OF THE TEST GENERATOR

One of the most important parts of the phase detectors test setup is the test signal generator. It generates two square wave signals with a controllable phase difference and duty cycle. The generator consists of a square wave pulse generator and a shift register. The pulse generator synthesizes square wave pulses with controllable duty cycle and an output frequency of 1/8 of the input clock. It consists of a 4-*bit* presettable binary counter, binary adder and a binary comparator. The duty cycle is controlled by a 3-*bit* binary number *D* applied to the data input of the counter and one of the inputs of the binary adder. The applied number is summed with constant “7” Fig. 2.

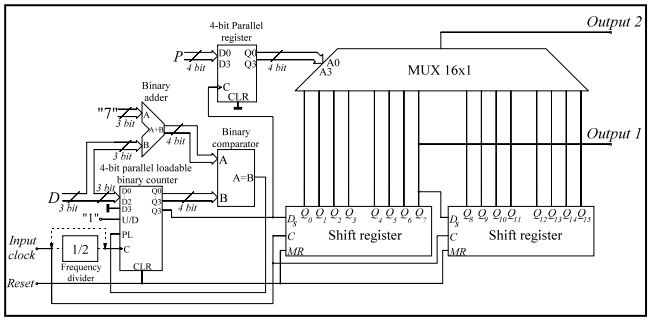

Fig. 2. Test generator – logical diagram

The 4-*bit* result of the addition is compared with the state of the counter by the binary comparator. When the state of the counter becomes equal to the sum, the output of the comparator activates the parallel load enable input of the counter. The next clock cycle loads number *D* in the counter. In this way one cycle of the process is always 8 clock cycles long. Number *D* defines the range of numbers in which the cycle will develop. Depending on number *D* the counter will count from 0 to 7 or from 1 to 8 up to 7 to 14. As the output is taken from Q_3 of the counter, the duty cycle of the output pulses will depend on the number *D* and will have one of the following values: 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75% and 87.5%. As the 0% duty cycle is unusable, the number *D* is limited from 1 to 7.

The generated square wave signal is applied to the series input D_S of the 16-*bit* shift register. The phase difference range and the phase step depend on the relation of the clock frequencies to the pulse generator and the shift register. The clock signal to the shift register can be either the same as the clock signal to the pulse generator, or with twice the frequency. This configuration is achieved by adding a frequency divider at the clock input of the pulse generator. With a frequency ratio of 2:1 between the shift register and the pulse generator, the phase difference range is ±180° and the frequency step is 22.5° between two adjacent outputs of the shift register. The frequency of the output pulses is $1/16^{th}$ of the input clock frequency. In the case of frequency relation 1:1 between the shift register and the pulse generator, the phase difference ratio becomes ±360° and the phase step is 45°. The output pulses frequency is $1/8^{th}$ of the input clock frequency. The timing diagrams of the test generator are presented in Fig. 3.

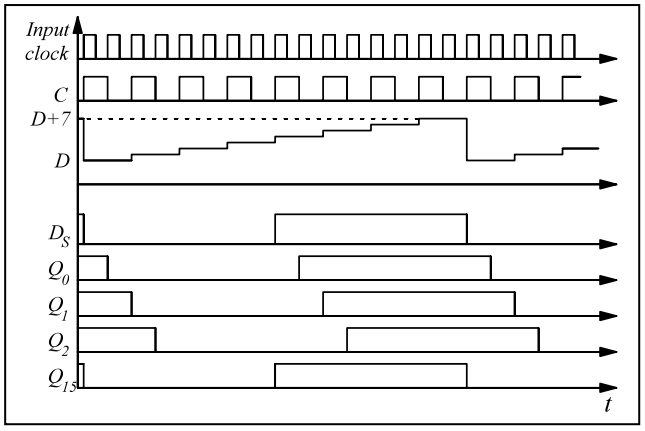

Fig. 3. Test generator – timing diagrams

The square wave generator and the shift register generate 16 signals with standard phase differences. The 16 to 1 multiplexer (MUX) chooses one of the available signals. The other signal is permanently connected to the middle of the shift register. In this way the phase difference between the two signals can be adjusted on the basis of number *P*. Some phase detectors are sensitive to a phase jump of the signals at a certain moment of the period. To solve this problem number *P* is fed to a parallel register, which receives a clock signal from the output of the square wave generator. In this way the address to the multiplexer is changed synchronously at the beginning of every period. Some phase detectors need to be tested with two different duty cycles of the compared signals. The proposed circuit cannot generate two signals with different duty cycles. In these cases, the proposed solution is to use two identical circuits with common clock signal. The fixed outputs from the middle of the shift registers are not used, and the two test signals are connected to the outputs of the multiplexers. In this configuration we can adjust the duty cycle independently for the two signals. Also, we have a larger phase difference interval for the same phase step. The test setup with two test generators is presented in Fig. 4.

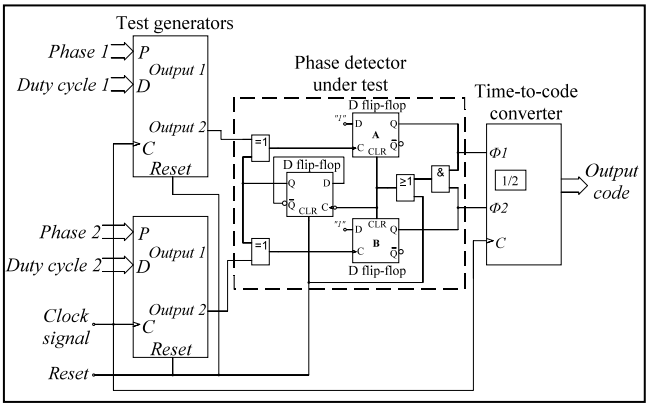

Fig. 4. Test setup with two generators – block diagram

The duty cycles of the two signals are controlled from the *D* inputs of the two generators. The phase difference is controlled by the *P* inputs of the two generators. In this case the phase ranges of the two generators are summed.

IV. Structure of the Time-to-Code Converter

The digital phase-frequency detectors have output pulses whose width depends on the phase difference of the input signals. In order to test the phase-frequency detectors the width of the output pulses should be converted to a digital code [10]. On the basis of that code the phase-to-amplitude response of the detector can be built. The output pulses of the detectors can be converted to digital code by an ideal digital integrator. This method is not useful in this case because it will give a code that increments continuously on every period of the input signals. A time-to-code converter is designed to generate digital code proportional to the pulse width [10, 11]. It integrates the pulse width of the signals for one period and stores the result in a parallel register. Then the reversible counter is loaded with the initial value. As the tested phase differences can be positive and negative for some of the detectors, the time-to-code

converter should have the ability to register positive and negative values. This task is achieved by loading the counter with initial value equivalent to the middle of its range. The logical diagram of the time-to-code converter is presented in Fig. 5.

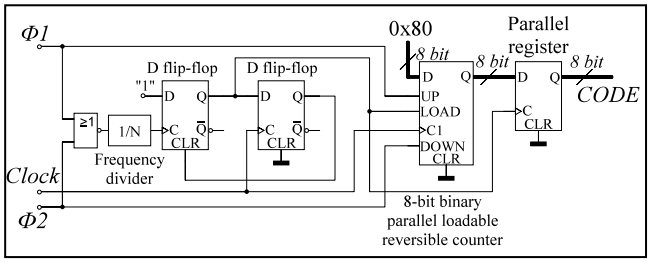

Fig. 5. Time-to-code converter – logical diagram.

The circuit consists of three parts:
- triggering circuit;
- integrating circuit;
- storage circuit.

The triggering circuit detects the periods of the input signals and generates the signals needed for loading the counter and storing the value into the parallel register. The circuit is built with two *D* type flip-flops. The falling edge of the tested signal loads the first flip-flop with logical "1". Its output is connected to the parallel load enable input of the counter-integrator and to the clock input of the parallel register. The next clock pulse of the *Clock* signal loads the value from the counter into the parallel register and loads the counter with its initial value. It also loads the second *D* flip-flop with logical "1" which clears the first flip-flop asynchronously. At this moment the circuit is in its initial condition ready for measurement of the next pulse. The pulses of the *Clock* signal are integrated into the reversible counter depending on the input to which the pulse from the tested detector has arrived. If the pulse has arrived at the Φ_1 input, the *UP* enable of the counter is activated, and the *clock* pulses are added to the current value. If the pulse has arrived to the Φ_2 input, the *DOWN* enable of the counter is activated and the *clock* pulses are subtracted from the value. In some cases, the integration time should be longer than one period of the output signals. For these situations a frequency divider is connected before the clock input of the triggering circuit. Depending on the division coefficient *N* periods can be integrated. The timing diagrams of the time-to-code converter are presented in Fig. 6.

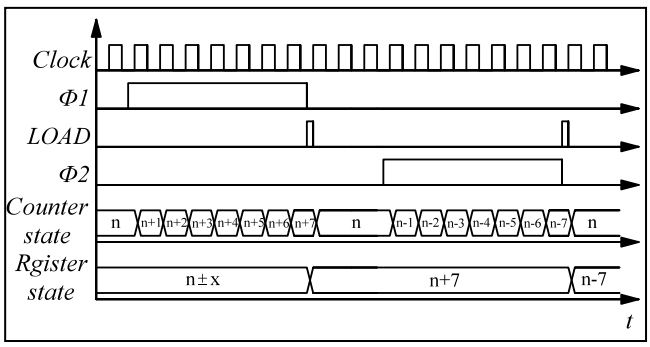

Fig. 6. Time-to-code converter – timing diagrams.

The circuit can be modified easily for testing phase detectors with only one output. The clock input of the triggering circuit is connected to either one of the input signals, or to the output signal of the detector. The *UP* enable input of the counter is connected directly to the phase detector output, and the *DOWN* enable input is connected to the same signal but in inversed form.

V. Experimental results

A phase-frequency detector with three D type flip-flops working on the two edges of the compared signals is tested using the developed testing methodology. The used test setup is presented in Fig. 4. The value of the clock frequency is 1 *kHz*. The test generators have 2:1 frequency ratio between the shift register and the pulse generator clock signals. The test pulses to the phase-frequency detector are with 1/16th of the input frequency. The time-to-code converter is configured to integrate the value for two cycles of the phase-frequency detector signals. Its output code is then divided by two in order to find the mean value of the two integrations. The division by two is implemented as 1-*bit* shift to the right of the output value. The results from the test with two signals with 50% duty cycle are presented in a tabulated form in Table 1.

Table 1. Results from the phase-frequency detector test

Phase °	-315°	-270°	-225°	-157.5°	-135°
CODE	0x79	0x79	0x79	0x79	0x7A
Phase °	-90°	-45°	0°	45°	90°
CODE	0x7C	0x7E	0x80	0x82	0x84
Phase °	135°	157.5°	225°	270°	315°
CODE	0x86	0x87	0x87	0x87	0x87

The phase in degrees is represented along with the output code of the time-to-code converter in hexadecimal value. The phase-to-amplitude response of the examined phase-frequency detector is presented in Fig. 7.

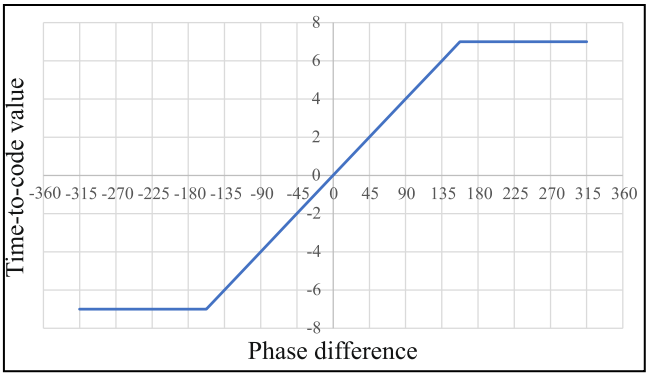

Fig. 7. Phase-to-amplitude response of phase-frequency detector.

The output code from the time-to-code converter is depicted on the vertical axis in decimal format. The code is shifted in a such way that the middle of the range is represented as zero. The linear phase range of the converter is clearly seen along with its two dead zones. The results from the testing of the same phase-frequency detector with signals with 25% duty cycle of the first signal and 50% of the second are presented in tabulated and graphic form in Table 2 and Fig. 8.

TABLE 2. RESULTS FROM THE PHASE-FREQUENCY DETECTOR TEST

Phase °	-225°	-180°	-135°	-90°	-45°
CODE	0x79	0x79	0x7A	0x7B	0x7C
Phase °	0°		45°	90°	135°
CODE	0x7E		0x80	0x82	0x84
Phase °	180°		225°	270°	315°
CODE	0x85		0x86	0x87	0x87

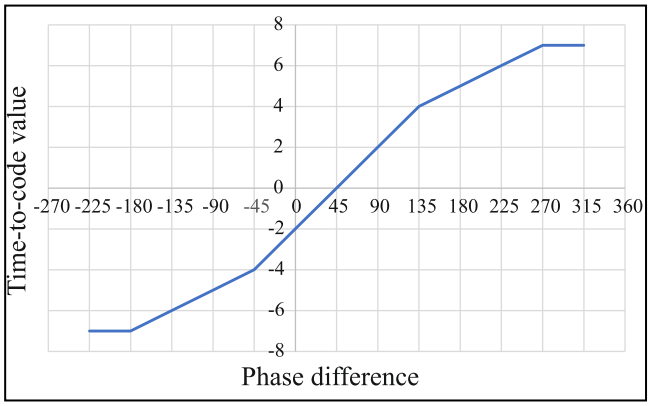

Fig. 8. Phase-to-amplitude response of phase-frequency detector.

With two different duty cycles of the test signals we can clearly observe the formation of two linear phase regions with different steepness and a shift of the middle of the linear phase range to the positive output codes.

VI. CONCLUSION

A methodology for measurement of digital phase and phase-frequency detectors has been developed and tested. A module for generating test signals with adjustable duty cycle and phase difference is proposed. A module for converting the output signals of the detectors to a digital code is developed. Different modifications of the proposed circuits are discussed in order to achieve the most accurate testing for the different types of digital phase detectors. Using the developed methodology, the different phase and phase frequency detectors can be tested with signals with different duty cycles and frequencies. Using the proposed methodology, the phase-to-amplitude responses of the detectors can be measured and analyzed. In this way a phase detector for a digital phase synchronizer can be tested conveniently in its natural environment - the digital logic chip. On the basis of the results the different phase and phase-frequency detectors can be compared. The most suitable detector for the application can be chosen on the basis of its linear range or frequency sensitivity. New types of detectors can be designed more easily using the developed methodology. For more precise examination of the phase-to-amplitude responses of some phase detectors it is better to have a smaller phase step. This can be achieved with a longer chain of shift registers and a higher clock frequency relation between the shift register and the pulse generator. The use of a FPGA programmable logic device has the advantages of fast reconfiguration for examining different detectors. It also offers fast and easy scalability of the design for different working frequencies and phase ranges for the different phase detectors. All the developed circuits are tested, and their advantages and limitations are discussed. A solution to the limitations is proposed through modifications of the designed circuits. A phase-frequency detector working on the rising and the falling edges of the input signals is tested using the methodology developed herein. The results from the testing prove the effectiveness of the proposed methodology and show good accuracy as they coincide with the results from the software simulation.

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