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Simulation Investigation of a Power Amplifier Circuit for Measurements of Power Losses in Soft Magnetic Materials

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Abstract – **This paper presents an investigation of a high frequency power amplifier circuit intended to be used for measurements of power loss in soft magnetic materials. It is given a description of the envisaged measurement system. Afterwards, simulation investigation of two variants of the amplifier circuit realization is presented where the frequency response of the two circuits is within the focus of interest. The results obtained will serve a reference point in the progress of the dedicated measurement system development.**

Keywords – **core losses, measurement set up, operational power amplifier, simulations**

I. INTRODUCTION

One of the most spread approaches for measurements of power losses in soft-magnetic materials is the no-load transformer measurement method [1-3]. A principal schematic of the circuit for applying this method is depicted in Fig. 1. The method consists of the following: around a magnetic core made of the soft-magnetic material under interest (CUT) there are wound two windings – primary one and secondary one. For sinusoidal excitation conditions, across the primary winding sinusoidal test voltage is applied and the secondary winding is left open. The power losses in the core are obtained through calculating the integral of the product of the time-varying secondary voltage measured within one period of the waveform and the current through the primary winding measured within that same time interval.

In order to obtain the power losses in the core at different frequencies and magnetic flux density levels, the voltage waveform applied across the primary winding has to be set accordingly. For example, for one and same given flux density level B_{peak} to present in the magnetic core at different frequencies f_{op}, at each frequency one and same magnetic field intensity has to be maintained, that is current of one and same magnitude $I_{\text{p,peak}}$ must flow through the primary winding of the test transformer. Therefore, for measurements at constant B_{peak} and increasing frequencies, the amplitude of the test primary voltage $U_{\text{p,peak}}$ has to be increased in order to compensate the increasing impedance of the primary winding's inductance L_{p}. Alternatively, for increasing B_{peak} at a single f_{op}, that is increasing amplitudes of the current through the primary winding at this same frequency, the primary voltage's amplitude has to be again accordingly increased in order to cause increased currents to flow through the one and same impedance of L_{p} at that given frequency. In summary, the primary winding of the test transformer has to be powered by a source that is capable of delivering from low to high current and voltage amplitudes. At certain measurement conditions, these amplitudes could need to be quite large – in the order of units of amperes and tens to hundreds and thousands of volts, which depend upon the magnetic core cross section and the number of turns of the primary winding N_{p}. An example of the $U_{\text{p,peak}}$ and $I_{\text{p,peak}}$ values needed to measure core loss at different f_{op} and B_{peak} conditions of ferrite N87 using ring core R 36.0×23.0×15.0 with N_{p}=4, is shown in Table 1.

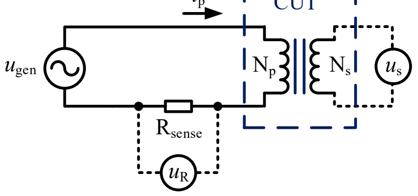

Fig. 1. Schematic of the measurement method under consideration

TABLE 1. VOLTAGE AND CURRENT NEEDED TO MEASURE POWER LOSS OF N87 FERRITE WITH A RING CORE R36, N_{P}=4 AND THE METHOD DEPICTED IN FIG. 1

$U_{\text{p,peak}}$, [V]		at f_{op}, [kHz]						
		10	20	50	100	200	500	1000
to get B_{peak}	25 mT	0.6	1.2	3.0	6.0	12.0	30.1	60.2
	50 mT	1.2	2.4	6.0	12.0	24.1	60.2	120.4
	100 mT	2.4	4.8	12.0	24.1	48.2	120.4	240.8
	200 mT	4.8	9.6	24.1	48.2	96.3	240.8	481.7
	300 mT	7.2	14.5	36.1	72.3	144.5	361.3	722.5

$I_{\text{p,peak}}$, [A]		at f_{op}, [kHz]						
		10	20	50	100	200	500	1000
to get B_{peak}	25 mT	0.2	0.2	0.2	0.2	0.2	0.2	0.2
	50 mT	0.4	0.4	0.4	0.4	0.4	0.4	0.4
	100 mT	0.8	0.8	0.8	0.8	0.8	0.8	0.8
	200 mT	1.6	1.6	1.6	1.6	1.6	1.6	1.6
	300 mT	2.4	2.4	2.4	2.4	2.4	2.4	2.4

In applying the measurement method discussed, the common practice for fulfilling the power requirements to the sinusoidal source, as listed above, is the use of two separate devices – a function generator for providing the test voltage

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waveform and a power amplifier to provide the needed voltage and current levels [4, 5]. The research being carried out is focused on the development (design and physical realization) of a dedicated power amplifier circuit for setting up a core loss measurement system. Results of the research are reported in this paper.

The paper is organized as follows: Section II describes the envisaged measurement system; there are regarded requirements to the power amplifier circuit, decisions made so far about the concrete realization of the amplification and respective power supplies as well as the nature of the load as seen by the amplifier's output. Section III is devoted to presenting simulation investigation of the amplifier realizations that are taken into account. The end section concludes the work presented and outlines future directions of the research being carried out.

II. DESCRIPTION OF THE MEASUREMENT SYSTEM

The basic electrical connections of the measurement system envisaged to be utilized is shown in Fig. 2. In the figure, V_{in} represents a function generator, V_{CC} and V_{EE} are dc supplies, POA stands for the power amplifier circuit to be developed, and the C_{coup}-L_{CUT}-R_{sense} series circuit is the amplifier's load. Major specifics of the elements of the system are regarded below. The measurement data will be taken with an oscilloscope and processed with a computer software and this is out of the scope of this report.

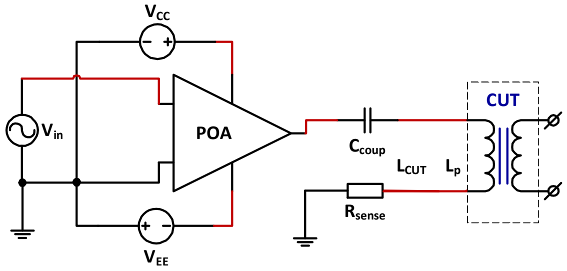


Fig. 2. Basic electrical connections of the measurement system envisaged to be utilized

A. Essential Requirements to the Power Amplifier Circuit

The essential requirements to the power amplifier circuit are basically imposed by the measurements intended to be carried out and may be summarized as follows:

- sinusoidal output voltage, no dc bias;
- high frequency capability;
- high voltage, high current capability.

While the first is a strict requirement, the two latter requirements are not that stringent for the present. As can be seen in Table 1, the voltages and currents needed vary with varying the aimed B_{peak} and f_{op} conditions. In general, for to achieve these same B_{peak} and f_{op} conditions with the same ferrite grade, there will be needed lower values of $U_{p,peak}$ and $I_{p,peak}$ if the same turns' number N_p but a smaller core are used for the tests. At present, there are no precise definitions of prospective CUTs. Rather, the aim of the power amplifier circuit design is to achieve as high frequency and high-power capabilities, as possible and reasonable. Targeted measurements are in the range "tens of kilohertz to megahertz", since these are the frequencies at which modern switching converters (and the corresponding magnetic components, respectively) are operated.

B. Decided Power Amplifier Circuit Realization

It is decided, the amplifier circuit to be built on the basis of an off-the-shelf operational amplifier integrated circuit (IC). For the purpose, two ICs are regarded – OPA548 of Texas Instruments [6] and PA107DP of APEX Microtechnology [7]. Both the ICs are power operational amplifiers (POA) and have class A/B biasing of the output stages for optimum linearity. Main parameters of the two ICs are listed in Table 2.

TABLE 2. MAIN PARAMETERS OF THE REGARDED OPERATIONAL AMPLIFIER ICS

Parameter	Unit	OPA548	PA107DP
Supply voltage (V+4V–)	V_{max}	60 (±30)	200 (±100)
Maximum continuous current output	A_{rms}	3	1.5
Voltage output	V	(V+) – 3.7; (V–) + 3.3	|V±| – 10
Slew rate, typ	V/µs	10	3000
Gain-bandwidth product	MHz	1	180
Full-power bandwidth	kHz	60 ($54V_{p-p}$)	2000 (170 V_{p-p})
Output current limit	A	± 5	n.a.
Thermal shutdown	-	yes	n.a.
Operational amplifier configuration	-	inverting, noninverting	inverting only

C. Amplifier Power Supply

The POA will be supplied in a bipolar mode using the V_{CC} and V_{EE} supplies, as shown in Fig. 2. In the physical implementation of the set up, each of the V_{CC} and V_{EE} supplies will be a set of four separate ac/dc switch-mode converting modules whose outputs can be connected in series. The nominal dc voltage of each module is 24 V. With this configuration, in terms of the POA rails' voltages variability, four general discrete settings will be available – from 24 V to 96 V, with a step of 24 V. In addition, the dc voltage of each ac/dc converting module may be finely adjusted within the interval 21-28 V, which gives additional degree of freedom for tuning the amplifier rails' voltages.

D. Operational Amplifier's Load

The load, as seen by the amplifier's output, consists of the C_{coup}-L_{CUT}-R_{sense} elements, as shown in Fig. 2. The purpose of the capacitor C_{coup} is to reject the inherent dc offset component of the op amp's output voltage (coupling capacitor); its value is set to 100 µF. The inductor L_{CUT} represents the inductance of the primary winding of the test transformer and its value depends upon the CUT and the turns' number N_p. The current-sense resistor R_{sense} will be below 1 Ω. Figure 3 exemplifies the impedance of the overall load for two different values of L_{CUT}.

As can be seen in Fig. 3, above 10 kHz the load that the op amp output will have to see will be approaching a pure inductive load. In terms of the POA ICs utilization, this means that the VA product needed to be supplied to the primary winding, must be dissipated as a real power by the operational amplifier itself.

III. SIMULATION INVESTIGATION OF THE POWER AMPLIFIER

The simulation investigation of the power amplifier circuit is an important part of the ongoing research and the results of it serve a reference point in the progress of the dedicated measurement system development. For the

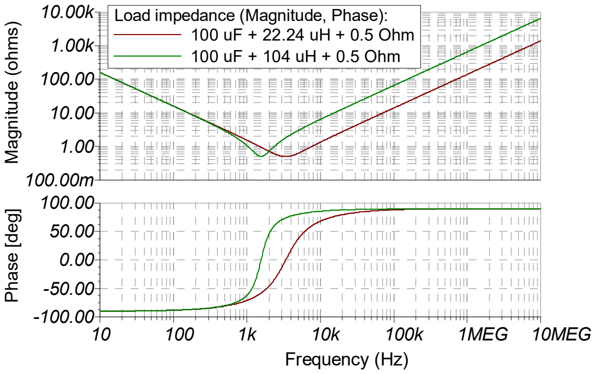


Fig. 3 Exemplary impedance of the operational amplifier's load

purposes of the investigation, simulation models are built in TINA-TI software [8] using the spice models of the regarded ICs [9, 10]. The simulation models are shown in Fig. 4. The OPA548-based amplifier variant is decided to be configured in a non-inverting mode and the PA107DP-based amplifier variant is in the only realizable inverting mode. With the so constructed models there are investigated the closed-loop frequency responses (CLFR) of the amplifier variants having the load connected to their outputs.

As stated earlier, there are no precisely defined cores to be tested but still there are prospective cores for carrying out measurements. These cores are listed in Table 3, along with the respective values of the test inductor L_{CUT}, which as can be seen, depends upon the particular CUT. In order to explore the amplifiers' CLFR with respect to different CUTs, the first set of simulations performed regards two different L_{CUT} values at a constant gain value. For comparison, the gain of an unloaded output of the amplifiers is also taken into account. The results obtained are shown in Fig. 5.

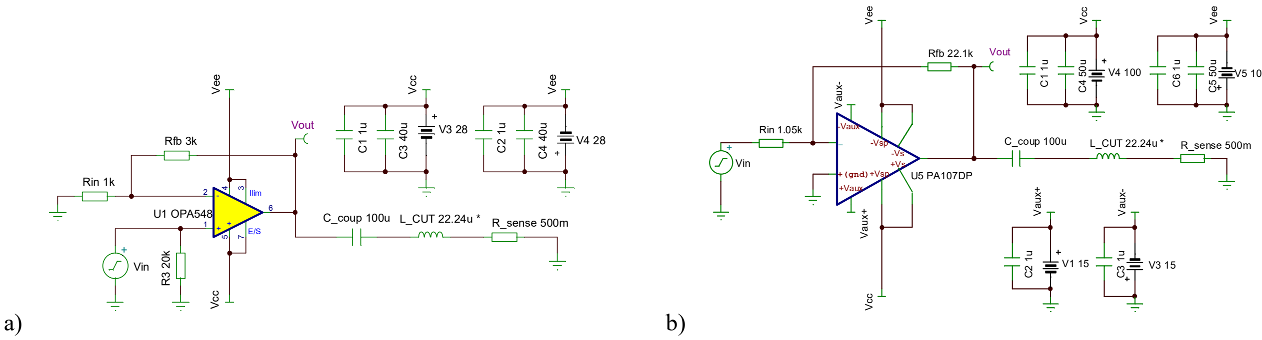
TABLE 3. CORES ENVISAGED FOR POWER LOSS MEASUREMENTS

Prospective inductor L_{CUT}				
CUT	Inductance factor [nH/turns^2]	Inductance [µH] @ $N_p = 4$	Impedance, [Ω]	
			@ 10 kHz	@ 100kHz
PQ50	6500	104 uH	6.53	65.31
R36	2940	47.04 uH	2.95	29.54
R18.4	2950	47.2 uH	2.96	29.64
R17	1390	22.24 uH	1.4	13.97

From Fig. 5 it may be deduced how the load influences the CLFR of the amplifiers. A considerable effect is observable with the OPA548, where both the gain and phase curves are significantly affected. It may be seen that the resonant frequencies of the load impedances, shown in Fig. 3, are the frequencies at which resonant disturbances occur in the OPA548 gain-phase responses. When L_{CUT} has a higher value, the disturbances are less pronounced, which suggests that this amplifier will perform better if loaded with higher value inductances. Another approach would be to use a coupling capacitor with a higher value, which would lower down the resonant frequency of the load impedance.

On the other hand, the CLFR of PA107DP is just slightly affected by the load with a somewhat decreased gain level at the lower inductance, however without resonance; unlike the OPA548 phase response, the PA107DP phase curve seems to be not affected by the load at all.

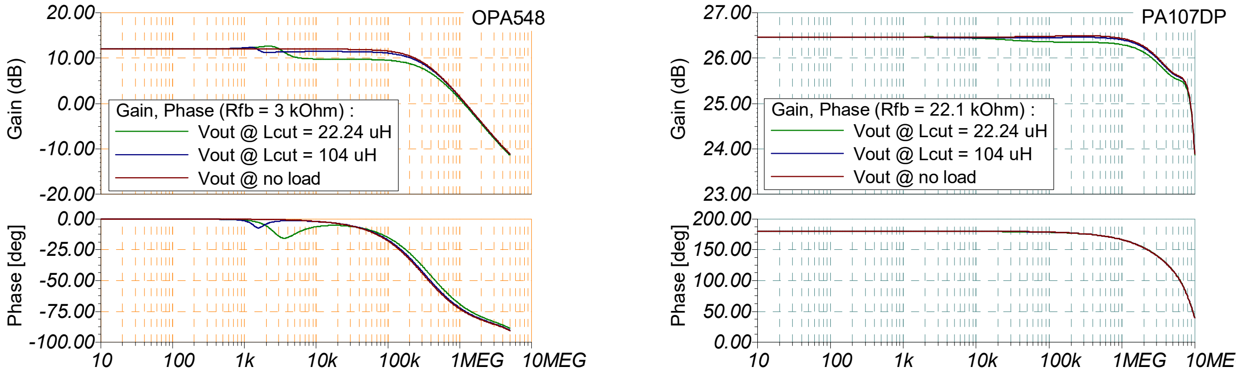
The second set of simulations is with regard to different gain factors. With the OPA548 amplifier, voltage gain of 4,



a)

b)

Fig. 4. Simulation models of the regarded operational amplifier circuits: *a)* model with OPA548 and *b)* model with the PA107DP



a)

b)

Fig. 5. Frequency response of the amplifiers with different values of the test inductor: *a)* OPA548 circuit and *b)* PA107DP circuit

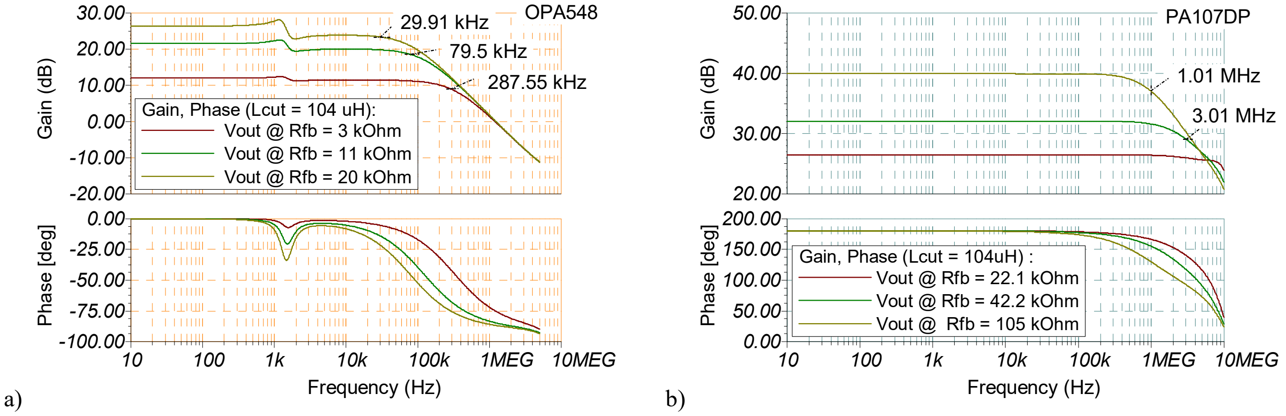


Fig. 6. Frequency response of the amplifiers with different values of the feedback resistor: *a)* OPA548 circuit and *b)* PA107DP circuit

12 and 21 is considered and with the PA107DP amplifier – gain of ~ 20, 40 and 100. The concrete values of the lowest gains in use are chosen on the basis of the gain-bandwidth product of the ICs and recommendations given in the op amps' datasheets. Based on the previous results, this set of simulations is carried out with the higher value of L_{CUT}. The respective results obtained are given in Fig. 6.

From the graphs in Fig. 6, it is obvious that the CLFR curves of the OPA548 op amp are exhibiting great dependance on the gain factor with the given load conditions – as the gain increases, the amplitude of the disturbances in the gain curve are also increasing and there is also increasing dip in the phase curve. From this observation it could be concluded that lower gain factor is preferable for utilizing this IC with the given application.

With regard to PA107DP, it is noticeable in the results in Fig. 6, that both the gain and the phase curves exhibit quite smooth behavior with all the gain factors considered.

At last, from the obtained results, depicted in Fig. 6, there are extracted the corner frequencies (-3dB) with the different gain factors for the two ICs. Respective details are summarized in Table 4.

TABLE 4. CLFR DETAILS OF THE REGARDED REALIZATIONS OF THE AMPLIFIER CIRCUIT

POA	R_{in} [kΩ]	R_{fb} [kΩ]	Gain		Cutoff frequency (-3dB)
			dB	Voltage ratio	
PA107DP	1.05	22.1	26.46	21.04	> 10 MHz
		42.2	32.08	40.18	3.01 MHz
		105	40	100	1.01 MHz
OPA548	1	3	12.02	3.99	287.55 kHz
		11	21.56	11.97	79.5 kHz
		20	26.42	20.94	29.91 kHz

IV. CONCLUSION

From the competitive investigation of two op amp ICs for developing an amplifier circuit dedicated for core loss measurements, it may be deduced that the PA107DP is likely to outperform OPA548 in terms of frequency response smoothness, i.e. it will have more predictable behavior of the gain setting. The latter IC is applicable at lower frequencies and lower output voltages, but it offers higher output current.

In terms of the utilization of the two ICs, from the simulation results obtained, two general conclusions may be drawn: *i)* a higher inductance value of the test transformer primary winding is preferable to be used and *ii)* operating the ICs at low gain is workable and even preferable (OPA548).

A next step of the research being carried out is to prototype a power amplifier printed circuit board based on the PA107DP IC. Another direction of work is to investigate for linearity problems with both the amplifier ICs which might not be obvious with the results presented here.

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