

Efficiency Investigation of BUCK DC-DC Converter with ZVS Using SPICE

Georgi Kunov¹, Tihomir Brusev² and Elissaveta Gadjeva³

Abstract – In this paper the efficiency of BUCK DC-DC converter with Zero Voltage Switching (ZVS) is an object of investigation. A simulation scheme of Gate Driver with Adaptive Dead Time (ADT) is proposed, which provides the independence of ZVS from the current value at which the transistors are switched. The influence on the switching losses of an externally connected drain-source capacitor is simulated using *PSpice*. Macros in the graphical analyzer *Probe* are proposed for calculating the average value of the currents, the losses in transistors and the efficiency. The simulation results are presented graphically as a function of the junction temperature.

Keywords – Power electronics, Switch mode power supply, Buck DC-DC converters, Zero Voltage Switching.

I. INTRODUCTION

The switched mode DC-DC converters are widely used to convert one level of electrical voltage into another level by switching action. These converters have received an increasing deal of interest in many areas, such as: cellular phones, tablets, laptops, radio-frequency power amplifiers, light emitting diode (LED) drivers, etc.

The most commonly used is the BUCK DC-DC converter with Pulse-Width Modulation. Recently, due to its better efficiency, the BUCK DC-DC converter with ZVS is approved. This type of control, with respect to their principle of operation, is similar to Hysteresis Current Mode Control (HCMC).

The BUCK DC-DC converter with HCMC and ZVS is characterized in that the lower hysteresis level has a minimum negative value and is a constant. The regulation of the output power is performed by changing the upper hysteresis level [1, 2]. The application of this control approach leads to optimal output-voltage transient response [3,4] in addition to improving the efficiency.

A subject of the present paper is the construction of a simulation model of BUCK DC-DC converter with HCMC and ZVS, which allows efficiency investigation.

An example study is performed using Infineon's SPICE Model of the transistor BSC024NE2LS [5].

II. BUCK DC-DC CONVERTER WITH HCMC AND ZVS

A. Power Circuit and Control System

The power circuit of the BUCK DC-DC converter is shown in Fig. 1. The selected SPICE model for the transistors Qt (top) and Qb (bottom) allows the study to be performed depending on the crystal temperature of the transistors.

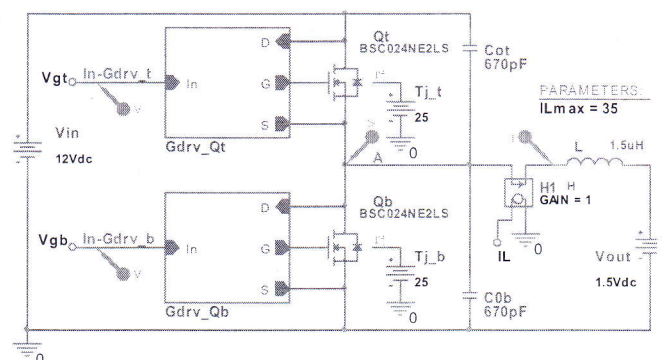


Fig. 1. BUCK DC-DC Converter

The control system of the DC-DC converter with HCMC and ZVS is shown in Fig. 2. Using the comparators EL (low level) and EH (high level), pulses are generated, corresponding to the Low and High Level of the current I_L through the inductor L .

The comparator is realized by the Analog-Behavioral Model (ABM) element of EFREQ type using the function: $5 * (\text{sgn}(V(\% \text{IN}+, \% \text{IN}-)) + 1) / 2$. The comparator EL sets the R-S trigger (U1,U2) in state "1" and as a result the transistor Qt is turn-on and the transistor Qb is turn-off.

The comparator EH sets the R-S trigger in state "0", whereby the transistor Qt is turn-off and the transistor Qb is turn-on.

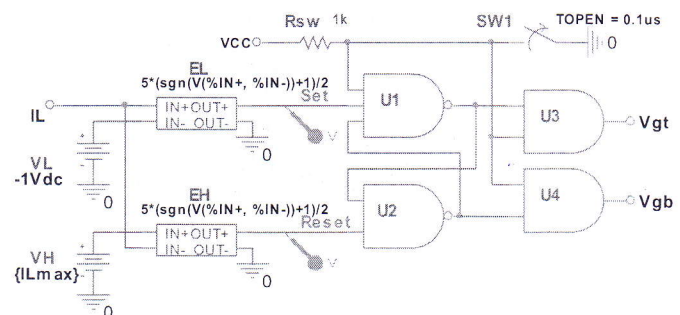


Fig. 2. Hysteresis current mode control system

¹Georgi Kunov is with the Faculty of Electronic Engineering and Technologies, Technical University of Sofia, Kl. Ohridski 8 Blvd., 1797 Sofia, Bulgaria, E-mail: gkunov@tu-sofia.bg

²Tihomir Brusev is with the Faculty of Telecommunications, Technical University of Sofia, Kl. Ohridski 8 Blvd., 1797 Sofia, Bulgaria, E-mail: brusev@ecad.tu-sofia.bg

³Elissaveta Gadjeva is with the Faculty of Electronic Engineering and Technologies, Technical University of Sofia, Kl. Ohridski 8 Blvd., 1797 Sofia, Bulgaria, E-mail: egadjeva@tu-sofia.bg

The principle of operating of the control system is illustrated by the waveforms shown in Fig. 3.

The value $I_{L,LowLevel} = -1A$ is selected for the low level of the current I_L . The high level of the current I_L is a simulation parameter and changes in the range from 2A to 35A.

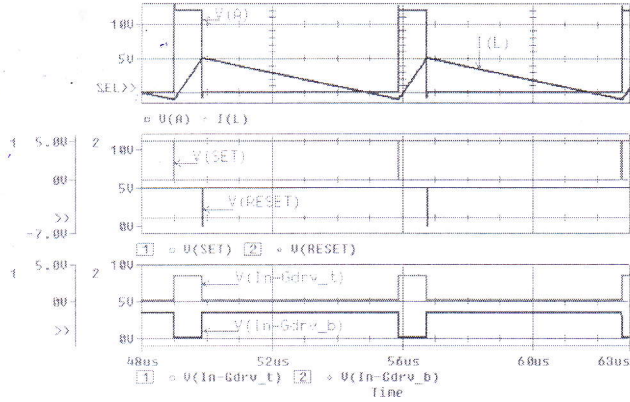


Fig. 3. Waveforms illustrating the principle of operation of BUCK Converter with ZVS

In this case of HCMC, the switching frequency depends on the hysteresis window ΔI_L [6]:

$$f_{sw} = \frac{1}{L\Delta I_L} \cdot \frac{V_{out}(V_{in} - V_{out})}{V_{in}}, \quad (1)$$

where

$$\Delta I_L = I_{L,HighLevel} - I_{L,LowLevel}$$

B. Gate Driver with Adaptive Dead Time

In order for ZVS to be possible, it is necessary the transistor turn-on pulse V_{gs} to be applied after the moment when the output capacitance of the MOSFET transistor is discharged by the current I_L during the dead time (DT).

The duration of DT (t_{DT}) is a function of the instantaneous value of the current $I_{L,HighLevel}$. The Gate Driver scheme with adaptive dead time is shown in Fig. 4. In this case, the index "t" corresponds to the top Gate Driver (for the bottom Gate Driver the index "b" is used).

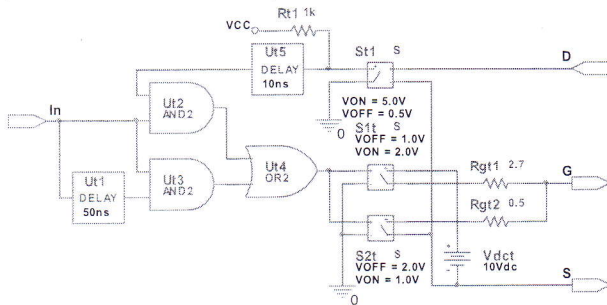


Fig. 4. Gate Driver with Adaptive Dead Time

Using the voltage-controlled switch St1 and the delay element Ut5, a comparator model is realized (with propagation time 10ns).

When the voltage V_{ds} is less than 0.5V, the logical element Ut2 allows the applied pulse at the input In to reach the transistor's gate. The delay element Ut1 and the logical element Ut3 form a maximum value of t_{DT-max} . This value is needed by the starting the DC-DC converter, since then the current $I_L = 0$. The switches S1t and S2t represent a classical driver of two transistors ($n-p-n$ and $p-n-p$).

III. SIMULATION RESULTS

The BUCK DC-DC converter with HCMC and ZVS is investigated using the program Cadence PSpice [7]. The simulation is performed for the time interval from 0 to 250 μs .

The following macro-definitions in the graphical analyzer Probe are defined for the postprocessing of the simulation results:

- The values of the currents and voltages in top and bottom power MOSFET transistors:

$$I_{d_b} = I(Qb:DD)$$

$$I_{d_t} = I(Qt:DD)$$

$$V_{ds_b} = V(Qb:DD)$$

$$V_{ds_t} = V(Qt:DD) - V(Qt:S0)$$

- The values of dissipated power in top and bottom power MOSFET transistors:

$$P_{ds_t} = V_{ds_t} * I_{d_t}$$

$$P_{ds_b} = V_{ds_b} * I_{d_b}$$

- The average value of dissipated power:

$$avg_P_{ds_b} = \max(S(M(P_{ds_b}))/249us)$$

$$avg_P_{ds_t} = \max(S(M(P_{ds_t}))/249us)$$

- The average value of the output current and output power:

$$I_{out} = YatX(AVG(I(L)), 250u)$$

$$P_{out} = 1.5 * I_{out}$$

- The efficiency:

$$efficiency = P_{out} / (P_{out} + avg_P_{ds_t} + avg_P_{ds_b})$$

The macros thus defined can be reused.

The waveforms illustrating the ZVS transistor switching are presented in Fig. 5 as follows:

- Fig. 5a and Fig. 5c – Qb-off, Qt-on ($I_L = -1A$);
- Fig. 5b and Fig. 5d – Qt-off, Qb-on ($I_L = 35A$);
- Fig. 5a and Fig. 5b – without additional capacitor drain-source (only with parasitic capacitance $C_o = 650pF$ of transistor BSC024NE2LS);
- Fig. 5c and Fig. 5d – with additional capacitors $C_{ot} = C_{ob} = 670pF$.

The switching losses P_{ds-t} and P_{ds-b} are presented on the coordinate systems (1) and (2). It is seen that the main switching losses are in the transistor Qt, at the moment of its turn-off, when the current $I_L = 35A$. The additional capacitor C_{ot} leads to a two-fold reduction of the amplitude of P_{ds-t} , but at the expense of longer duration.

The input pulses $InGdrv_t$ and $In-Gdrv_b$ of the Gate Driver are shown on the coordinate system (3), plot 1 and the gate pulses V_{gs_t} and V_{gs_b} – on plot 2.

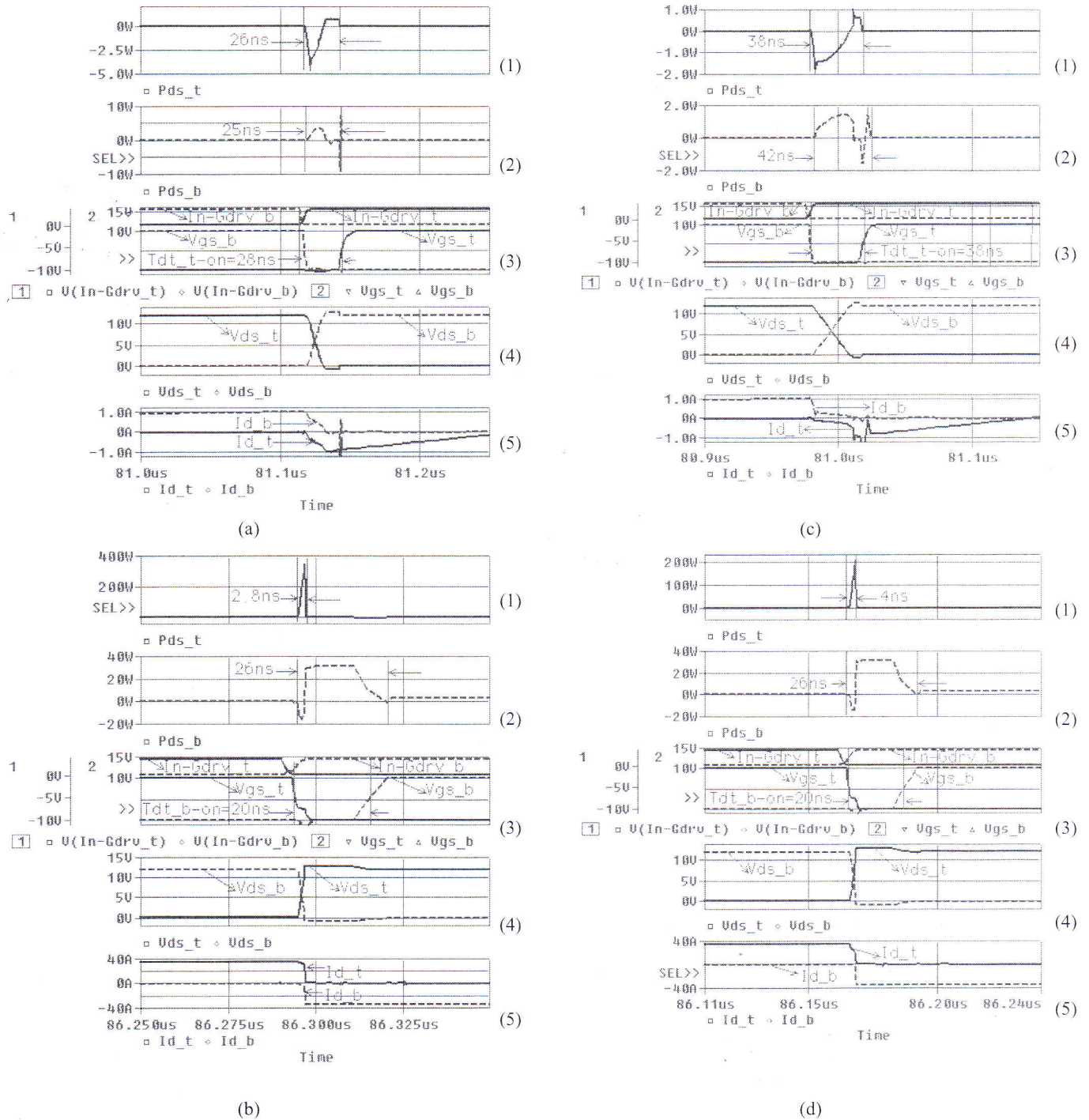
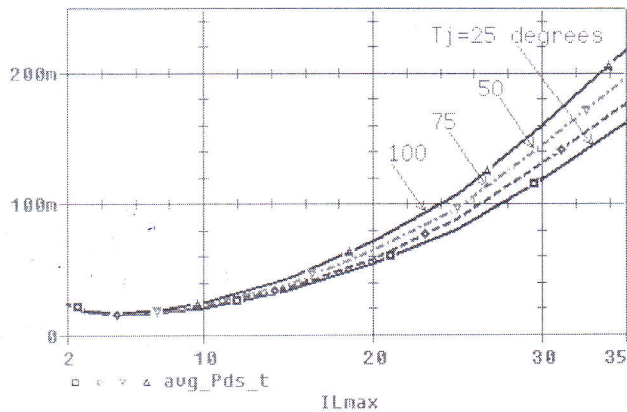


Fig. 5. Waveforms illustrating ZVS processes by $I_{L-High\ Level}$ and $I_{L-Low\ level}$

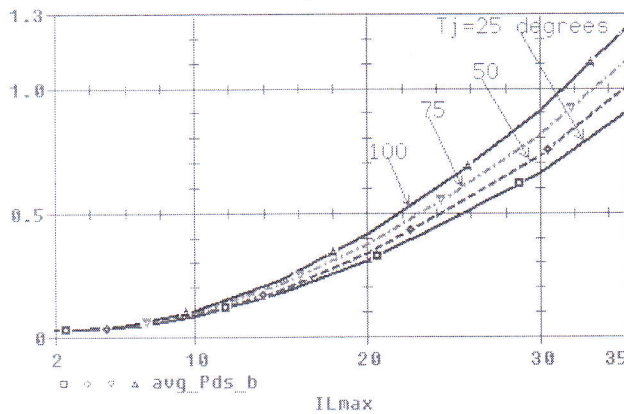
It is seen that the dead time for the transistor Q_t increases twice when the additional capacitor C_{ot} is connected. For the dead time for transistor Q_b , there is no change when the additional capacitor C_{ob} is connected, which can be explained by the large value of the switching current (at this time moment $I_L = 35A$).

The voltages V_{ds_t} and V_{ds_b} are shown on the coordinate systems (4). The additional capacitor C_{ot} leads to reducing the slope of the drain-source voltage.

By comparing the V_{ds_t} and V_{ds_b} waveforms with V_{gs_t} and V_{gs_b} waveforms from the coordinate system (3) – plot 2, it can be seen that the gate pulses reach the corresponding transistors when the drain-source voltage has become 0V. On the coordinate system (5) the waveforms I_{d_t} and I_{d_b} are presented. Fig. 6 shows the dependencies of the losses P_{ds_t} and P_{ds_b} in the MOSFET transistors as a function of the current I_{Lmax} for different junction temperatures. The macros described above are used and the *Append* function in the graphical analyzer *Probe* is applied.



(a)



(b)

Fig. 6. Dependences of MOSFET transistor losses in a function of I_{Lmax} for different junction temperatures: a) P_{ds-t} ; b) P_{ds-b}

Fig. 7 shows the dependency of BUCK converter efficiency as a function of the current I_{Lmax} for different junction temperatures. Fig. 8 shows the dependencies of the output power P_{out} ; the output current I_{out} and the average transistor currents: I_{d-t} and I_{d-b} as a function of the current I_{Lmax} .

CONCLUSION

The efficiency of BUCK DC-DC converter with ZVS has been studied. The scheme of the proposed Gate Driver allows obtaining of Adaptive Dead Time which ensures ZVS independently from the value of the switching current. The average values of the currents and the losses in transistors are simulated depending of the maximum value of the output current. The influence of the additional drain-source connected capacitor on the Adaptive Dead Time, as well as on the peak value of the switching losses is investigated.

ACKNOWLEDGEMENT

The investigations are supported by the project FNI E02-8 /2014.

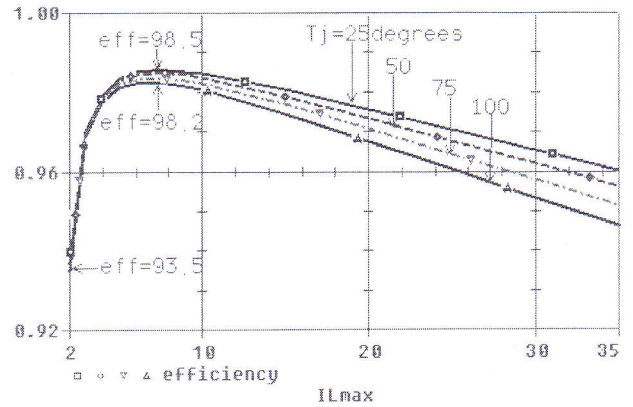


Fig. 7. Current dependences of BUCK converter efficiency in a function of the junction temperature

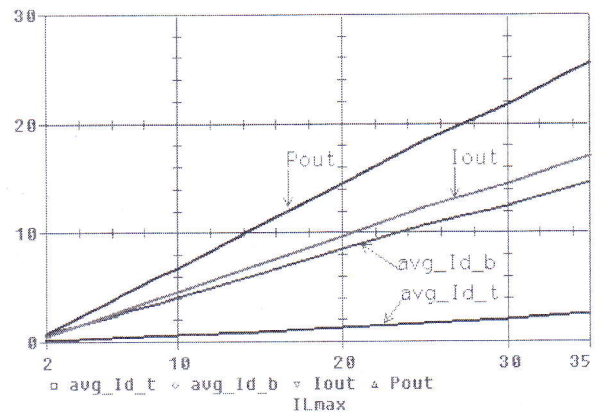


Fig. 8. Dependence of: output power P_{out} ; output current I_{out} and average transistor currents I_{d-t} and I_{d-b}

REFERENCES

- [1] S. Chen, O. Trescases, and W.T. Ng, "Fast Dead-Time Locked Loops for a High-Efficiency Microprocessor-Load ZVS-QSW DC/DC Converter", *IEEE Conference on Electron Devices and Solid-State Circuits, EDSSC'03*, pp. 391-394, 2003.
- [2] S. Zhou, and G. A. Rincon-Mora "A High Efficiency, Soft Switching DC-DC Converter With Adaptive Current-Ripple Control for Portable Applications", *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol. 53, no. 4, April 2006.
- [3] A. Borrell, M. Castilla, J. Miret, J. Matas, and L. Vicuna, "Simple Low-Cost Hysteretic Controller for Multiphase Synchronous Buck Converters", *IEEE Transactions on Industrial Electronics*, vol. 58, no. 6, June 2011.
- [4] L. Kisun, et al., "A Hysteretic Control Method for Multiphase Voltage Regulator", *IEEE Trans. on Power Electronics*, vol. 24, no.12, pp. 2726-2734, Dec. 2009.
- [5] Infineon-SimulationModel_OptiMOS_PowerMOSFET_PSpice_25V_N-Channel-SM-v01_00-EN <http://www.infineon.com/cms/en/product/promopages/power-mosfet-simulation-models/>
- [6] G. Kunov, T. Brusev, and E. Gadjeva, "Multiphase BUCK DC-DC Converter with Zero Voltage Switching", *18th International Symposium on Power Electronics*, Novi Sad, Serbia, 28-30 October, 2015.
- [7] PSpice User's Guide, Cadence PCB Syst. Division, 2000.