Design of Integrated Switching-Mode Amplifier on CMOS 0.35 μm Process

Tihomir Brusev[1], Georgi Kunov[2] and Elissaveta Gadjeva[3]

Abstract –**An integrated two-phase interleaved dc-dc converter designed on CMOS 0.35 μm process, is proposed in this paper. Switching-mode amplifiers deliver large amount of energy to the transmitter's power amplifier (PA) in the fourth generation (4G) long term evolution (LTE) wireless communication standard. The received results proved that tracking speed can be increased if two-phase switching-mode amplifier is used instead of single phase architecture. The simulation results show proper work of the designed circuit after layout design. The simulated efficiency of the converter is about 73% at particular case of 60 mA load current.**

Keywords – **Switching-mode amplifiers, CMOS 0.35 μm process, Cadence.**

I. Introduction

The portable electronic devices nowadays have extremely big functionality. This is connected with large amount of energy consumed from the battery. The increasing of the time between two consecutive charges becomes a big challenge. Efficient power conversion is the key to saving battery energy.

Switching-mode regulators are circuits which indicate high efficiency results [1]. In the new 4G LTE wireless communications standards those circuits usually work in hybrid architectures with linear amplifier [2], as a part of power supply circuits which deliver the energy to transmitter's power amplifier (PA) [3]. The disadvantage of the switching-mode amplifiers is that they are low bandwidth circuits [4]. However, the majority of the energy to the transmitter's PA is provided from them [5].

The portion of power ensured from high efficient switching-mode amplifiers can be increased if instead of low tracking speed single phase dc-dc converter, a multiphase dc-dc converter's architecture is used. Thus the overall efficiency of the envelope tracking power amplifier system could be improved. Envelope tracking power amplifier (ET PA) is the widespread used technique for efficiency enhancement [6].

Envelope amplifier in this technique ensures dynamically changeable supply voltage to the PA. Thus the modulated drain voltage is delivered to power amplifier according to the input envelope signal [7].

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The basic principles of operation of single phase and two-phase buck dc-dc converters are discussed in Section II of this paper. The investigation results of tracking speed possibilities of both circuit's architectures, designed on CMOS 0.35 μm process, are presented in Section III. The integrated circuit (IC) layout design of two-phase buck interleaved dc-dc converter is presented in Section IV.

II. Switching-mode DC-DC Converters

A. Buck DC-DC Converters

The switching-mode dc-dc converters are widely used as power supply circuits in integrated circuit applications, for low power mobile wireless communication devices. Their main advantage is that they have high efficiency characteristics. Theoretically efficiency η of switching-mode dc-dc converters is 100%. In practice due to the power losses in the building circuit's components, the real integrated dc-dc converters can indicate efficiency η values close or greater than 90%.

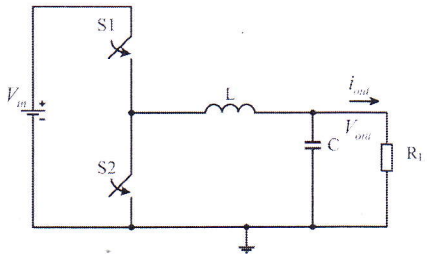

Fig. 1. Basic circuit of buck dc-dc converter

The schematic of buck dc-dc converter is shown in Fig. 1. It consists of two switches (*S1* and *S2*) and low-pass filter, formed by inductor *L* and capacitor *C*. In the basic circuit topology the function of *S1* is performed by transistor work as a switch, while a diode is used for *S2*. For low power applications instead of diode the function of *S2* is performed by another transistor. In such way the losses coming from voltage drop of the diode can be escaped. The two switches are synchronously regulated in a way that when one of the transistors is switched-on the other is switched-off.

Pulse-Width Modulation (PWM) is one of the methods that are used for control of *S1* and *S2*. The principle of operation of PWM control technique is shown in Fig. 2 [1]. The error signal voltage is formed by amplifying the difference between the actual output voltage V_{out} and the desire voltage level V_{ref}. The switching frequency f_s of buck dc-dc converter is determined by frequency of the ramp generator. The switch

control signal is formed at the output of the comparator. This signal determines the states of the buck converter's switches. The frequency f_s is constant for PWM control technique. The PWM control technique is suitable for constant envelope signals, when stable dc output voltage of the converter is desired.

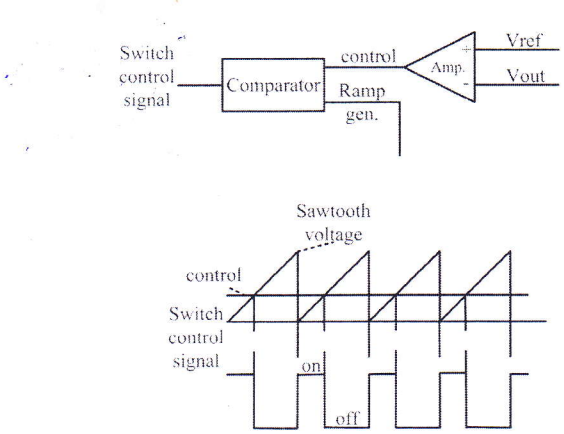

Fig. 2. Principle of operation of PWM control technique for buck dc-dc converter

In the 4G LTE standard, the envelope amplifiers, which have to supply voltage to the PA, should have fast tracking speed because the envelope frequency is increased. The disadvantage of the PWM controlled switching converters is that they are low bandwidth circuits. The switching frequency f_s of the dc-dc converter has to be about ten times higher than the bandwidth of the LTE signal [4].

B. Two-Phase Interleaved Buck DC-DC Converters

The two-phase interleaved dc-dc converter architecture is illustrated in Fig. 3.

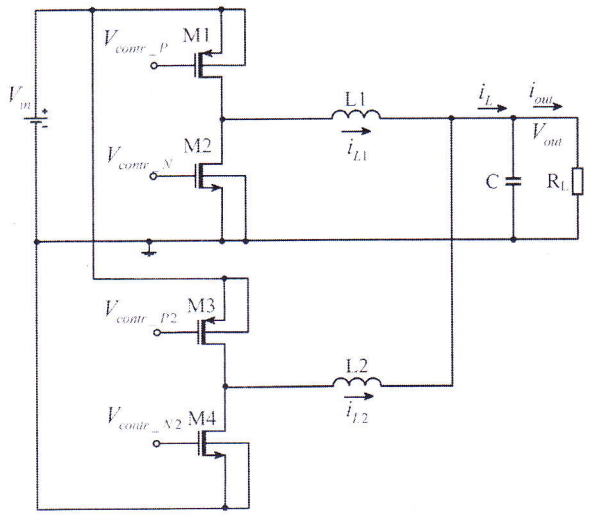

Fig. 3. Two-phase interleaved buck dc-dc converter

This circuit's architecture helps to reduction of the output current ripple Δi_{out} of the converter. This is possible because the phase shifted inductor current ripples respectively of the first and second sub-converter stage Δi_{L1} and Δi_{L2} are summed at the output. The output current ripple Δi_{out} of the two-phase interleaved buck converter with non-coupled inductors can be expressed in the form [8]:

$$\Delta i_{out} = \frac{V_{out}}{L}(1-2D)T_s, \tag{1}$$

where T_s is the switching period of converter, L is the value of filter inductors if L_1=L_2. If the duty cycle of the converter D is close to 0.5 then minimum values of the output current ripples Δi_{out} could be obtained. The inductor current ripples of the single phase buck dc-dc converter and two-phase interleaved buck converter with non-coupled inductors have equal values Δi_L, and can be expressed in the form [8]:

$$\Delta i_L = \frac{V_{out}}{L}(1-D)T_s. \tag{2}$$

The architecture of two-phase interleaved dc-dc converters permits to be obtained equal output current ripples as those of single-phase dc-dc converters using smaller inductance values of output filter inductors. Therefore those circuits can be used for LTE applications, when envelope amplifier has to be fast in order to track high frequency envelope signal. For example two-phase interleaved dc-dc converter can be used instead of the single phase switching-mode regulator in hybrid envelope amplifier structure. This will result in higher part of energy distributed from high efficient switching-mode dc-dc converter, leading to efficiency increasing of envelope amplifier. The reason is that the portion of power distributed from low efficient linear amplifier to PA will be smaller, compared to the case when switching-mode amplifier is a single phase dc-dc converter.

III. Investigation of PWM Controlled Two-Phase Switching-Mode Amplifier

Two-phase interleaved buck dc-dc converter controlled with PWM technique is designed on CMOS 0.35 µm. The block circuit is presented in Fig. 4.

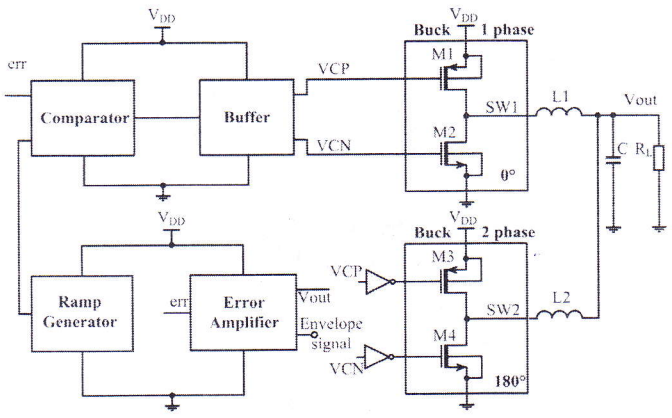

Fig. 4. PWM controlled two-phase switching-mode amplifier

The load resistance R_L of the dc-dc converter represents the current load of RF power amplifier. LTE envelop signal is simulated using source signal with sinusoidal waveform with frequency equal to 20 MHz. The sinusoidal signal emulates fast changing LTE envelope and it is used in this simulations as a test signal to evaluate the tracking speed of the two-phase interleaved buck dc-dc converter. The waveforms of the control signals VCP and VCN, which control the modes of operation respectively of the power transistor *M1* and *M2* of the first sub-converter, are presented in Fig. 5.

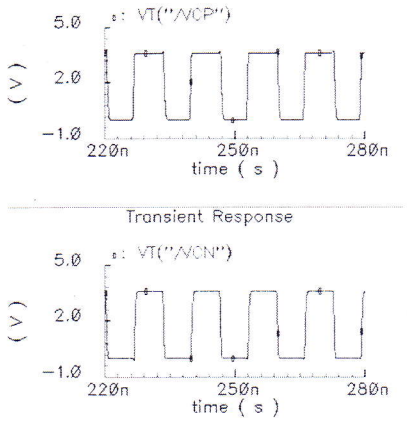

Fig. 5. The waveforms of the control signals VCP and VCN

The voltage signals VT("SW1") and VT("SW2"), which are respectively the outputs of the first and second buck sub-converter stages, are presented in Fig. 6. The simulation results demonstrate the synchronous operation in the both sub-converter stages.

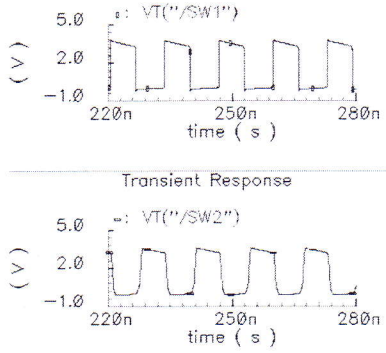

Fig. 6. The waveforms of output voltage signals VT("SW1") and VT("SW2")

The two voltage signals (VT("SW1") and VT("SW2")) are phase shifted on 180°. The waveforms of i_{L1}, i_{L2} and i_{out} of two-phase interleaved buck dc-dc converter are presented in Fig. 7. In this concrete case the average value of the output voltage $V_{out(av)}$ of the two-phase converter is equal to 1.6 V. The obtained results show that Δi_{L1} is equal to 88 mA, Δi_{L2} is equal to 83 mA, while Δi_{out} is equal to 5 mA. The average value of the output current $I_{out(av)}$ of the two-phase switching-mode converter is equal to 55 mA. The simulation results show that Δi_{out} is about 16 times lower than Δi_{L1} and Δi_{L2}, for these particular output parameters of the designed circuit.

Single phase and two-phase buck dc-dc converters are investigated at the same conditions. The average values of the output voltages $V_{out(av)}$ of both converters are regulated to be equal to 1.6 V. The values of passive components of low-pass filters of the converters are 125 nH for filter inductors and 5 pF for filter capacitors. The average value of the load current of two-phase dc-dc converter $I_{out(av)}$ is two times higher than in the single-phase circuit.

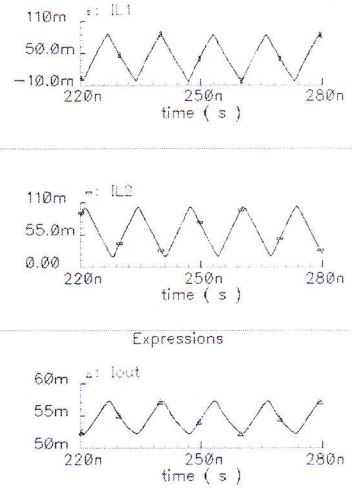

Fig. 7. The waveforms of i_{L1}, i_{L2}, and i_{out} of two-phase buck dc-dc converter

The simulation results presented in Table I show that Δi_{out} of the two converters have equal values, while output voltage ripple ΔV_{out} of single-phase converter is 2.3 times higher than ΔV_{out} of two-phase converter.

TABLE I
SINGLE PHASE AND TWO-PHASE SWITCHING-MODE BUCK DC-DC CONVERTERS INVESTIGATION RESULTS

	single phase buck converter	two-phase buck converter
Efficiency [%]	73	72.8
$I_{out(av)}$ [mA]	22.5	50
Δi_{out} [mA]	5	5
ΔV_{out} [mV]	341	148
P_{PMOS} [mW]	3.17	3.94
P_{NMOS} [mW]	10.1	9.8

The efficiency of switching-mode dc-dc converter is equal to:

$$\eta = \frac{P_{out(av)}}{P_{in(av)}}, \quad (3)$$

where $P_{out(av)}$ is the output average power, and $P_{in(av)}$ is the input average power of the converter. If the single-phase converter should deliver the same output voltage ripples, the output capacitance C should be significantly increased, which would impact negatively on the tracking speed of the converter. If a reduction of tracking speed is not acceptable, the large ripples should be compensated by a linear amplifier, which on the other hand would degrade system efficiency.

IV. Layout Design of PWM Controlled Two-Phase Switching-Mode Amplifier on CMOS 0.35 μM Process

The layout of PWM controlled two-phase switching-mode amplifier is designed on CMOS 0.35 μm process using Virtuoso layout tool of Cadence. The whole converter layout, including power stage and control feedback circuits, is shown in Fig. 8. The re-simulation of layout after the extraction of parasitic capacitance is made in order to verify the proper work of the system.

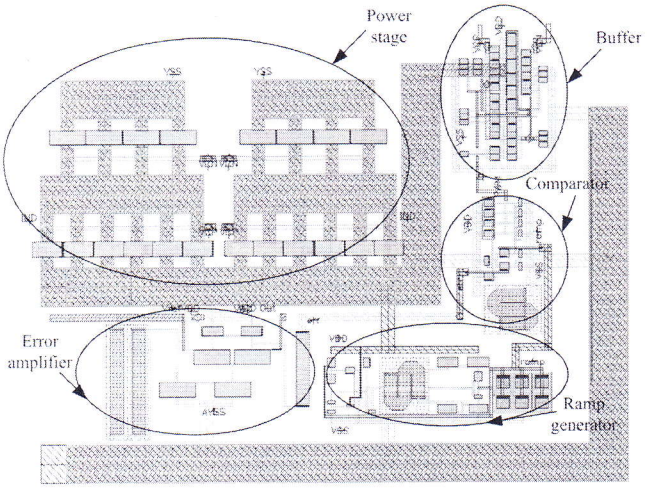

Fig. 8. Layout of PWM controlled two-phase switching-mode amplifier

The simulated waveforms of output current i_{out} of the two-phase buck dc-dc converter, respectively of schematic and layout with extracted parasitics, are presented in Fig. 9.

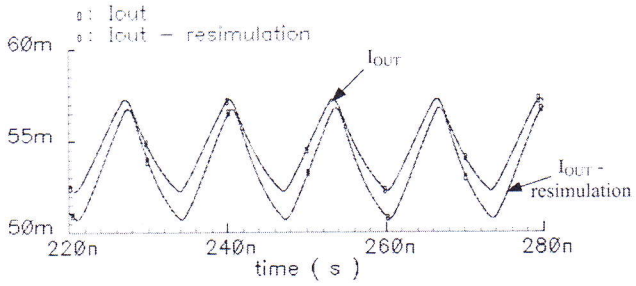

Fig. 9. The waveforms of output current i_{out} of the two-phase buck DC-DC converter

The obtained results shown in Fig. 9 prove the proper work of two-phase switching-mode amplifier after layout design. The slight difference between the two curves is due to the extracted parasitic capacitance. They are formed by overlapping layers of metal used for wiring. The total estimated parasitic capacitance after layout designed is equal to 1.9 pF. More than 90% of overall parasitic capacitance is contributed from power stage of the switching-mode amplifier. All four metal layers connected in parallel are used in order to ensure the output current of the converter. If smaller number of metal layers is used in layout design, the parasitic capacitance could be decreased, but more silicon area will be occupied.

V. Conclusion

Two-phase switching-mode amplifier designed on CMOS 0.35 μm technology has been proposed in this paper. The investigations show that if two-phase switching-mode amplifier is used instead of single phase architecture, tracking speed can be increased. In this way the overall efficiency of envelope amplifier, which delivers the energy of transmitter's PA for LTE applications, could be improved. The proper work of the circuit is proved by re-simulation of the whole system with extracted parasitic capacitance after the layout design.

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