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CONTENTS

Buck Converter Modeling with MATLAB Simulink

Tihomir Sashev Brusev

Abstract – **Switching mode power converters (SMPC) are widely used in the electronics' industry due to their high efficiency. Miniaturization of integrated circuits (IC) leads to decreasing of operating voltages. Modeling of regulator used for low power applications can be good approach for designing of the control circuits. State-space average model of buck converter is considered in this paper. MATLAB Simulink is used for model investigations of dc-dc regulator.**

Keywords – **Buck DC-DC Converter, Modeling, MATLAB Simulink**

I. INTRODUCTION

In the modern life battery powered electronic equipments are used everywhere. Switching-mode buck dc-dc converters, which decrease input dc voltage to another stable output dc voltage level, have high efficiency because their principle of operation [1]. Therefore they are suitable for RF electronic devices which used MEMS components, mobile phones, laptops etc.

Modeling of buck dc-dc converter topology could help to proper and faster design of control circuits. The basic circuit's topology of buck converter is shown in Figure 1 [2].

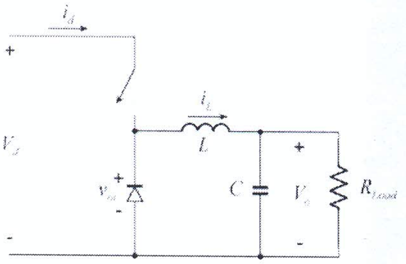

FIGURE 1. BASIC CIRCUIT'S TOPOLOGY OF BUCK CONVERTER.

For low power applications the better choice is synchronous buck converter's topology, which is presented in Figure 2. The efficiency in this structure is higher compare to the basic regulator because voltage drop of the diode is eliminated. CMOS technology is commonly used for designing integrated circuits for low power applications. For two switches in synchronous dc-dc converter regulated by control circuits are used MOS transistors.

In practice the components included in the power stage of converter are not ideal. The two switches (S_1 and S_2) could be represented by their R_{ON} resistance when they are switched-on. With good approximation for low frequency can be assumed that transistors have infinite resistance when they are switched-off. The real model of MOS transistor is much more complex because parasitic capacitance is also included there. From the efficiency point of view high frequency is not desirable, but is needed in order to be reduced sizes and volumes of the filter components.

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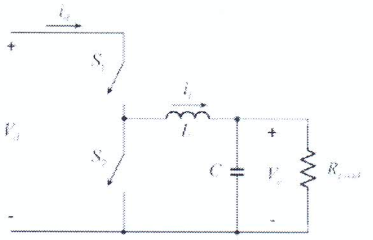

FIGURE 2. SYNCHRONOUS BUCK CONVERTER SCHEMATIC.

The simplest equivalent circuits for the non-integrated filter inductor could be representing by inductance L and series resistance R_L. Integrated inductors model include more parasitic resistances and capacitances. The filter capacitor can be modeled as an ideal capacitor C and series connected ideal resistor R_C, which is parasitic resistance of C.

In Section II of this paper is discussed state-space averaged modeling of buck converter. MATLAB Simulink is used for model investigations of switching mode step-down dc-dc regulator. The received results are presented in Section III.

II. STATE-SPACE AVERAGED MODELING OF BUCK CONVERTER

The switching mode dc-dc converters are time-variant systems, which could be described as time-invariant system during respectively t_{on} or t_{off} time intervals of the main switch S_1 [3]. Pulse width modulation (PWM) control method is common used regulation technique for buck converters. The switching frequency f_s is constant and when main switch *S1* is switched-on *S2* is switched-off. For simplicity of the considered model bellow is assumed that two switches (S_1 and S_2) have equal R_{ON} resistance when they are switched-on. This assumption has to be taking into account during the design of the real circuit of buck converter. The transistors in the power stage should be chosen in such a way that their resistance R_{ON} will be the same.

A. Buck converter switched-on state

In Figure 3 is shown equivalent circuit of the synchronous buck converter when the main transistor (main switch S_1) is switched-on. The currents flowing through the filter inductor and filter capacitor are respectively $i_L(t)$ and $i_c(t)$. The input voltage and input current are denoted as $V_d(t)$ and $i_d(t)$, while $V_o(t)$ and $i_{Rload}(t)$ are output voltage and load current of the power stage.

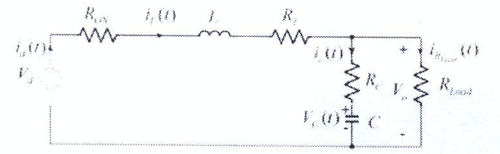

FIGURE 3. BUCK CONVERTER WHEN THE MAIN TRANSISTOR IS SWITCHED-ON.

The state-space equation of regulator in this case can be represented by (1).

$$\begin{cases} \dot{x} = A_1 x + B_1 u \\ y = C_1 x + D_1 u \end{cases} \qquad (1)$$

, where [4]:

$$x = \begin{bmatrix} i_L(t) \\ V_C(t \end{bmatrix} \quad y = \begin{bmatrix} V_o(t) \\ i_d(t) \end{bmatrix} \quad u = V_d(t)$$

For state variables are considered inductor current $i_L(t)$ and capacitor's voltage $V_C(t)$. The coefficients A_1, B_1, C_1 and D_1 in (1) can be expressed as:

$$A_1 = \begin{bmatrix} \frac{\left[R_{ON}(R+R_C)+R_L(R+R_C)+RR_C\right]}{L(R+R_C)} & -\frac{R}{L(R+R_C)} \\ \frac{R}{C(R+R_C)} & -\frac{1}{C(R+R_C)} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 1/L \\ 0 \end{bmatrix} \quad C_1 = \begin{bmatrix} \frac{RR_C}{R+R_C} & \frac{R}{R+R_C} \\ 1 & 0 \end{bmatrix} \quad E_1 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \qquad (2)$$

They could be derived using Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL) for circuit shown in Figure 3.

B. Buck converter switched-off state

In Figure 4 is presented equivalent circuit of synchronous the buck dc-dc converter when the main transistor (main switch S_1) is switched-off. The state-space equations of the converter are:

$$\begin{cases} \dot{x} = A_2 x + B_2 u \\ y = C_2 x + D_2 u \end{cases} \qquad (3)$$

where:

$$A_2 = A_1 \quad B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad C_2 = C_1 \quad E_2 = E_1 \qquad (4)$$

The coefficients A2, B2, C2 and D2 can be derived using Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL).

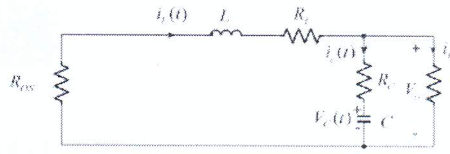

FIGURE 4. BUCK CONVERTER WHEN THE MAIN TRANSISTOR IS SWITCHED-OFF.

III. MODEL SIMULATION OF BUCK CONVERTER USING MATLAB SIMULINK

MATLAB Simulink is very powerful environment for system modeling and simulation. Therefore, it is suitable for various investigations, model examinations and analysis. This software can be used also for high level system design.

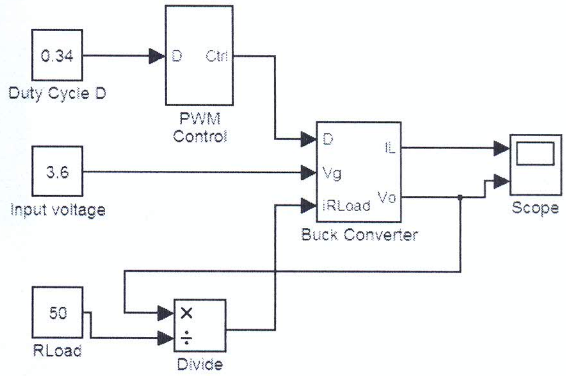

FIGURE 5. THE BENCHMARK CIRCUIT OF BUCK CONVERTER SYSTEM.

In Figure 5 is presented benchmark circuit of simulated buck converter system [5]. It consist pulse-width modulation (PWM) control circuit and power stage of regulator. The input voltage, duty cycle and load resistance can be adjusted. The load current of the investigated system is set to be 24 mA. The input voltage V_d of the modeled buck converter is 3.6 V. Output voltage V_o is regulated to 1.2 V.

The equivalent model of power stage of buck converter is shown in Figure 6 [5].

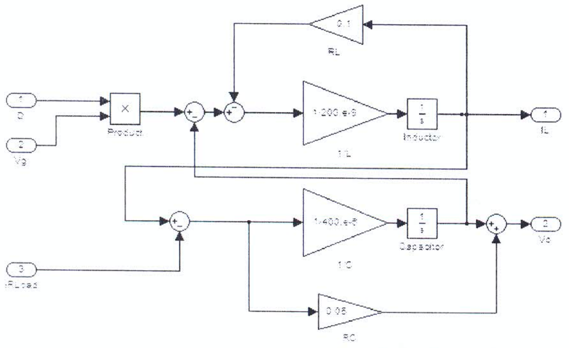

FIGURE 6. EQUIVALENT MODEL OF POWER STAGE OF BUCK CONVERTER SYSTEM.

The filter inductor L of regulator is equal to 200 nH, while filter capacitor C is equal to 400 μF. Block diagram modeling software could save time to design proper control circuits that can satisfy performance conditions of buck converter [6]. The pulse-width modulation (PWM) control circuit modeled with MATLAB Simulink is shown in Figure 7 [5]. The switching frequency f_s can be determined by ramp generator.

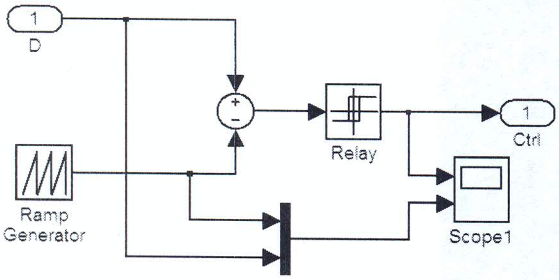

FIGURE 7. EQUIVALENT MODEL OF PWM CONTROL CIRCUIT.

In Figure 8 are presented the waveforms of the signals of PWM control circuit. The control pulses, which regulate the state of the switches S_1 and S_2 of synchronous buck converter, are shown in the first graph. They are formed by comparing of saw-tooth signal generated by ramp generator and duty cycle.

When output signal of ramp generator became higher than duty cycle level control pulses of the power stage of converter are reset to zero. The switching frequency determined from ramp generator f_s is set to 150 MHz. High switching frequency of the buck converter is the key parameter which helps the sizes and volumes of the filter components to be reduced.

The integrated circuit (IC) of dc-dc step-down regulator using CMOS technology has been designed with Cadence. Output and input voltages have same level, respectively V_d=3.6 V and V_o=1.2 V, like those of the modeled system presented in this paper. The switching frequency f_s of the converter is 150 MHz. In Figure 9 is shown output voltage of the designed system as function of the load resistance R_{Load}. The simulations of the whole buck converter including control system with Cadence takes much more time compared to model investigations of regulator with MATLAB Simulink.

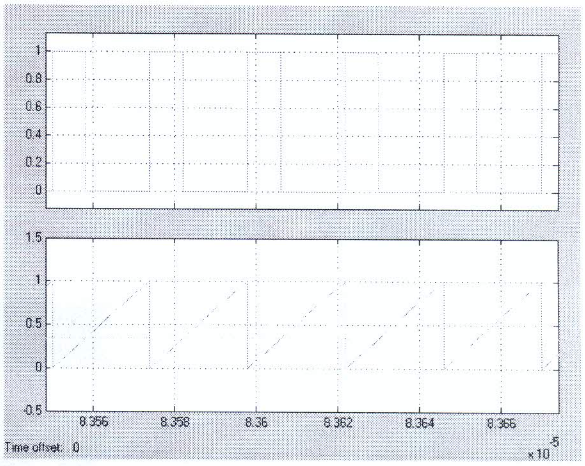

FIGURE 8. THE WAVEFORMS OF THE SIGNALS OF PWM CONTROL CIRCUIT IN MATLAB SIMULINK.

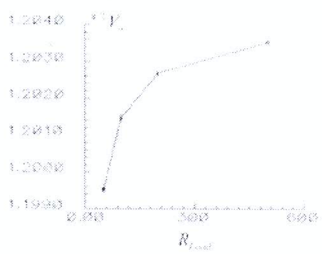

FIGURE 9. OUTPUT VOLTAGE V_O OF THE IC OF BUCK CONVERTER DESIGNED WITH CADENCE AS A FUNCTION OF LOAD.

The output voltage of buck converter model simulated with MATLAB Simulink is shown in Figure 10. As can be seen from the picture the output voltage level is stabilized to 1.2 V.

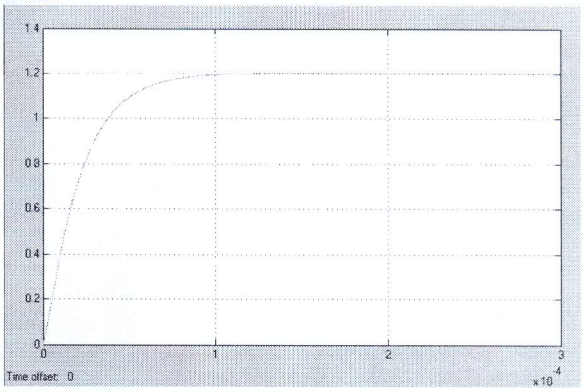

FIGURE 10. OUTPUT VOLTAGE V_O IN MATLAB SIMULINK.

In Figure 11 is shown another model of synchronous buck converter simulated with MATLAB Simulink [3].

The components used in this model are taken from Power System Blockset tool. For S_1 and S_2 are used controllable ideal switches. There R_{ON} resistance can be changed to de desire value.

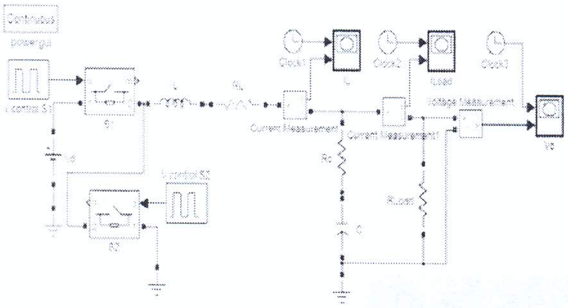

FIGURE 11. SYNCHRONOUS BUCK CONVERTER MODEL SIMULATED WITH MATLAB SIMULINK.

Two switches are regulated synchronously using ideal pulse generators. The control signals respectively for S_1 and S_2 are presented in Figure 12.

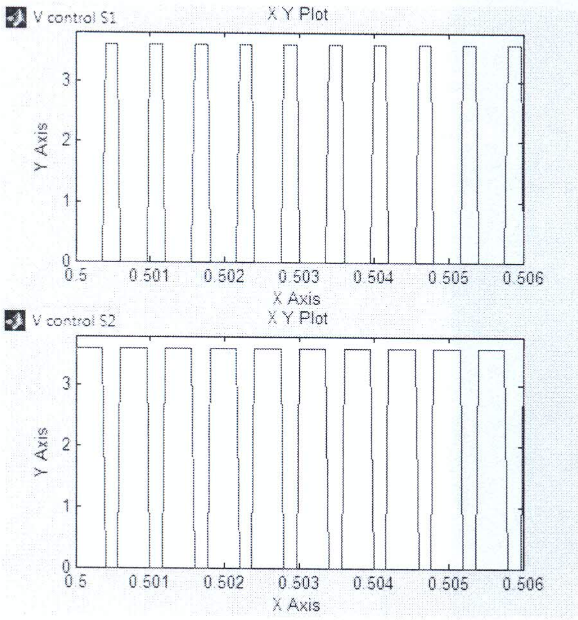

FIGURE 12. THE WAVEFORMS OF THE SIGNALS V CONTROL S1 AND V CONTROL S2.

The input and output voltage of the investigated system are respectively V_d=3.6 V and V_o=1.2 V.

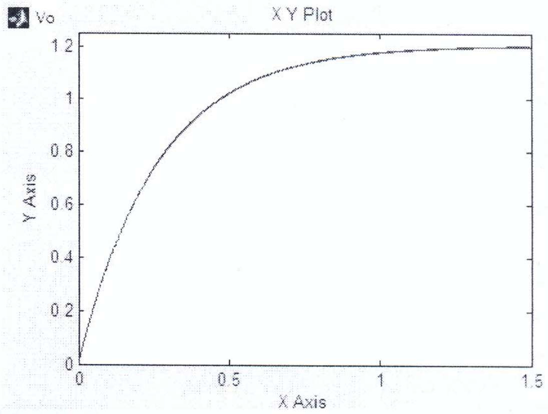

FIGURE 13. OUTPUT VOLTAGE OF BUCK CONVERTER V_O.

The output voltage V_o signal of the modeled buck converter illustrated in Figure 11 is shown in Figure 13.

IV. CONCLUSION

In this paper are presented model investigations of buck converter for low power applications using MATLAB Simulink. State-space averaged modeling of buck converter is considered. High level system investigations could save time to design control circuit of switching mode step-down dc-dc regulator with desirable performance conditions.

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