ANNUAL JOURNAL
OF
ELECTRONICS

Technical University of Sofia
Faculty of Electronic Engineering and Technologies
ANNUAL JOURNAL OF ELECTRONICS

EDITOR'S BOARD

President: Prof. Dr. Racho Ivanov
Vice President: Prof. Dr. Marin Hristov
Members: Prof. Dr. Stefan Ovcharov
          Prof. Dr. Georgy Mihov
          Assoc. Prof. Dr. Petar Yakimov

The Journal is issued by the FACULTY OF ELECTRONIC ENGINEERING
AND TECHNOLOGIES, TECHNICAL UNIVERSITY of SOFIA,
BULGARIA.

The Journal includes the selected papers from the International Scientific
Conference Electronics '12, held on 19 – 21 September 2012 in Sozopol,
Bulgaria.

© 2012 Faculty of Electronic Engineering and Technologies, Technical
University of Sofia, Bulgaria.
CONTENTS

BOOK 2
Vavilov Vl., Modeling Thermal NDT Problems 1
Vainshtein S., G. Duan and J. Kostamovaara, Avalanche Bipolar Transistor: 9
60 Years Old, but Modern Device with New Advances
Duan G., S. Vainshtein and J. Kostamovaara, Effect of Spatial Triggering 15
Inhomogeneity on 3-D Transient in a High-current Avalanche
Transistor
Yordanov R. S., J. I. Ivanov, Automated Design System for Gate Array-based 19
Bipolar Integrated Circuits
Craemer, Development of RF Energy Scavenging System in the Area
of KHBO - Ostend
Gaydazhiev D. G., I. St. Uzunov and G. O. Georgiev, Opportunities for 27
Passband Bandwidth Extension in FBAR Ladder Filters
Gieva E. E., Behavioral Modeling of a Circuit Functionally Analogous to 31
Hydrogen Bonding Network with Water Molecules
Rusev R. P., G. V. Angelov, E. E. Gieva, B. P. Atanasov and M. H. Hristov, 35
Microelectronic Aspects of Hydrogen Bond Characteristics in Active
Site of β-lactamase during the Acyl enzyme Reaction
Spasova M. L., G. V. Angelov and M. H. Hristov, Simulation of 1T DRAM 39
Memory Cell with Verilog-A Model of CNTFET in Cadence
Raykov K. T. and V. H. Videkov, Problems in Wire Bonding Process 43
Videkov V. H. and R. I. Radonov, New Considerations for the Design of IC 46
Bond Pads Using CAD Systems
Bankova A. G. and V. H. Videkov, Measuring the Stability of Nanomaterials 49
Toteva I. Pl. and A. Vl. Andonova, Modeling Snapback Characteristic with 51
SCR-based Device Using PSpice
Andonova A. Vl., Al. P. Radev and K. V. Stankulov, Accelerated Aging for 55
LEDs
Andonova A. Vl., Formation of Thermal Compact Model 59
Delibozov N. G., R. I. Radonov and M. H. Hristov, Evolution of Integrated 63
MEMS Design Methodology
Aleksandrova M. P. and A. Ozturk, Capacitive MEMS Compression Sensor 66
for Touchscreen Display Applications
Bouras M. and A. Hocini, Study of Birefringence in Hybrid Magneto-Optical 70
Thin Film on Ion-Exchanged Glass Waveguide
Vavilov Vl., D. Nesteruk and Vl. Khorev, Ultrasonic and Inductive IR 74
Thermographic Procedures as Newly-Emerged Techniques in Thermal
NDT
Hotra Z. Y. and L. Y. Voznyak, Development of Green OLED Structures 78
Based on Organic Semiconductor Alq3
Spasov G. S., Auger Electron Spectroscopy for Investigation in Microelectronics

Spasov G. S., Auger Electron Spectroscopy for Investigation of Aluminium Nitride Layers

Kolev G. D., Investigation of Piezoelectric Effect in Thin Layers, for Application in Harvesting Devices and MEMS Sensors

Brusev T. S., DC – DC Converter Integrated on CMOS 0.35 μm Technology

Hotra Z. Y., Z. M. Mykytyuk, A.V. Fechan, O. Y. Sushynskyy and O. V. Chaban, Magnetically Controlled Liquid Crystalline Structures for Fiber-Optic Link


Hotra Z. Y., D. Y. Volnyuk and N. V. Kostiv, Investigation of Solar Cell Based on ITO/CuI/SubPc/C60/Al Heterostructure

Pashinski Ch. O., R. D. Kaknakov, L. P. Kolaklieva, T. M. Cholakova and C. P. Bahchedjiev, Even Distribution of the Thickness of Coatings Produced by Vacuum Arc Deposition on Large Parts

Shindov P. C., V. Smatko, T. G. Anastasova and V. St. Serbezov, Nah Modification of CdSSe Layers Properties by Fast CW CO2 Laser Annealing

Denishev K. H., G. B. Kadijski, G. D. Kolev and D. G. Gaydazhiev, Design and Investigation of RF MEMS Switch with Piezoelectric Actuation

Shoikova E. D., and M. Y. Krumova, Innovative Learning Scenario Design

Yordanov R. St., R. Sl. Mitev and G. Dimitrov, Interactive Education in Microelectronics

Goranova M. E. and L. J. Stoyanova, Effective Query Implementation of Scientific Data Based on LINQ to XML


Stoimenov E. Ch. and I. M. Pandiev, An Educational Electronic Prototype System for Phase-Locked Loop - Based Circuits

Mitov K. M. and I. A. Bozhilov, Preparing Students for International Robotics Competitions

Tchoumatchenko V. Pl., T. K. Vaseileva and M. E. Goranova, A Lightweight Learning Content Management System

Todorova V. D. and Sv. S. Kamenov, Program Module for Calculating Constructional Dimensions of Passive Microelectronic Components

Cordemans P., J. Boydens and E. Steegmans, Deterministic State Space Exploration for Concurrent Embedded Software

Catteeuw W., P. Cordemans and J. Boydens, Integration of a CANopen Protocol Stack in an Embedded Application Employing the CANFestival Stack

Vincze R., S. V. Landschoot, E. Steegmans and J. Boydens, Refactoring Sequential Embedded Software for Concurrent Execution Using Design Patterns

II

Naydenov T. B. and P. G. Manoilov, FPGA Implementation of XR Router for Alpha Omega Highway SAN

Kireva T. T., FPGA Implementation of System on a Chip, Using 32-bit RISC Core

Badarov D. H. and G. Sl. Mihov, Universal Digital Counter Based on Xilinx FPGA

Spirov R. P., P. N. Tzanov and N. St. Grancharova, Adaptive FPGA System of Recognition Dynamic Objects

Bogdanov L. V. and R. M. Ivanov, Approaches for Reducing the Power Consumption in Embedded Systems

Brusev T. S. and B. M. Nikolova, Reliability and Power Supply Voltages of Embedded System Platforms

Dilov K. D. and E. N. Dimitrov, Software Integrated Environment for Real-Time System Design and Analysis

Spasov G. V., Open Source Hardware in Education on Embedded Systems for Non-EE Students

Petrov B. B., Application of the Programmable Logic Devices for Implementation of In-circuit Tester for Microprocessor System

Chayleva I. K., M. A. Botev, V. Pl. Dobrev and B. B. Petrov, Methods and Techniques for Real-Time Audio Data Streaming to and from High Capacity Local DSP SDRAM Memory

III
DC – DC Converter Integrated on CMOS 0.35 µm Technology

Tihomir Sashev Brusev

Abstract – DC – DC converter is designed and integrated on CMOS 0.35 µm technology. Investigations results of efficiency and power losses are presented. Different control techniques of monolithic buck converter system are developed.

Keywords – dc – dc converter, CMOS technology, efficiency, power losses

I. INTRODUCTION

In the modern electronic equipments different power supply voltages for the building blocks are needed. DC – DC converters with high efficiency are required to be designed [1]. A way to decreasing the size, weight and consequently the price of these devices is miniaturizations. The integration is the present and future of the electronic technique for many applications. Fully monolithic dc – dc converter could reduce the volume of the devices. The tendency in microelectronics nowadays is to continuously scale down the standard CMOS process technology, which leads to decreased breakdown voltages. In battery-powered electronic devices, however, the battery voltage remain relatively constant and it should be converted to the desired voltage levels with minimum energy loss. The requirement to increase the battery life and the system run-time of these devices becomes stringent. To reduce the power dissipations is necessary subsystems to operate at its optimum supply voltages.

A high switching frequency is the key design parameter, which help to make monolithic integration of active and passive devices. At this high switching frequency, the energy dissipated in power MOS transistors dominates the total losses in dc-dc converter. To receive the best possible efficiency we need to operate exactly at the frequency, where the inductor of low-pass filter has maximum quality factor Q. In CMOS technology, passive components and especially integrated inductor are very lossy. The passive components are for energy storage and output filtering.

The custom designed monolithic voltage converters for individual loads have high efficiency and their volumes are small. The standard PWM control, which is constant frequency method, is widely used to maintain a fixed voltage to output of the converter. When the converter operates with high load, the circuit work in the basic mode and high efficiency could be achieved. In most of the portable electronic devices, a light-load operation or standby mode is a key to achieve longer battery life, and at this mode the system should also indicate high efficiency.

This paper presents dc – dc monolithic buck converter designed on 0.35-µm CMOS technology. Section II is divided into three parts. In Section II A efficiency investigations results as function of different circuit’s parameters are given. Power losses evaluations are presented Section II B. In Section II C developed PWM and PFM controls of the designed buck converter are described.

II. INVESTIGATIONS

A. Efficiency investigations

Figure 1 shows the circuit of a buck converter implemented on standard CMOS 0.35-µm technology. The NMOS and PMOS transistors, which are forming the power stage, are synchronously controlled in a way that when one of the transistors is switched-on the other is switched-off. In the following, the efficiency performance of the power stage is evaluated assuming ideal drivers with the goal to select an appropriate switching frequency and filtering components.

![Figure 1. Synchronous buck converter schematic.](image)

One of the most important parameters in the deconverters is efficiency:

\[ \eta = \frac{P_{\text{OUT}}}{P_{\text{IN}}} \]  

(1)

where \( P_{\text{OUT}} \) is the average output power, \( P_{\text{IN}} \) is the average input power of the converter. The losses in power stage of buck converter are much higher compare to the energy dissipation in the feedback control system [2]. They dominate and determine the efficiency of the system.

The power losses in the filter inductor can seriously decrease the overall efficiency of the converter’s system. Integration of whole dc – dc converter together with passive filter’s inductor and capacitor is possible at high switching frequency \( f_s \). On the other hand this leads to increasing of power losses in CMOS integrated circuits. The disadvantages of monolithic inductors are that they are usually with low inductance, occupied large silicon area and have low quality factor \( Q \).
The influence of the filter's inductor value \( L \) over the efficiency of the synchronous buck converter is investigated. The received results are achieved by simulations using Cadence design tools. In Figure 2 is presented efficiency \( \eta \) of the evaluated circuit as a function \( L \) at different load currents.

![Figure 2](image)

**Figure 2. Efficiency of the designed monolithic buck converter as a function of filter inductor \( L \) at different load currents.**

As can be seen from the picture at small inductor's values \( \eta \) of the investigated circuit is decreasing dramatically. The best efficiency results are achieved at load current equal to 20 mA, because for that current are optimized the sizes of N and P channel power MOS transistors.

The price and volume of electronic equipments is one of the major factors in their design. There are restrictions on the value and the chip area, which can occupy integrated filter capacitor in monolithic buck converter [3]. The effect of the maximum allowable output voltage ripple over efficiency performance of the converter is investigated. The influence of the capacitor value over the system efficiency is evaluated. The output voltage ripple is kept constant at three different levels respectively 10 mV, 20 mV a 50 mV. The investigations are made are average load current equal to \( I_{\text{LOAD}} \), 20 mA.

In Figure 3 are presented received simulations results of the buck converter’s efficiency \( \eta \) as function of filter capacitor \( C \).

![Figure 3](image)

**Figure 3. Efficiency of the designed monolithic buck converter as a function of filter capacitor \( C \) at different maximum allowable output voltage ripple \( \Delta V_{\text{out}} \).**

In Figure 4 is presented relationship between switching frequency \( f_s \) and output filter capacitor \( C \) of the synchronous buck converter, when output voltage ripple is kept constant. As can be seen from the picture, higher \( \Delta V_{\text{out}} \) leads to decreasing of \( f_s \) in order to maintain a constant value of output voltage and inductor current ripple \( I_L \) at fixed value of. At lower switching frequency losses in the power MOS transistors goes down. Thereby reducing the requirements to output voltage ripple \( \Delta V_{\text{out}} \) is increasing the efficiency of monolithic buck converter at fixed filter capacitor \( C \).

![Figure 4](image)

**Figure 4. Switching frequency \( f_s \) of the designed monolithic buck converter as a function of filter capacitor \( C \) at different maximum allowable output voltage ripple \( \Delta V_{\text{out}} \).**

Decreasing the switching frequency \( f_s \) is increased the reliability of the whole integrated buck dc-dc converter system, because the design of PWM control technique became simple.

B. Power losses investigations

At high switching frequencies the losses in the transistors are inadmissibly large and the efficiency of the converter decreases:

\[
\eta = \frac{P_{\text{OUT}}}{P_{\text{IN}}} = \frac{P_{\text{OUT}}}{P_{\text{OUT}} + P_{\text{LOSS}}} \quad (2)
\]

where \( P_{\text{LOSS}} \) are all power losses occurring in the power transistors, as well as in the controlling stages. To obtain high converter efficiency, all conversion losses should be kept to a minimum. The conducting losses in the transistors are proportional to the switching frequency \( f_s \) and the rms-value of the current flowing through the device 0. This relationship is repeated bellow:

\[
P_{\text{LOSS}} = k_1I_{\text{rms}}^2 + k_2f_s \quad (3)
\]

where \( k1 \) and \( k2 \) is are technology dependent coefficient, which are taking into account the size of the power MOS, as well as the resistive and the capacitive losses associated with the MOS structure. Small inductor ripple current will result in smaller rms-value of the current through the MOS structure, and it will respectively lead to better efficiency.
Power losses in filter inductor of designed monolithic dc-de converter are evaluated.

![Graph showing power losses in the filter inductor of buck converter](image)

Figure 5. Power losses in the filter inductor of buck converter of $fs$ and $M_i$, for load (en)$\approx$20 mA.

In Figure 5 are presented received simulations results. Power losses in the filter inductor are investigated as a function of switching frequency $f_s$ and inductor current ripple $M_i$ at $I_{in} = 20$ mA. The received results show that by increasing of switching frequency $f_s$ of the circuit power dissipations in the filter inductor decreased. By increasing of the $M_i$ requirements for the inductor's value decreased for fixed switching frequency $f_s$. This reduces the parasitic impedance of the filter inductor and the related power loss. A higher value of the $M_i$ leads to the increasing of rms current through the inductor which causes to the bigger conduction losses in the inductor.

C. PWM and PFM controls

![PWM block diagram](image)

Figure 6. PWM block diagram

The block diagram of the switching-mode DC-DC buck converter system using standard PWM control loop is shown in Figure 6. The system consists of bandgap reference, error amplifier, ramp generator, comparator, buffer and power buck stage. The power losses in the controlling stages are minimized in order to improve the overall converter efficiency $\eta$. The nominal supply voltage of the converter is 3.6 V and steps-down to 1.2. The system operates at switching frequency $f_s$ of 150 MHz.

The bandgap voltage reference provides a stable voltage for the whole converter system that is independent from the power supply, load current, and temperature variations. This stage consumes only 0.27 mA, which helps to improve $\eta$.

The error amplifier determines the control voltage, which amplifies the difference between the output voltage $V_{out}$ and the reference voltage $V_{ref}$. The ramp generator is a part of the regulation system, which performs the Pulse-Width Modulation (PWM) control. This stage determines the switching frequency $f_s$ of the buck converter. In Figure 7 is shown designed circuit of ramp generator.

![Ramp Generator](image)

Figure 7. Ramp Generator.

This circuit helps to whole designed buck converter system to react when input voltage is changed. When $V_{in}$ jumps the threshold voltages of two comparators, which are included in the ramp generator, are changed. The reason is simple resistive divider consist of $R_1$, $R_2$ and $R_s$. Therefore duty cycle of the control circuit is changed eliminating delay of the output reaction of the buck dc-de converter system.

In Figure 8 are presented reactions of synchronous dc-de buck converter system respectively with ramp generator including resistive divider and with ramp generator without resistive divider, when input voltage $V_{in}$ jumps.

![Reactions of synchronous dc-de buck converter system](image)

Figure 8. Reactions of synchronous dc-de buck converter system respectively with ramp generator including resistive divider and with ramp generator without resistive divider, when input voltage $V_{in}$ jumps.

The control pulses for the power transistors are generated by comparing the sawtooth signal generated by the ramp generator and the control signal from the error amplifier. The comparator generates rectangular pulses whose duty-cycle is a function of the output voltage, and the PWM control loop regulates the output to the desired value.

The buffer stage delivers the controlling pulses for the power transistors. The short-circuit losses are prevented by providing a short gap time during which the NMOS and the PMOS transistors are both switched-off 0. Thus, power losses generated due to this phenomenon are avoided.
In Figure 9 is presented efficiency of the designed buck dc-dc converter as function of average load current $I_{\text{load}}$.

![Figure 9. Efficiency of the designed buck dc-dc converter as function of average load current $I_{\text{load}}$.](image)

As can be seen from the picture efficiency of the buck dc-dc converter system is decreasing dramatically at light-load. PFM control technique is developed to improve the performance of the designed system at these conditions.

In Figure 10 are illustrated output voltages $V_{\text{out}}$ of the converter respectively before and after layout design of the integrated circuit, when PWM control technique is used.

![Figure 10. Output voltage $V_{\text{out}}$ respectively before and after layout design when PWM control technique is used.](image)

The block diagram of the converter utilizing a PFM control technique is shown in Figure 11. Here, a generator with a fixed duty-cycle (50%) is used to drive the power transistors. The voltage regulation is achieved by turning on and off the control loop. When the output voltage exceeds a predefined value, the comparator generates a control signal, which puts the whole system in sleep mode. In sleep mode, the filtering capacitor $C$ delivers power to load, while all active blocks are disabled, except the comparator and the bandgap. When the output voltage goes below certain value, the comparator wakes up the system and the normal operation is restored. This technique allows minimization of the static control block consumption in light-load conditions, thus the overall efficiency is improved.

In Figure 12 are illustrated output voltages $V_{\text{out}}$ of the converter respectively before and after layout design of the integrated circuit, when PFM control technique is used.

![Figure 12. Output voltage $V_{\text{out}}$ respectively before and after layout design when PFM control technique is used.](image)

III. CONCLUSION

In this paper dc–dc buck converter integrated on CMOS 0.35 µm technology is presented. Efficiency of whole system is investigated as a function of different circuit parameters. Power losses in the power stage are evaluated. PWM and PFM control techniques are developed. Resimulation results after layout design of the integrated circuit show good overlapping.

ACKNOWLEDGMENTS

The research described in this paper was carried out within the framework of UNIK Project DUNK – 01/03 – 12.2009.

REFERENCES