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CONTENTS

BOOK 1

Vainshtein, S., V. Yuferev, J. Kostamovaara, V. Palankovski, Collapsing Field Domains in Avalanche Gaas Transistor: Peculiar Phenomenon and Prospective Applications b1 p12
Vitanov, S., V. Palankovski, Electron Mobility Models for III-Nitrides b1 p18
Duan, G., S. N. Vainshtein, J. T. Kostamovaara, Physical Interpretation of "Soft" Surface Breakdown Typical of GaAs Avalanche Transistors b1 p22
Duan, G., S. N. Vainshtein, J. T. Kostamovaara, Self-Organizing of Avalanche Transistor Operating Area in Accordance with Parameters of External Circuit b1 p26
Machan, L., P. Steffan, Accumulation Mode MOS Structure Usage in the Analog Design b1 p30
Videkov, V. H., R. I. Radonov, Die Packaging Methods and Their Relation to the Layout of Integrated Circuits b1 p33
Radonov, R. I., Considerations for the Design of Bond Pads in Integrated Circuits Using CADENCE b1 p36
Brusev, T. S., M. H. Hristov, B. M. Nikolova. Investigations of Power Losses in Off-Chip and On-Chip Inductors b1 p38
Gieva, E. E., R. P. Rusev, G. V. Angelov, M. H. Hristov, T. B. Takov, Microelectronic Differential Amplifier Functionally Analogous to Hydrogen Bonding Network b1 p42
Rusev, R. P., G. V. Angelov, I. D. Panayotov, M. H. Hristov, T. B. Takov, Matlab and Verilog-A Models of Solar Cells b1 p46
Nikolov, D. N., F. T. Koparanov, M. H. Tsanov, E. D. Manolov, M. H. Hristov, Energy Harvesting Transducers: An Overview b1 p50
Nikolov, D. N., E. D. Manolov, M. H. Hristov, M. H. Tsanov, F. T. Koparanov, Architecture of Energy Harvesting Devices b1 p54
Bobeva, S. D., M. H. Hristov, K. H. Denishev, Overview of Automotive MEMS Sensors b1 p 58
Yordanov, R. S., M. H. Hristov, H. L. Yatanski, Interactive Learning Relative to MCM Design b1 p62
Velev, R. Grigorov, S. I. Ivanov, Methods for Measuring of Small Capacitance b1 p65
Karachomakov, A. N., Power–On–Reset Schematic with Low–Voltage Flag Generation Circuitry with Build–in Initial State b1 p69
Arnaudov, R. G., Impact of Via Shielding on Parasitic Coupling and Cavity-Resonance Modes in Multilayer Packages and MCMs b1 p72
Dvořák, P., M. Macalík, M. Kunovjánek, V. Musílek, O. Čech, Liquid Electrolytes for Electrochemical Energy Sources b1 p79
Kunovjánek, M., J. Hýbl, New Types of Membranes for Water Electrolyser b1 p82
Vesely, A., J. Vanek, J. Stencel, J. Dolensky, System for Automatic Recognizing Defects in Solar Cells b1 p84
Prasek, J., J. Chomoucka, J. Policky, New Approach to Polymer Screen-printed Electrodes Enhancement b1 p88
Adamek, M., M. Reznicek, J. Prasek, The Thermal Processes in Milk Production Monitoring by the Simple Thermodynamic Sensor b1 p91
Huran, J., P. H. Shindov, V. Smatko, A. Valovic, A. P. Kobzev, Electrical and Optical Characterization of PECVD Silicon Carbon Nitride Thin Films b1 p94
Stratev, A. B., Component Recognition Algorithms in Automated Assembly b1 p97
Aleksandrova, M. P., M. M. Rassovska, K. A. Gesheva, D. V. Petkov, V. P. Petkov, Preparation of Electron Injecting Layers for Polyfluorenevinylene-Based Electroluminescent Structures b1 p100

Mladenova, D. L., R. H. Kazacov, D. B.a Karashanova, V. . Milenkov, T. S. Dobreva, D. S. Budurova, V. A. Sinigersky, I. T. Zhivkov, Optimization of Thin Polyvinylcarbazole Spin Coated Films Applicable in Organic Based Devices b1 p104
Denishev, K. H., I. F. Ivanov, MEMS Generators for Microdroplets b1 p108
Kolev, G. D., K. H. Denishev, S. D. Bobeva, Design and Analyzing of Silicon Diaphragm for MEMS Pressure Sensors b1 p112
Boyadzhiev, S. I., M. M. Minkova - Rassovska, Preparation and Characterization of Reactive Sputtered ITO Thin Films b1 p116
Vervenne, I., J. Catrysse, G. Deconinck, Comparison of Reliability Prediction Analysis and HALT of an Electronic System b1 p120
Milanov, P. M., N. G. Kenarov, FPGA Platform for Support Digital and Mixed-signal Design Development b1 p124
Farkov, G. A., M. Camminadi, Approaches for Automated PCB Measurements b1 p127
Videkov, V. H., G. A. Farkov, B. R. Tzaneva, I. A. Vrublevski, Investigation of Nanostructured Objects Using Cross-section Techniques b1 p130
Andonova, A. V, S. V. Todorov, Buried Objects Detection by Thermography b1 p133
Andonova, A. V., A. P. Radev, Degradation Analysis for Light Emitting Diodes b1 p137
Peuteman, J., J. Baert, R. De Craemer, P. Knapo, Implementing DSP Course Modules with Multimedia Oriented Projects b1 p141
Shoikova, E. D., M. J. Krumova, O*NET and Competency Based Education b1 p145
Shoikova, E. D., M. J. Krumova, Overview of the Occupational Information Network b1 p152
Ivanova, M. S., J. Alam, Wave for Personal Learning Network Forming and for Collaborative Knowledge Transfer b1 p157
Vasileva, T. K., V. P. Tchoumatchenko, Knowledge Practices Laboratory b1 p161
Kostadinov, A. N., Using Logisim and MiSim DE Software Tools in the Digital Logic and Microprocessor Design Subject b1 p165
Spasova, N. V., Implementing an Electronic System for Assessment in Engineering Education b1 p169
Peuteman, J., P. Devlies, J. Knockaert, G. Vandecasteele, T. Verbeerst, I. Vervenne, Laboratory Setup for Teaching Reflection Phenomena between a PWM Inverter and an Induction Motor b1 p172
Yankov, P. V, V. C. Valchev, Power/Frequency Characteristics of Passive Controlled Wind Turbines with Additional Reactive Components in the Circuitry b1 p176
Valchev, V. C., P. V. Yankov, Improvement on Passive Controlled Wind Turbines Schematics and Obtaining Power/Frequency Curves b1 p180
Gigov, G. H., G. T. Kanov, E. I. Popov, Steady – State and Transient Processes in a Current–Fed Inverter Supplied from a Buck DC – DC converter b1 p184
Hinov, N. L., D. D. Arnaudov, N. P. Gradinarov, G. V. Kraev, Comparative Analysis of Circuits with Limitation of the Voltage over Commutating Inductance in Force-Commutating Mode of the Devices b1 p188
Hinov, N. L., D. D. Arnaudov, G. V. Kraev, S. V. Georgiev, Study of Photovoltaic Systems for Supplying DC Loads b1 p192
Vuchev, A. S., N. D. Bankov, G. P. Terziyski, Analysis of LCC Resonant DC-DC Converter with Capacitive Output Filter b1 p196
Vuchev, A. S., N. D. Bankov, G. P. Terziyski, Load Characteristics of LCC Resonant DC-DC Converter with Capacitive Output Filter b1 p200
Mareva, D. J., D. D. Yudov, E. M. Marev, Inverter for Induction Heating of Fluids b1 p204
Popov, E. I., L. I. Pindeva, S. T. Tsolov, Three – Dimensional Generalized Characteristics of Autonomous Serial R L C Inverters without Free – Wheeling Diodes b1 p208

Investigations of Power Losses in Off-Chip and On-Chip Inductors

Tihomir Sashev Brusev, Marin Hristov Hristov and Boyanka Marinova Nikolova

Abstract – **This paper includes investigations of power losses in off-chip and on-chip filter inductors in monolithic dc-dc converter designed on CMOS 0.35 µm technology. Chip coils of the company Murata are used for off-chip inductors. For the extraction of the model's parameters of integrated inductors of CMOS 0.35 µm process is used one of the Cadence tools named "Virtuoso Passive Component Designer". Comparison between power losses in off-chip and on-chip inductors is made.**

Keywords – **power losses, off-chip and on-chip inductors, dc-dc converters.**

I. Introduction

The fully monolithic dc-dc converters can reduce the cost and size of the battery powered portable electronic devices. One of the most important parameters in the dc- converters is efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} \qquad (1)$$

where P_{OUT} is the average output power, P_{IN} is the average input power of the converter. The losses in power stage of buck converter are much higher compare to the energy dissipation in the feedback control system [1]. They dominate and determine the efficiency of the system. The power losses in the filter inductor can seriously decrease the overall efficiency of the converter's system. It's very important to be investigated and compared power dissipations when off-chip and on-chip filter components are used. Integrated inductors occupied huge silicon area. Therefore is necessary to be estimated which type of inductors is more suitable for the designed dc-dc converter.

This paper presents the investigations results of power losses in filter inductor of monolithic dc-dc converter designed on CMOS 0.35 µm technology in buck converter implemented on standard CMOS 0.35-µm technology. In Section II are presented the received simulations results with Cadence. This section is divided on two parts. In Section II *A* are shown the received results for power dissipations in the off-chip filter inductor. For the investigations are used chip coils of the company Murata. In Section II *B* are presented power losses when on-chip filter inductors of CMOS 0.35 µm process are used. Influence of the low Q-factor of integrated filter inductor over the dc-dc converter efficiency is evaluated.

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II. Power Losses in Off-Chip and On-Chip Inductors

In Fig. 1 is shown the circuit of a buck converter implemented on standard CMOS 0.35-µm technology. For the power losses investigation of off-chip and on-chip filter inductors an input voltage of 3.6V is chosen for the converter, since this is the normal voltage for Lithium-Ion battery cell that is typically used in battery-powered devices. The output voltage V_{out} is regulated to 1.2V, which on the other hand is determined by the standard supply voltages of advanced CMOS processes.

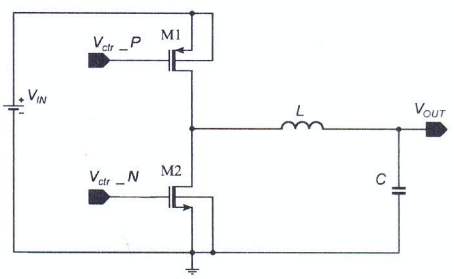

FIG. 1. SYNCHRONEOUS BUCK CONVERTER SCHEMATIC.

Part of the total power losses in the monolithic switching mode buck dc-dc converter are due to the series resistance and parasitic capacitance of the filter inductor. Integrated inductors have high series resistance, which grow up with increasing of the inductor's value. This lead to the low quality factor Q of these components [2]. Integration of a spiral inductor with sufficient inductance is not feasible, because they occupy huge silicon area and have low Q factor. The total power dissipated in filter inductor, assuming that the inductor parasitic impedance scale linearly with the inductance is equal to [3]:

$$P_{ind} = b\left[\frac{I^2}{\Delta i_L f_s} + \frac{\Delta i_L}{3 f_s} + \frac{C_{L0} V_{DD1}^2}{R_{L0} \Delta i_L}\right] \qquad (3)$$

where b is a coefficient depending from the parasitic capacitance and parasitic series resistance of the filter inductor, C_{L0} and R_{L0} are respectively the parasitic stray

capacitance and parasitic series resistance per 1 nH inductance, V_{DD1} is power supply.

The influence of switching frequency f_s and inductor current ripple Δi_L over the power losses in the filter inductor is investigated. Integrated passive inductors occupied huge silicon area, which make more expensive the electronic devices. It's necessary to be estimated energy dissipation in off-chip and on-chip filter inductors.

Power losses in the filter inductor of the synchroneous buck converter designed on CMOS 0.35-µm technology are analyzed with Cadence, as a function of switching frequency f_s and inductor current ripple Δi_L. Evaluated and compared are power losses in off-chip and on-chip filter inductor of monolithic buck dc-dc converter.

A. Power losses in the off-chip filter inductor

In this section is evaluated power losses in off-chip filter inductors of monolithic dc-dc converter designed on CMOS 0.35-µm technology. The investigated inductors are chip coils for high frequency horizontal wire wound of the company Murata. They have broad range of inductance and high self-resonant frequency. This realizes high Q-factor and stable inductance at high frequency. Their low dc resistance is ideal for low power losses. These off-chip inductors are often used in telecommunication applications.

The received results of power losses in the off-chip filter inductor of buck dc-dc converter are presented below. For the simulations with Cadence on CMOS 0.35-µm technology are used inductor's models of the company Murata [4].

In Table 1 are presented power losses in the off-chip filter inductor P_{ind} as a function of switching frequency f_s and inductor current ripple Δi_L. Average output current of the buck converter $I_{out\ (av)}$ equal to 20 mA and Δi_L=0.5x$I_{out\ (av)}$.

TABLE 1. POWER LOSSES IN THE OFF-CHIP INDUCTORS OF BUCK CONVERTER; $\Delta I_L/0.5xI_{OUT\ (AV)}$;

	L=10 nH	L=50 nH	L=100 nH	L=200 nH
$I_{out\ (av)}$ [mA]	20	20	20	20
f_s [MHz]	5000	2000	1500	1000
$\Delta i_L/0.5xI_{out\ (av)}$	0.5	0.5	0.5	0.5
P_{ind} [mW]	0.0579	0.148	0.316	1.02

In Table 2 are presented power losses in the off-chip filter inductor P_{ind} as a function of switching frequency f_s and inductor current ripple Δi_L. Average output current of the buck converter $I_{out\ (av)}$ equal to 20 mA and Δi_L=$I_{out\ (av)}$.

In Table 3 are presented power losses in the off-chip filter inductor P_{ind} as a function of switching frequency f_s and inductor current ripple Δi_L. Average output current of the buck converter $I_{out\ (av)}$ equal to 20 mA and Δi_L=2x$I_{out\ (av)}$. Received simulations results for power losses in the off-chip filter inductor P_{ind} of buck converter implemented on CMOS 0.35-µm technology as a function of f_s and Δi_L, for $I_{out\ (av)}$=20 mA given in Table 1, Table 2 and Table 3, are graphically presented in Fig. 2. For simulations the inductor's models of the company Murata are used.

TABLE 2. POWER LOSSES IN THE OFF-CHIP INDUCTORS OF BUCK CONVERTER; $\Delta I_L/I_{OUT\ (AV)}$

	L=10 nH	L=50 nH	L=100 nH	L=200 nH
$I_{out\ (av)}$ [mA]	20	20	20	20
f_s [MHz]	2500	1000	750	500
$\Delta i_L/I_{out\ (av)}$	1	1	1	1
P_{ind} [mW]	0.056	0.183	0.333	1.02

TABLE 3. POWER LOSSES IN THE OFF-CHIP INDUCTORS OF BUCK CONVERTER; $\Delta I_L/2xI_{OUT\ (AV)}$

	L=10 nH	L=50 nH	L=100 nH	L=200 nH
$I_{out\ (av)}$ [mA]	20	20	20	20
f_s [MHz]	1250	500	350	250
$\Delta i_L/2xI_{out\ (av)}$	2	2	2	2
P_{ind} [mW]	0.062	0.139	0.291	0.97

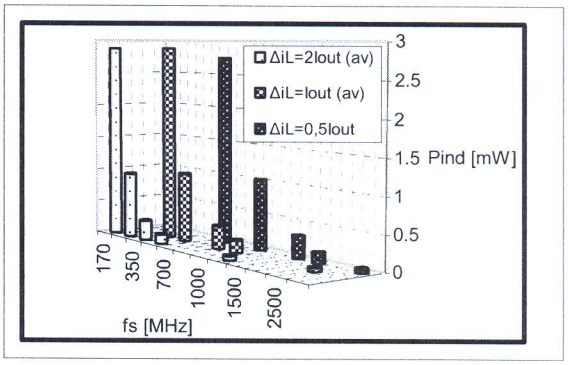

FIG. 2. POWER LOSSES IN THE OFF-CHIP FILTER INDUCTOR OF BUCK CONVERTER IMPLEMENTED ON CMOS 0.35-µm TECHNOLOGY AS A FUNCTION OF f_s AND Δi_L, FOR $I_{OUT\ (AV)}$=20 mA.

Power losses in the off-chip filter inductor of buck dc-dc converter decreased with increasing of switching frequency f_s and inductor current ripple Δi_L.

B. Power losses in the on-chip filter inductor

The dependence of the power dissipation in on-chip filter inductors of CMOS 0.35-µm technology are investigated and evaluated. Standard monolithic inductors are not optimized for the specific applications. In the other hand theirs number of values are limited. That's way is necessary to be designed integrated

inductors with desired value and geometry. One of the Cadence tools named "Virtuoso Passive Component Designer" is used for the extraction of inductor's model parameters [5].

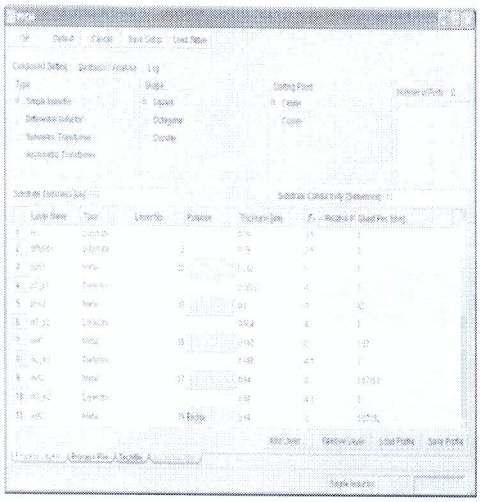

FIG. 3. WINDOW FROM CADENCE TOOL "VIRTUOSO PASSIVE COMPONENT DESIGNER".

The model of on-chip inductors used in the investigations is shown in Fig. 4. The parameters presented in Fig. 4 are: L_s – series inductance; R_s – series resistance; C_p – parallel capacitance; $C_{OX1/2}$ – oxide capacitance; $C_{s1/2}$ – substrate capacitance; $R_{s1/2}$ – substrate resistance.

The values of the extracted parameters are used for simulations. The received results of power losses in the on-chip filter inductor of buck dc-dc converter are presented below. Investigations are made for average output current of the buck converter $I_{out\ (av)}$ equal to 20 mA.

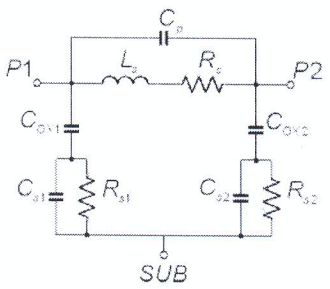

FIG. 4. THE MODEL OF ON-CHIP INDUCTORS.

In Table 4 are presented power losses in the on-chip filter inductor P_{ind} as a function of switchnig frequency f_s and inductor current ripple Δi_L, for Δi_L=0.5x$I_{out\ (av)}$.

In Table 5 are presented power losses in the on-chip filter inductor P_{ind} as a function of switching frequency f_s and inductor current ripple Δi_L. Average output current of the buck converter $I_{out\ (av)}$ equal to 20 mA and $\Delta i_L = I_{out\ (av)}$.

In Table 6 are presented power losses in the on-chip filter inductor P_{ind} as a function of switching frequency f_s and inductor current ripple Δi_L. Average output current of the buck converter $I_{out\ (av)}$ equal to 20 mA and $\Delta i_L = 2xI_{out\ (av)}$.

Received simulations results for power losses in the on-chip filter inductor P_{ind} of buck converter implemented on CMOS 0.35-µm technology as a function of f_s and Δi_L, for $I_{out\ (av)}$=20 mA given in Table 4, Table 5 and Table 6, are graphically presented in Fig. 5.

TABLE 4. POWER LOSSES IN THE ON-CHIP INDUCTORS OF BUCK CONVERTER; $\Delta i_L/0.5xI_{out\ (av)}$

	L=10 nH	L=14.1 nH	L=28.2 nH	L=51 nH
$I_{out\ (av)}$ [mA]	20	20	20	20
f_s [MHz]	5000	4000	3000	2000
$\Delta i_L/0.5xI_{out\ (av)}$	0.5	0.5	0.5	0.5
P_{ind} [mW]	15.37	15.9	16.35	23.59

TABLE 5. POWER LOSSES IN THE ON-CHIP INDUCTORS OF BUCK CONVERTER; $\Delta i_L/I_{out\ (av)}$

	L=10 nH	L=14.1 nH	L=28.2 nH	L=51 nH
$I_{out\ (av)}$ [mA]	20	20	20	20
f_s [MHz]	2500	2000	1500	1000
$\Delta i_L/I_{out\ (av)}$	1	1	1	1
P_{ind} [mW]	15.37	15.74	16.37	23.6

TABLE 6. POWER LOSSES IN THE ON-CHIP INDUCTORS OF BUCK CONVERTER; $\Delta i_L/2xI_{out\ (av)}$

	L=10 nH	L=14.1 nH	L=28.2 nH	L=51 nH
$I_{out\ (av)}$ [mA]	20	20	20	20
f_s [MHz]	1250	1000	750	500
$\Delta i_L/2xI_{out\ (av)}$	2	2	2	2
P_{ind} [mW]	15.37	15.5	16.3	23.59

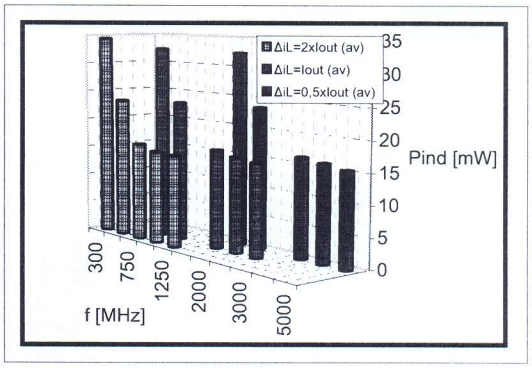

FIG. 5. POWER LOSSES IN THE ON-CHIP FILTER INDUCTOR OF BUCK CONVERTER IMPLEMENTED ON CMOS 0.35-µm TECHNOLOGY AS A FUNCTION OF FS AND Δi_L, FOR $I_{out\ (av)}$=20 mA.

As can be seen from Fig. 2 and Fig. 5 power losses in the filter inductor of buck dc-dc converter goes down with increasing of switching frequency f_s and inductor current ripple Δi_L. When off-chip filter inductors of the company Murata are used, power dissipation is around 10 times lower compare to the losses in integrated inductors of CMOS 0.35-μm process (Fig. 2, Fig. 5). The reason is the high series resistance and low Q-factor of the on-chip inductors.

The efficiency of the designed monolithic dc-dc converter as a function of on-chip filter inductors is evaluated. Investigations are made at different average outputs currents ($I_{out\ (av)}$) of the circuit. In Table 7 are shown received results at $I_{out\ (av)}$=5 mA. In Table 8 are shown received results at $I_{out\ (av)}$=20 mA. The simulation results shown in Table 7 and Table 8 are graphically presented in Fig. 6.

TABLE 7. EFFICIENCY OF THE DC-DC CONVERTER

	L=1.4 nH	L=2.6 nH	L=4.7 nH	L=9 nH
$I_{out\ (av)}$ [mA]	5	5	5	5
η [%]	8.7	13.9	15.4	15.5

TABLE 8. EFFICIENCY OF THE DC-DC CONVERTER

	L=1.4 nH	L=2.6 nH	L=4.7 nH	L=9 nH
$I_{out\ (av)}$ [mA]	20	20	20	20
η [%]	24.7	34.4	36.3	33.5

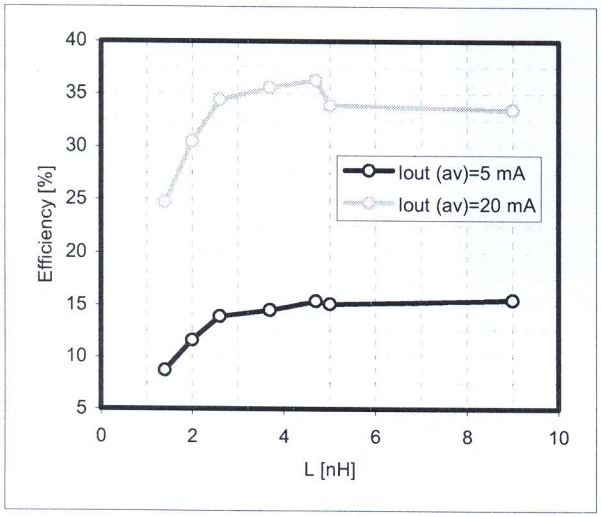

FIG. 6. EFFICIENCY OF THE MONOLITHIC DC-DC CONVERTER DESIGNED ON CMOS 0.35-μM TECHNOLOGY AS A FUNCTION OF DIFFERENT ON-CHIP INDUCTORS.

The maximum value of the converter's efficiency when on-chip filter inductors are used is 36 %. One of the reasons is low Q-factor of the available integrated inductors.

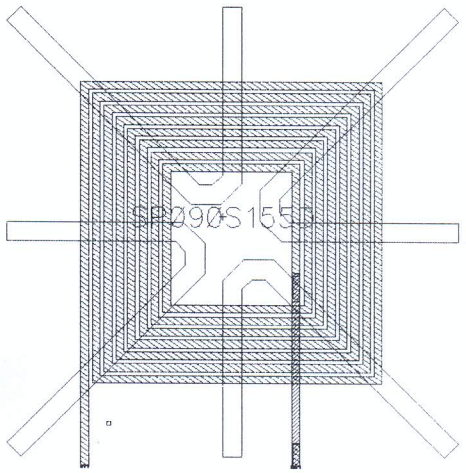

FIG. 7. THE LAYOUT OF ON-CHIP INDUCTORS.

III. CONCLUSION

The power losses in the off-chip and on-chip filter inductors of monolithic buck dc-dc converter designed on CMOS 0.35 μm technology has been investigated. When off-chip filter inductors of the company Murata are used, power dissipation is around 10 times lower compare to the losses in integrated inductors of CMOS 0.35-μm process (Fig. 2, Fig. 5). The received results show that by increasing of switching frequency f_s of the circuit power dissipations in the filter inductor decreased. By increasing of the Δi_L requirements for the inductor's value decreased for fixed switching frequency f_s. This reduces the parasitic impedance of the filter inductor and the related power loss. A higher value of the Δi_L leads to the increasing of rms current through the inductor which causes to the bigger conduction losses in the inductor.

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