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Investigations of Power Losses in Off-Chip and On-Chip Inductors

Tihomir Sashev Brusev, Marin Hristov Hristov and Boyanka Marinova Nikolova

Abstract – This paper includes investigations of power losses in off-chip and on-chip filter inductors in monolithic dc-dc converter designed on CMOS 0.35 μm technology. Chip coils of the company Murata are used for off-chip inductors. For the extraction of the model’s parameters of integrated inductors of CMOS 0.35 μm process is used one of the Cadence tools named “Virtuoso Passive Component Designer”. Comparison between power losses in off-chip and on-chip inductors is made.

Keywords: power losses, off-chip and on-chip inductors, dc-dc converters.

I. INTRODUCTION

The fully monolithic dc-dc converters can reduce the cost and size of the battery powered portable electronic devices. One of the most important parameters in the dc-converter is efficiency:

\[ \eta = \frac{P_{OUT}}{P_IN} \]  

(1)

where \( P_{OUT} \) is the average output power, \( P_IN \) is the average input power of the converter. The losses in power stage of buck converter are much higher compared to the energy dissipation in the feedback control system [1]. They dominate and determine the efficiency of the system. The power losses in the filter inductor can seriously decrease the overall efficiency of the converter’s system. It’s very important to be investigated and compared power dissipations when off-chip and on-chip filter components are used. Integrated inductors occupied huge silicon area. Therefore is necessary to be estimated which type of inductors is more suitable for the designed dc-dc converter.

This paper presents the investigations results of power losses in filter inductor of monolithic dc-dc converter designed on CMOS 0.35 μm technology in buck converter implemented on standard CMOS 0.35-μm technology. In Section II are presented the received simulations results with Cadence. This section is divided on two parts. In Section II A are shown the received results for power dissipations in the off-chip filter inductor. For the investigations are used chip coils of the company Murata. In Section II B are presented power losses when on-chip filter inductors of CMOS 0.35 μm process are used. Influence of the low \( Q \)-factor of integrated filter inductor over the dc-dc converter efficiency is evaluated.

II. POWER LOSSES IN OFF-CHIP AND ON-CHIP INDUCTORS

In Fig. 1 is shown the circuit of a buck converter implemented on standard CMOS 0.35-μm technology. For the power losses investigation of off-chip and on-chip filter inductors an input voltage of 3.6V is chosen for the converter, since this is the normal voltage for Lithium-Ion battery cell that is typically used in battery-powered devices. The output voltage \( V_{OUT} \) is regulated to 1.2V, which on the other hand is determined by the standard supply voltages of advanced CMOS processes.

\[ P_{out} = \frac{1}{3f_c} \left( \Delta I + \frac{\Delta I}{R_{L,0}} + \frac{C_{L,0} \Delta V_{IN}}{R_{L,0} \Delta f} \right) \]  

(3)

where \( b \) is a coefficient depending from the parasitic capacitance and parasitic series resistance of the filter inductor, \( C_{L,0} \) and \( R_{L,0} \) are respectively the parasitic stray
capacitance and parasitic series resistance per 1 nH inductance, \( V_{IN} \) is power supply.

The influence of switching frequency \( f_s \) and inductor current ripple \( \Delta I_L \) over the power losses in the filter inductor is investigated. Integrated passive inductors occupied huge silicon area, which make more expensive the electronic devices. It's necessary to be estimated energy dissipation in off-chip and on-chip filter inductors.

Power losses in the filter inductor of the synchronous buck converter designed on CMOS 0.35-\( \mu \)m technology are analyzed with Cadence, as a function of switching frequency \( f_s \) and inductor current ripple \( \Delta I_L \). Evaluated and compared are power losses in off-chip and on-chip filter inductor of monolithic buck dc-dc converter.

### A. Power losses in the off-chip filter inductor

In this section is evaluated power losses in off-chip filter inductors of monolithic dc-dc converter designed on CMOS 0.35-\( \mu \)m technology. The investigated inductors are chip coils for high frequency horizontal wire wound of the company Murata. They have broad range of inductance and high self-resonant frequency. This realizes high Q-factor and stable inductance at high frequency. Their low dc resistance is ideal for low power losses. These off-chip inductors are often used in telecommunication applications.

The received results of power losses in the off-chip filter inductor of buck dc-dc converter are presented below. For the simulations with Cadence on CMOS 0.35-\( \mu \)m technology are used inductor’s models of the company Murata [4].

In Table 1 are presented power losses in the off-chip filter inductor \( P_{out} \) as a function of switching frequency \( f_s \) and inductor current ripple \( \Delta I_L \). Average output current of the buck converter \( I_{out(ava)} \) equal to 20 mA and \( \Delta I_L = 0.5 x I_{out(ava)} \).

### TABLE 1. POWER LOSSES IN THE OFF-CHIP INDUCTORS OF BUCK CONVERTER; \( \Delta I/I_{out(ava)} \)

<table>
<thead>
<tr>
<th>( L = 10 ) nH</th>
<th>( L = 50 ) nH</th>
<th>( L = 100 ) nH</th>
<th>( L = 200 ) nH</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{out(ava)} ) [mA]</td>
<td>20</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>( f_s ) [MHz]</td>
<td>5000</td>
<td>2000</td>
<td>1500</td>
</tr>
<tr>
<td>( \Delta I/I_{out(ava)} )</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>( P_{out} ) [mW]</td>
<td>0.0579</td>
<td>0.148</td>
<td>0.316</td>
</tr>
</tbody>
</table>

In Table 2 are presented power losses in the off-chip filter inductor \( P_{out} \) as a function of switching frequency \( f_s \), and inductor current ripple \( \Delta I_L \). Average output current of the buck converter \( I_{out(ava)} \) equal to 20 mA and \( \Delta I_L = 0.5 x I_{out(ava)} \).

### TABLE 2. POWER LOSSES IN THE OFF-CHIP INDUCTORS OF BUCK CONVERTER; \( \Delta I/I_{out(ava)} \)

<table>
<thead>
<tr>
<th>( L = 10 ) nH</th>
<th>( L = 50 ) nH</th>
<th>( L = 100 ) nH</th>
<th>( L = 200 ) nH</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{out(ava)} ) [mA]</td>
<td>20</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>( f_s ) [MHz]</td>
<td>1250</td>
<td>500</td>
<td>350</td>
</tr>
<tr>
<td>( \Delta I/I_{out(ava)} )</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>( P_{out} ) [mW]</td>
<td>0.062</td>
<td>0.139</td>
<td>0.291</td>
</tr>
</tbody>
</table>

In Fig. 2 is presented power losses in the off-chip filter inductor of buck dc-dc converter with increasing of switching frequency \( f_s \), and inductor current ripple \( \Delta I_L \).

### B. Power losses in the on-chip filter inductor

The dependence of the power dissipation in on-chip filter inductors of CMOS 0.35-\( \mu \)m technology is investigated and evaluated. Standard monolithic inductors are not optimized for the specific applications. In the other hand their number of values are limited. That's why is necessary to be designed integrated...
inductors with desired value and geometry. One of the Cadence tools named "Virtuoso Passive Component Designer" is used for the extraction of inductor’s model parameters [5].

The model of on-chip inductors used in the investigations is shown in Fig. 4. The parameters presented in Fig. 4 are: $L_s$ – series inductance; $R_s$ – series resistance; $C_p$ – parallel capacitance; $C_{GOX/2}$ – oxide capacitance; $C_{St/2}$ – substrate capacitance; $R_{St/2}$ – substrate resistance.

The values of the extracted parameters are used for simulations. The received results of power losses in the on-chip filter inductor of buck dc-dc converter are presented below. Investigations are made for average output current of the buck converter $I_{out (av)}$ equal to 20 mA.

In Table 4 are presented power losses in the on-chip filter inductor $P_{on}$ as a function of switching frequency $f_s$ and inductor current ripple $\Delta I_L$, for $\Delta I_L = 0.5 I_{out (av)}$.

In Table 5 are presented power losses in the on-chip filter inductor $P_{on}$ as a function of switching frequency $f_s$ and inductor current ripple $\Delta I_L$. Average output current of the buck converter $I_{out (av)}$ equal to 20 mA and $\Delta I_L = 2 I_{out (av)}$.

Received simulations results for power losses in the on-chip filter inductor $P_{on}$ of buck converter implemented on CMOS 0.35-µm technology as a function of $f_s$ and $\Delta I_L$ for $I_{out (av)} = 20$ mA given in Table 4, Table 5 and Table 6, are graphically presented in Fig. 5.

<table>
<thead>
<tr>
<th>$L$ (nH)</th>
<th>$I_{out (av)}$ (mA)</th>
<th>$f_s$ (MHz)</th>
<th>$\Delta I_L / I_{out (av)}$</th>
<th>$P_{on}$ (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>20</td>
<td>5000</td>
<td>0.5</td>
<td>15.37</td>
</tr>
<tr>
<td>14.1</td>
<td>20</td>
<td>4000</td>
<td>0.5</td>
<td>15.19</td>
</tr>
<tr>
<td>28.2</td>
<td>20</td>
<td>3000</td>
<td>0.5</td>
<td>16.35</td>
</tr>
<tr>
<td>51</td>
<td>20</td>
<td>2000</td>
<td>0.5</td>
<td>23.59</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$L$ (nH)</th>
<th>$I_{out (av)}$ (mA)</th>
<th>$f_s$ (MHz)</th>
<th>$\Delta I_L / I_{out (av)}$</th>
<th>$P_{on}$ (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>20</td>
<td>2500</td>
<td>1</td>
<td>15.37</td>
</tr>
<tr>
<td>14.1</td>
<td>20</td>
<td>2000</td>
<td>1</td>
<td>15.74</td>
</tr>
<tr>
<td>28.2</td>
<td>20</td>
<td>1500</td>
<td>1</td>
<td>16.37</td>
</tr>
<tr>
<td>51</td>
<td>20</td>
<td>1000</td>
<td>1</td>
<td>23.6</td>
</tr>
</tbody>
</table>

TABLE 6. POWER LOSSES IN THE ON-CHIP INDUCTORS OF BUCK CONVERTER; $\Delta I_L / I_{out (av)}$

<table>
<thead>
<tr>
<th>$L$ (nH)</th>
<th>$I_{out (av)}$ (mA)</th>
<th>$f_s$ (MHz)</th>
<th>$\Delta I_L / I_{out (av)}$</th>
<th>$P_{on}$ (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>20</td>
<td>1250</td>
<td>2</td>
<td>15.37</td>
</tr>
<tr>
<td>14.1</td>
<td>20</td>
<td>1000</td>
<td>2</td>
<td>15.5</td>
</tr>
<tr>
<td>28.2</td>
<td>20</td>
<td>750</td>
<td>2</td>
<td>16.3</td>
</tr>
<tr>
<td>51</td>
<td>20</td>
<td>500</td>
<td>2</td>
<td>23.59</td>
</tr>
</tbody>
</table>
As can be seen from Fig. 2 and Fig. 5 power losses in the filter inductor of buck dc-de converter goes down with increasing of switching frequency $f_s$ and inductor current ripple $\Delta I_l$. When off-chip filter inductors of the company Murata are used, power dissipation is around 10 times lower compare to the losses in integrated inductors of CMOS 0.35-μm process (Fig. 2, Fig. 5). The reason is the high series resistance and low Q-factor of the on-chip inductors.

The efficiency of the designed monolithic dc-de converter as a function of on-chip filter inductors is evaluated. Investigations are made at different average outputs currents ($I_{out}\ (av)$) of the circuit. In Table 7 are shown received results at $I_{out}\ (av)=5$ mA. In Table 8 are shown received results at $I_{out}\ (av)=20$ mA. The simulation results shown in Table 7 and Table 8 are graphically presented in Fig. 6.

**TABLE 7. EFFICIENCY OF THE DC-DC CONVERTER**

<table>
<thead>
<tr>
<th>$I_{out\ (av)}$ [mA]</th>
<th>$L=1.4$ nH</th>
<th>$L=2.6$ nH</th>
<th>$L=4.7$ nH</th>
<th>$L=9$ nH</th>
</tr>
</thead>
<tbody>
<tr>
<td>η [%]</td>
<td>8.7</td>
<td>13.9</td>
<td>15.4</td>
<td>15.5</td>
</tr>
</tbody>
</table>

**TABLE 8. EFFICIENCY OF THE DC-DC CONVERTER**

<table>
<thead>
<tr>
<th>$I_{out\ (av)}$ [mA]</th>
<th>$L=1.4$ nH</th>
<th>$L=2.6$ nH</th>
<th>$L=4.7$ nH</th>
<th>$L=9$ nH</th>
</tr>
</thead>
<tbody>
<tr>
<td>η [%]</td>
<td>24.7</td>
<td>34.4</td>
<td>36.3</td>
<td>33.5</td>
</tr>
</tbody>
</table>

**FIG. 6. EFFICIENCY OF THE MONOLITHIC DC-DC CONVERTER DESIGNED ON CMOS 0.35-μM TECHNOLOGY AS A FUNCTION OF DIFFERENT ON-CHIP INDUCTORS.**

The maximum value of the converter’s efficiency when on-chip filter inductors are used is 36 %. One of the reasons is low Q-factor of the available integrated inductors.

**III. CONCLUSION**

The power losses in the off-chip and on-chip filter inductors of monolithic buck dc-de converter designed on CMOS 0.35 μm technology has been investigated. When off-chip filter inductors of the company Murata are used, power dissipation is around 10 times lower compare to the losses in integrated inductors of CMOS 0.35-μm process (Fig. 2, Fig. 5). The received results show that by increasing of switching frequency $f_s$ of the circuit power dissipations in the filter inductor decreased. By increasing of the $\Delta I_l$ requirements for the inductor’s value decreased for fixed switching frequency $f_s$. This reduces the parasitic impedance of the filter inductor and the related power loss. A higher value of the $\Delta I_l$ leads to the increasing of rms current through the inductor which causes to the bigger conduction losses in the inductor.

**ACKNOWLEDGEMENT**

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