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TABLE OF CONTENTS

PLENARY SESSION

Initial Steps in Development of Computer Science in Macedonia and Pioneering Contribution to Human-Robot Interface using Signals Generated by a Human Head	3
Stevo Bozinovski	

RADIO COMMUNICATIONS, MICROWAVES, ANTENNAS

Coupled Halfwave Microstrip Resonators with Dumbbell Type Defected Ground Structure	13
Marin Nedelchev, Alexander Kolev	
Effect of RF Receiver Nonlinearity on Mobile Telecommunication Systems.....	17
Youssef Abd Alrahman and Ilia Iliev	
Omnidirectional Double Biquad Omni-Antenna for 2.4 GHz Wireless Link Application.....	21
Kalina Kalinovska and Peter Z. Petkov	
Synthesis of Wideband Edge Coupled Microstrip Filters with Defected Ground Structures.....	25
Marin Nedelchev, Alexander Kolev, Ilia Iliev	
Modified Fractal Super J-pole Antenna	29
Boncho Bonev, Peter Petkov and Nina Spassova	
Experimental Determination of 2biQUAD Antenna Radiation Pattern Using CRM Method.....	33
Kalina Kalinovska and Kliment Angelov	
Infrared investigation on the thermal field in the case of influence of low frequency magnetic signals on live tissue.....	37
Kalin Dimitrov	
Statistical Characteristics of Optimal Divergence of Laser Beam at FSO Systems ...	41
Tsvetan Mitsev	
ANN Approach for Return Loss Analysis of Ohmic Series RF MEMS Switches.....	45
Tomislav Ćirić, Zlatica Marinković, Marija Milijić, Olivera Pronić-Rančić, Vera Marković, Larissa Vietzorreck	
Calculation of Capacitance of the Rectangular Coaxial Lines with Offset Inner Conductor by Strong FEM.....	49
Vladimir V. Petrovic and Žaklina J. Mančić	
Design and Analysis of Realistic Vehicle Traces Model based on the Evolutionary Algorithms	53
Danijel Čabarkapa and Petar Pavlović	
Transmitting coherent carrier frequencies in modern CATV/HFC systems.....	57
Oleg Borisov Panagiev	
Control of Photon Energy Sharing for Photovoltaic Power Charge in Power Grid of Optic Fiber With Enhanced Effectiveness	61
Jovan Shikoski, Juli Zlatev, Tinko Eftimov, Georgi Stanchev	
Polynomial-Based Extraction Procedure for Determination of HEMT Noise Wave Temperatures	65
Vladica Đorđević, Zlatica Marinković, Olivera Pronić-Rančić and Vera Marković	
Study the impact of the instability of oscillators in the Head End modules.....	69
Oleg Borisov Panagiev	
Mixer Linearization in Direct Conversion Receiver.....	73
Aleksandar Atanasković, Aleksandra Đorić and Nataša Maleš-Ilić	

TELECOMMUNICATION SYSTEMS AND TECHNOLOGY

Novel Transport protocol for 5G Networks	79
Ivan Petrov and Toni Janevski	
OP of SC Diversity for OFDM-based WLAN System Operating in Microcell and Picocell Environment.....	83
Aleksandra Panajotović, Dragan Drača and Nikola Sekulović	
Chromatic Polynomial Heuristics for Connectivity Prediction in Wireless Sensor Networks	87
Vladislav Vasilev	
Hybrid Environment Service Orchestration for Fog Computing	91
Stojan Kitanov and Toni Janevski	
Transformation of the existing operator in the service provider for business customers	95
Zlata Radak and Nataša Gospić	
2D Localization of Source of Stochastic EM Radiation by using Neural Networks...	99
Zoran Stankovic, Ivan Milovanovic, Nebojsa Doncov, Bratislav Milovanovic	
Analysis and evaluation of the human factor in the communication and information systems	103
Evgeniy Hubenov, Antonio Andonov, Zoya Chiflidzhanova	
Software development of Content Management System in Online-CADCOM platform.....	107
Ognyan Chikov	
Investigation of algorithms for VoIP signaling	111
Todorka Georgieva, Ekaterina Dimitrova and Slava Yordanova	
Contemporary Trends for Increasing the Reliability of the SCADA systems Communication Level.....	115
Emiliya Dimitrova and Vasil Dimitrov	
Transmission of multimedia data in Wireless Sensor Networks	119
Miloš Kosanovic and Mirko Kosanovic	
Performance analysis of FSO transmission over M atmospheric turbulence channels.....	123
Petar Spalević, Bojan Prlinčević, Stefan Panić, Mladen Veinović, Aleksandra Kokić Arsić	
Performance Analysis of Wireless Macrodiversity SSC Receiver in Gamma-Shadowed nLoS Fading Channel	127
Caslav Stefanovic	
Outage Performance of Satellite-Terrestrial Multiuser Networks with Fixed Gain AF Relay.....	131
Aleksandra M. Cvetkovic, Jelena A. Anastasov and Nemanja M. Zdravkovic	
Responsive Web Design in Online-CADCOM platform	135
Ognyan Chikov	

SIGNAL PROCESSING

Statistical Analysis of Round-off Noise in First-Order IIR DSP Systems	141
Zlatka Valkova-Jarvis, Kamelia Nikolova and Venera Dimitrova	
Novel CIC FIR Filter Functions: Design and Influence of Added Filter Blocks	145
Biljana P. Stošić, Vlastimir D. Pavlović	
Model of the Operational Conveyor based on Currentsteering output stage	149
Slobodan Djukic and Milan Veskovc	

The Evaluation of Speech Intelligibility in the Orthodox Church on the Basis of MOS Test Intelligibility Logatom Type CCV	153
Dijana Kostić, Zoran Milivojević and Violeta Stojanović	
Research and signal analysis with different classes of wavelets	157
Mariana Todorova and Reneta Ivanova	
Optimization of the parameter of 2P Keys interpolation kernel according to the criterion of similarity to sinc function in the spectral domain.....	161
Nataša Savić, Zoran Milivojević, Zoran Veličković, Darko Brodić	

DIGITAL IMAGE PROCESSING

Kernel based Extreme Learning Machines for Image Classification	167
Stevica S. Cvetković, Miloš B. Stojanović, Saša V. Nikolić, Goran Z. Stančić	
New interactive interface for visualization of 3D meshes.....	171
Nicole Christoff, Hadrien Greef, Sébastien Gormond-Mazet, Jean-Luc Mari, Laurent Jorda and Agata Manolova	
Comparison of Complex Hadamard Transform with other Unitary Transforms	175
Rumen P. Mironov	
Some Finger Vein Databases Evaluation	179
Ivo Draganov, Darko Brodić	
Tracking Dynamics Objects on Binocular Vision System.....	183
Rosen Spirov, Neli Grancharova and Svilen Soyakov	
An Approach for Renal Vessels Evaluation in US Images.....	187
Veska Georgieva, Stephan Vassilev	
The Insertion of the Encrypted Low-Resolution Watermark in the Uncompressed Video.....	191
Zoran Veličković, Zoran Milivojević and Marko Veličković	
Face Recognition using LBP and PCA under Different Lighting Condition	195
Dipak P. Patil, Pallavi. S. Sonar and Svetlin I. Antonov	

COMPUTER SYSTEMS AND INTERNET TECHNOLOGIES

Formal Verification of Models for M2M Device Registration.....	201
Evelina Pencheva, Ivaylo Atanasov and Anastas Nikolov	
Autonomous Agent Model for Connectivity Management in M2M Communications.....	205
Ivaylo Atanasov, Anastas Nikolov and Evelina Pencheva	
Integrated HPC Data-log Monitoring System.....	209
Kostadin Mishev, Sonja Filiposka, and Anastas Mishev	
E-content Development and Task Solution Using the Content Management System of Online-CADCOM.....	213
Galia Marinova and Ognyan Chikov	
SCADA system for monitoring and control of small industrial producing unit.....	217
Hristo Nenov	
Project of Crochet Software Development	221
Elena Zaharieva-Stoyanova	
Graph Construction Algorithm for finding the Shortest Path in a Maze.....	225
Milena Karova, Ivaylo Penev, Mariana Todorova, Hristian Bobev, Neli Kalcheva	

INFORMATICS AND COMPUTER SCIENCE

A Hybrid Metaheuristic Algorithm for Flexible Job Shop Scheduling “PSO&TS” ..	231
Asen Tochev and Vassil Guliashki	
NoTree.....	235
Iliya Tronkov	
Random Generation of Bent Functions on Multicore CPU Platform.....	239
Miloš Radmanović and Radomir S. Stanković	
Education of Patients by using Mobile Learning System.....	243
Dusan Tatić and Dragan Janković	
Versatile Program Model of Avatar Face.....	247
Milan Adamović, Dragan Ivetić, Aleksandar Kupusinac	
Hadoop – Next Generation of Business Intelligence Systems	251
Borivoje Milosevic, Srdjan Jovkovic and Marko Jankovic	
Formal Methods for Data Analysis	255
Blagovest Kirilov	
An Approach in Spatial Databases.....	259
Mariana Stoeva and Violeta Bozhikova	
Studying the process of software development through intensive use of software tools.....	263
Violeta Bozhikova, Mariana Stoeva and Dimitrichka Nikolaeva	
Statistical Analysis of Text Encryption Software.....	267
Darko Brodić, Ivo R. Draganov and Zoran N. Milivojević	

ELECTRONICS

Analytical Modeling of a ZVS Bidirectional Series Resonant DC-DC Converter... .	273
Aleksandar Vuchev, Nikolay Bankov, Yassen Madankov and Angel Lichev	
Load and Control Characteristics of a ZVS Bidirectional Series Resonant DC-DC Converter	277
Aleksandar Vuchev, Nikolay Bankov, Yassen Madankov and Angel Lichev	
Two-Phase Switching-Mode Converter with Zero Voltage Switching Designed on CMOS 0.35 μm Technology	281
Tihomir Brusev, Georgi Kunov and Elissaveta Gadjeva	
Converters with Energy Dosing for Charging of EV’s Li-ion Batteries.....	285
Nikolay Madzharov and Goran Goranov	
Mathematical model of thermoelectric Peltier module	289
Liliya Staneva, Ivaylo Belovski, Anatoliy Alexandrov and Pavlik Rahnev	
Mathematical model of control system based on programmable environment.....	293
Anatolii Aleksandrov, Goran Goranov, Pavel Hubenov	
Electronic Module for 2D Positioner Manuel Control	297
Nikola Draganov, Totka Draganova and Dragan Draganov	
Study of Nonlinear Effects in Parallel Gyration Resonance Circuits.....	301
Atanas Tanev, Ivan Uzunov, Marin Hristov, Sotir Ouzounov	
Problems and Properties of a Current Amplifier When Realized in Ultra Deep Sub-micron Technology.....	305
Simeon Kostadinov, Ivan Uzunov, Dobromir Gaydazhiev	
Optimization and analysis ALL Digital PLL For resonant inverter.....	309
Goran Goranov, Nikolay Madzharov	
Design and Realization of a 12W Quasi-Resonant Flyback Converter	313
Zoran Zivanovic and Vladimir Smiljakovic	

Two-Phase Switching-Mode Converter with Zero Voltage Switching Designed on CMOS 0.35 μm Technology

Tihomir Brusev¹, Georgi Kunov² and Elissaveta Gadjeva³

Abstract –A two-phase switching-mode dc-dc converter with Zero Voltage Switching (ZVS) is presented in this paper designed on CMOS 0.35 μm technology with Cadence. The losses in the main power transistors are evaluated. The investigation results show that when ZVS technique is used, the efficiency of the whole system could be increased by about 3% compared to the standard two-phase dc-dc converter architecture.

Keywords – Two-phase switching-mode converter, Zero Voltage Switching (ZVS), Efficiency, CMOS technology, Cadence.

I. INTRODUCTION

Today smart phones can transfer large data packages in a real time, thanks to the fourth generation Long-Term Evolution (4G LTE) wireless communication standard. The great functionality of modern telecommunication devices is due to the use of OFDM (Orthogonal Frequency-Division Multiplexing) modulation. The signal is transferred by several sub-carrier frequencies, which are summed at the output of modulator. Thus the spectrum in 4G LTE standard is used much more effectively [1].

On the other hand the sizes of the new mobile phones became larger, which allows increasing of the battery dimensions. Nevertheless, the time between two consecutive charges is small. The efforts of the designers are focused over the increasing of power supplies efficiency. Those circuits have to ensure the desire energy of transmitter's power amplifier (PA). The standard switching-mode dc-dc converter cannot fulfill the requirements to deliver appropriate fast dynamically changeable output voltage to drain or collector, respectively of MOS or BJT RF transistor of PA.

The power supply circuit, which provides the desire energy to transmitter's PA is called envelope amplifier. The block diagram of envelope tracking power amplifier's system is shown in Fig. 1. Envelope amplifier delivers the drain or collector supply voltage of PA's transistors [2]. It dynamically changes this supply voltage according to the variations of the PA input signal. The envelope amplifier tracks the PA input signal and controls the PA supply voltage according to the

envelope of this signal. The efficiency η_{ETPA} of the envelope tracking power amplifier's system is equal to [3]:

$$\eta_{ETPA} = \eta_{EA} \cdot \eta_{PA}, \quad (1)$$

where η_{EA} is the efficiency of the envelope amplifier; η_{PA} is respectively the efficiency of the PA. The run-time of wireless communication devices could be increased if envelope amplifier with high efficiency is designed.

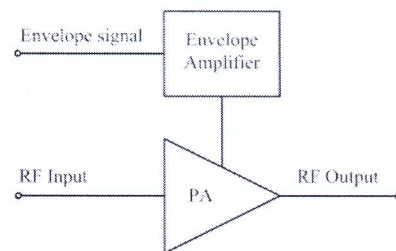


Fig. 1. Envelope tracking power amplifier's system

Most of the envelope amplifier's architectures include parallel or series connected linear amplifier and switching-mode dc-dc converter. Switching-mode converter ensures between 70% and 80% energy delivered to PA [2]. Therefore, high efficient dc-dc converter could improve significantly the efficiency of envelope amplifier. One of the features of switching-mode converters is that they are good choice only when relatively low-data rate communication signal is transferred. The tracking speed of the switching-mode converter could be increased if the single phase dc-dc converter is replaced by two-phase converter. Thus the portion of energy distributed from low efficient linear amplifier in envelope amplifier will be smaller, compared to the case when the switching-mode amplifier is a single phase dc-dc converter. This leads to improving of the overall efficiency of envelope tracking power amplifier system.

The tracking speed possibilities of standard synchronous single phase dc-dc converter and two-phase interleaved buck converter are discussed in Section II A of this paper. In Section II B, the Zero Voltage Switching (ZVS) technique is considered, which helps to reduce power losses in the main transistor of switching-mode dc-dc converters. Two-phase dc-dc converter with ZVS is designed with Cadence on CMOS 0.35 μm process. Power losses in the main power MOS transistors are considered and evaluated. The efficiency results of two-phase dc-dc converter with ZVS are evaluated and compared to the efficiencies of the standard two-phase interleaved dc-dc converter. The received results are presented in Section III.

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II. SWITCHING-MODE CONVERTERS

A. Single phase and two-phase switching-mode converters

The standard synchronous single phase dc-dc converters, shown in Fig. 2, indicate high power losses in the inductor at large values of the inductor current ripple Δi_L . The two-phase converter structure helps to reduce this negative effect [4].

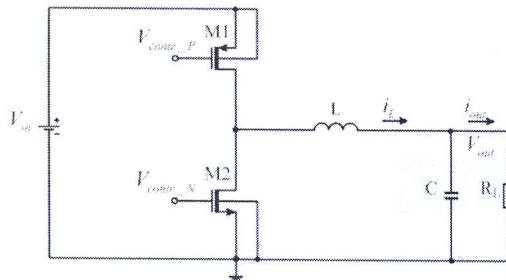


Fig. 2. Single phase dc-dc converter

The two-phase interleaved dc-dc converter architecture, presented in Fig. 3, leads to reduction of the output current ripple Δi_{out} of the circuit. The reason is that the phase sifted inductor current ripples respectively of the first and second sub-converter stage Δi_{L1} and Δi_{L2} are summed at the output.

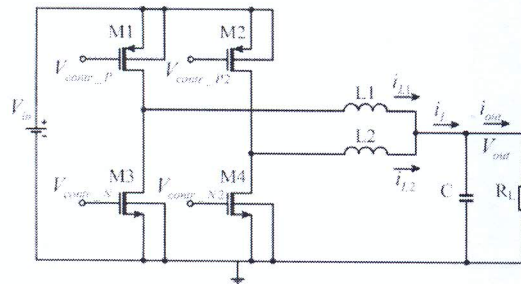


Fig. 3. Two-phase interleaved dc-dc converter

The output current ripple Δi_{out} of the two-phase interleaved buck converter with non-coupled inductors can be expressed in the form [5]:

$$\Delta i_{out} = \frac{V_{out}}{L} (1 - 2D) T_s, \quad (2)$$

where T_s is the switching period of converter, L is the value of filter inductors (if $L1=L2$, which is the case of the investigated dc-dc converter architecture).

Minimum values of the output current ripple Δi_{out} can be received if the duty cycle of the converter D is close to 0.5. The inductor current ripples Δi_L of the single phase buck dc-dc converter and two-phase interleaved buck converter with non-coupled inductors have equal values, and can be expressed in the form [5]:

$$\Delta i_L = \frac{V_{out}}{L} (1 - D) T_s. \quad (3)$$

In two-phase interleaved dc-dc converters architectures the same output current ripples as those of single-phase dc-dc converters could be established with smaller values of output filter inductors respectively $L1=L2$. These phenomena could be very useful for LTE applications power supply circuit, when envelope amplifier has to be fast in order to track high frequency envelope signal. The two-phase dc-dc converter could replace the single phase switching-mode regulator in parallel hybrid envelope amplifier structure. Thus most of the energy delivered to power amplifier can be ensured from fast and high efficient switching-mode multiphase dc-dc converter. The portion distributed from low efficient linear amplifier will be smaller, compared to the case when switching-mode amplifier is a single phase dc-dc converter, improving the overall efficiency of envelope tracking power amplifier system.

B. Zero Voltage Switching

The circuit of synchronous single phase switching-mode buck dc-dc converter with ZVS is shown in Fig. 4. The advantage of those types of circuits is that the main power transistor $M1$ can be switched-on and switched-off respectively at zero voltage [6].

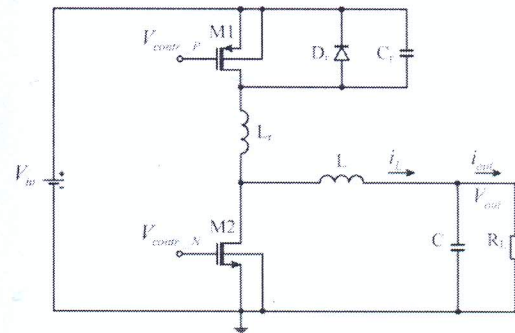


Fig. 4. Single phase dc-dc converter with ZVS

The zero voltage switch-off of the main PMOS transistor $M1$ of dc-dc converter is because of the capacitor C_r . The Zero voltage switching-on state of the PMOS transistor $M1$ is ensured by the diode D_r . The function of this component is to clamp to zero capacitor voltage V_c , when transistor $M1$ is at switch-off state [6].

The effect of ZVS will lead to zero switching power losses of main PMOS transistor $M1$. Thus the total power losses in the MOS transistors of synchronous dc-dc converter could be decreased. They are equal to [7]:

$$P_{tot,MOS} = a \sqrt{\left(I^2 + \frac{\Delta i_L^2}{3} \right)} f_s, \quad (4)$$

where Δi_L is the inductor current ripple, I is a dc current

supplied to the load, and a is a coefficient depending on the equivalent series resistance of the transistors, the input total capacitance of the MOS transistors C_{tot} and the power supply V_m . The decreasing of total power losses in MOS transistors of dc-dc converter will improve the efficiency of the circuit. The efficiency of the buck dc-dc converter can be expressed by:

$$\eta = \frac{P_{out}}{P_{out} + P_{losses}}, \quad (5)$$

where P_{out} is the output power of the dc-dc converter; P_{losses} are overall power losses in the dc-dc converter.

III. INVESTIGATION OF TWO-PHASE SWITCHING-MODE CONVERTER WITH ZVS

The two-phase switching-mode converter with ZVS is designed with Cadence on AMS CMOS 0.35 μm 4-metal technology. The block circuit of whole buck dc-dc converter system is presented in Fig. 5. It consists of two power buck stages, error amplifier, ramp generator, comparator and buffer stage. In the designed two-phase switching-mode converter, Pulse-Width Modulation (PWM) control technique is used.

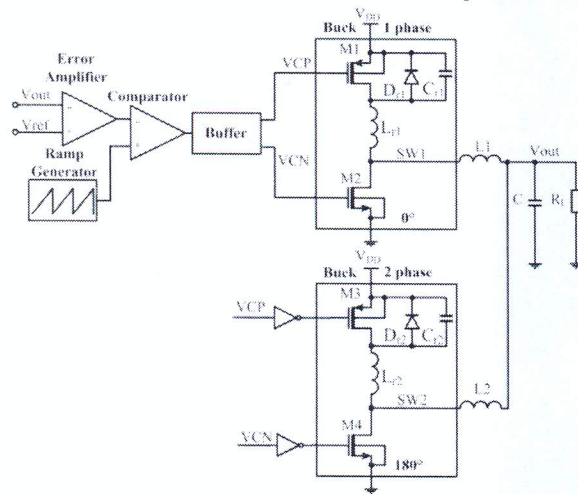


Fig. 5. Two-phase switching-mode converter with ZVS

The control signals, which regulate the main power MOS transistors of the both power buck stages, are 180° phase shifted. The supply voltage V_{DD} is equal to 3.6 V, which is a standard output voltage of lithium-ion battery. The average value of the output voltage $V_{out(av)}$ of the converter is regulated to be equal to 1.2 V. The output filter inductors $L1$ and $L2$ of the both power buck stages are equal to 125 nH. The filter capacitor C is equal to 400 pF. The switching frequency f_s of the two-phase dc-dc converter with ZVS is equal to 76 MHz. The PMOS transistors $M1$ and $M3$ in both buck power stages are represented by 6 equal “*modprf*” transistors connected in parallel. Their sizes (W/L) are respectively 150/0.35 [μm]. For NMOS transistors $M2$ and $M4$, which replace the diode in the standard buck dc-dc converter circuit, 4 equal connected

in parallel “*modprf*” transistors are used. Their sizes (W/L) are respectively 200/0.35 [μm]. The values of resonant inductors L_{r1} and L_{r2} are equal to 10 nH. The values of resonant inductors C_{r1} and C_{r2} are equal to 50 pF. The waveform of output voltage V_{out} of the two-phase switching-mode converter with ZVS is shown in Fig. 6.

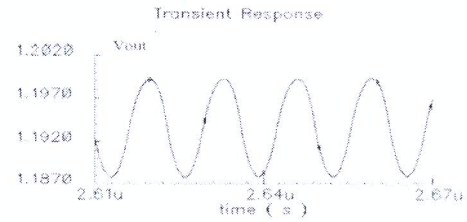


Fig. 6. The waveform of output voltage V_{out} of the two-phase switching-mode converter with ZVS

The waveforms respectively of I_{L1} and I_{L2} of two-phase switching-mode converter with ZVS are presented in Fig. 7.

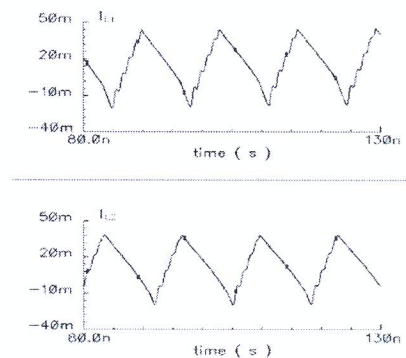


Fig. 7. Waveforms of the inductor currents I_{L1} and I_{L2} of two-phase switching-mode converter with ZVS

The waveforms of control signal VCP , which regulate the mode of operation of main PMOS transistors of the first buck stage, and the capacitor’s voltage V_C are shown in Fig. 8.

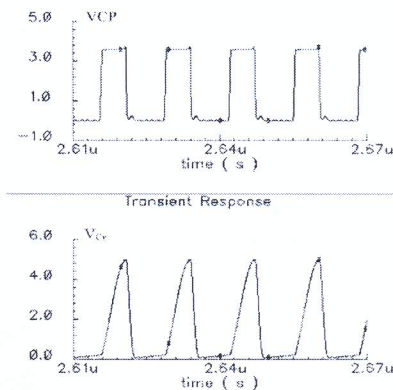


Fig. 8. The waveforms of control signal VCP and the capacitor’s voltage V_C

The total power losses in main PMOS transistors (P_{PMOS}) of two-phase dc-dc converter, designed on CMOS 0.35 μm technology, are investigated as a function of the load R_L . The investigations are performed when the circuit works with and without ZVS. The efficiencies of two-phase switching-mode converter, respectively with and without ZVS are evaluated. The received results are presented in Table I.

TABLE I
POWER LOSSES IN MAIN PMOS TRANSISTORS AND EFFICIENCY OF TWO-PHASE DC-DC CONVERTER AS A FUNCTION OF LOAD R_L , RESPECTIVELY WITH AND WITHOUT ZVS

	$R_L=10$ [Ω]	$R_L=20$ [Ω]	$R_L=25$ [Ω]	$R_L=30$ [Ω]
P_{PMOS} [mW]	21.4	13.8	11.8	8.7
$P_{PMOS-ZVS}$ [mW]	19.4	11.4	9.6	6.3
Efficiency [%]	67.89	71.25	74.2	76.84
Efficiency-ZVS [%]	69.14	73.43	76.14	78.26

All the results shown in Table I are received when average value of the output voltage $V_{out(av)}$ of converter is equal to 1.2 V.

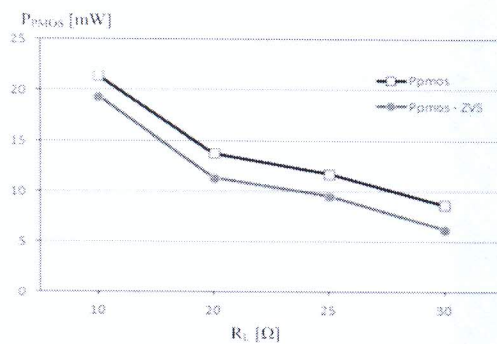


Fig. 9. Power losses P_{PMOS} of two-phase dc-dc converter as a function of load R_L with and without ZVS

The power losses of PMOS transistors of two-phase dc-dc converter are presented graphically in Fig. 9 as a function of the load R_L with and without ZVS.

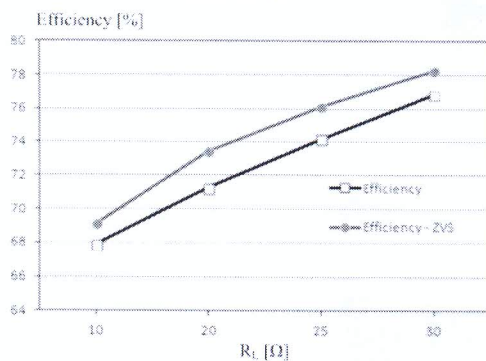


Fig. 10. Efficiency of two-phase dc-dc converter as a function of load R_L , respectively with and without ZVS

As it can be seen from the picture shown in Fig. 9, the total power losses in the main transistors of two-phase switching-mode ($M1$ and $M3$) are decreased by about 11% when ZVS technique is used. The reason is that switching power losses are minimized. This effect can be seen in Fig. 10, where the efficiency results of two-phase dc-dc converter as a function of the load R_L are graphically presented. As it can be seen from the picture efficiency of the whole converter system is increased by about 3% when ZVS is used. The values of the load resistance R_L are changed between 10 Ω and 30 Ω , because this range represents the practical equivalent value of PA used as a load [8].

IV. CONCLUSION

In this paper two-phase buck dc-dc converter with ZVS designed on CMOS 0.35 μm technology has been proposed. This circuit could be used as switching-mode regulator in parallel hybrid envelope amplifier for LTE applications. The investigation result shows that efficiency of two-phase dc-dc converter can be increased by about 3% if ZVS technique is used. The reason is that the total losses in the main switch of the converter's power stage are minimized.

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