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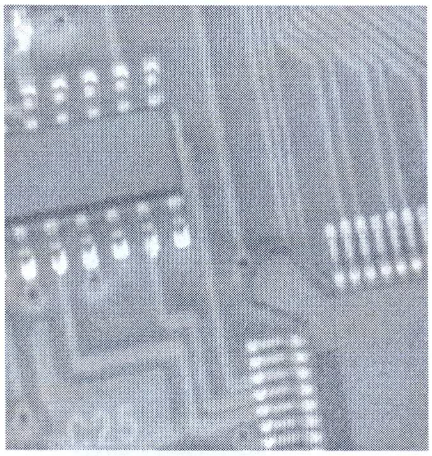

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Investigation of Parallel Hybrid CMOS Envelope Amplifier Designed on AMS 0.35 µm Process

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***Abstract*—Customer demands for battery powered portable electronic devices have increased. Today high data rates could be transmitted using fourth generation Long-Term Evolution (4G LTE) wireless communications standard. To increase system run-time proper envelope amplifier's architecture has to be selected. Using envelope tracking technique efficiency of the transmitter's power amplifier (PA) can be improved. In this paper different circuit architectures of envelope amplifier are considered. Parallel combined hybrid structure is designed using CMOS 0.35 µm technology. Switching-mode buck converter operates with switching frequency f_s up to 80 MHz to address the wide bandwidth of LTE envelope. The maximum simulated efficiency of the envelope amplifier is 79. 8 %.**

***Keywords*—envelope amplifier, Cadence, efficiency, 4G LTE, CMOS technology**

I. INTRODUCTION

The handheld battery powered portable electronic devices like smart phones and tablets are used everywhere in our life. The new wireless communications 4G LTE standards is already widespread used. Voice audio signal and large date packages like broadband TV signal, mobile web browsing etc., could be transferred. This is possible, because OFDM (Orthogonal Frequency-Division Multiplexing) modulation is used in LTE. Power consumptions of the building blocks of new generation mobile communication devices are incredibly increased. New energy saving method needs to be developed and used to increase the battery life. The most energy consuming building block of the transmitter is the power amplifier (PA). In LTE those circuit have to work with very high peak to average power ratio (PAPR). This leads to efficiency degradation, because in the majority of the operation time power amplifiers have to work in the back-off mode of operation. Increasing the system run-time is big challenge for the designers. Another very important requirement for PAs is the linearity, which is necessary for LTE applications because it helps to avoid interference with nearby users. Unfortunately, a disadvantage of the linear PAs is their low efficiency.

Envelope tracking method is very good technique for efficiency improving of linear power amplifiers, which is reported in the literature [1], [3], [5], [7], [8], [10]. In Fig. 1 is shown the basic block diagram of envelope tracking power amplifier's system. The envelope amplifier there is used to deliver the drain or collector supply voltage of PA's transistors [2]. It dynamically changes this supply voltage according to the variations of the PA input signal. When the linear PA is in back-off mode of operation, this technique moves the PA supply voltage closer to the envelope of the signal, which improves the efficiency.

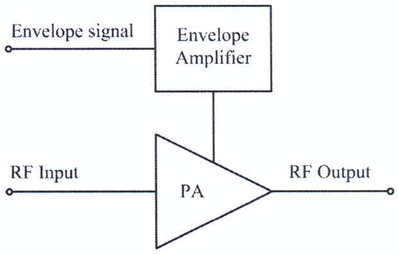

Fig. 1. Envelope tracking power amplifier's system.

An example of envelope amplifier designed on Austria Microsystem (AMS) 0.35 µm CMOS process is shown in this paper. Its building blocks are combined from various sources and modified appropriately according process requirements. The presented simulation results confirm the basic design concepts. The basic requirements for LTE transmitter's PA and the architecture of the envelope amplifier are discussed briefly in Section II. The building blocks of the envelope amplifier are described in Section III together with simulation results, characterizing them.

II. ENVELOPE TRACKING POWER AMPLIFIER SYSTEM

A. Power Amplifier

Linear PA's have to work at large back-off, because signals in LTE wireless communications standard have high values of PAPR. The efficiency of the power amplifiers decreases when they work in back-off mode of operation if constant supply voltage is used. The linear power amplifier consumes equal dc energy for large and low input signal and its maximum efficiency is when it works with high input signal. The PA input signals in the LTE standard are low in the most of the operating time and the efficiency of PA is unacceptable small during that time. As it is seen in Fig. 1 the envelope tracking system includes a PA and an envelope amplifier, delivering the supply voltage for the PA. The

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envelope amplifier tracks the PA input signal and controls the PA supply voltage according the envelope of this signal. Thus the efficiency $\eta_{ET\,PA}$ of the whole system in Fig. 1 is defined by the efficiencies of both amplifiers (PA and envelope) according the formula [3].

$$\eta_{ET\,PA} = \eta_{EA} \cdot \eta_{PA}, \qquad (1)$$

where η_{EA} is the efficiency of the envelope amplifier; η_{PA} is respectively the efficiency of the PA. Evidently both stages should have high efficiency in order to increase the battery run-time efficiency of the mobile communication system.

The LTE standard includes signals with various bandwidths (1.4; 3; 5; 10; 20; 40 MHz), i.e. the bandwidth extends up to 40 MHz with a trend of further increase. In the new mobile portable devices all available communication standards have to be covered. This requirement makes the task to design high efficiency power amplifier system more complicated, because obviously more than one PA in the transmitter is needed [4].

B. Envelope amplifier's architectures

The function of the envelope amplifier is to supply dynamically changeable supply voltage to the RF PA. The development of the LTE standard leads to increased signal bandwidth, respectively increased envelope frequency, which means that the envelope amplifier should have fast tracking speed. This makes the choice of proper envelope amplifier's architecture a challenge and it is still difficult to define which the best structure is. Some brief considerations are given below.

If only standard switching-mode converter is used to perform the functions of envelope amplifier (as it is in the GSM transmitters), then its switching frequency f_s have to be 5 to 10 times higher than the bandwidth of the LTE signal (when standard pulse-width modulation (PWM) control is used) [6]. Then f_s become very high and this high switching frequency leads to unacceptable large power dissipation in the dc-dc converter. The consequence is degradation of the converter's efficiency and respectively degradation the efficiency ($\eta_{ET\,PA}$) of the whole PA system. On the other hand switching-mode buck converters are good choice when relatively low-data rate communication signal is transferred.

Another option is LDO (low drop-out) regulators having wider bandwidth than switching buck dc-dc converter. They have also small output ripples and this leads to very good out-of-band spectral performance. The big disadvantage of LDO regulators is their low efficiency, especially when the difference between the output and the input voltage of its linear regulator is large. Unfortunately during most of the time the envelope amplifier works in this mode of operation.

The proper combination between linear amplifier and switching regulator could be a good decision for envelope amplifier structure. Different types of envelope amplifiers architectures are proposed in the literature. In most of cases hybrid combination of switching type dc-dc converter and linear amplifier are used [1], [4], [7], [10]. In Fig. 2 is shown parallel combined switching and linear amplifier topology. An example of such combination is the parallel combined switching and linear amplifier topology in Fig. 2, which is investigated here.

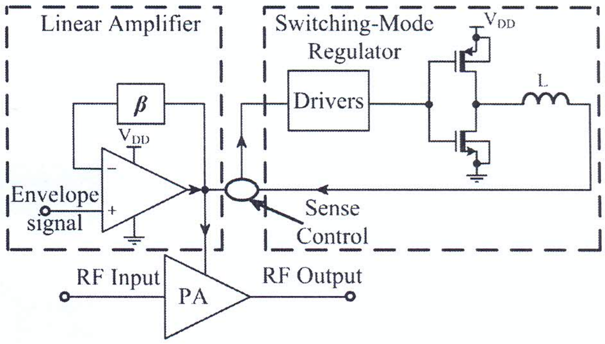

Fig. 2. Parallel combined switching and linear regulator topology of envelope amplifier.

This envelope amplifier's architecture combines advantages of switching and linear stages of step-down converters. Basically the switching stage has to supply the average power to PA. On the other hand the linear amplifier has to filter the current ripples generated from switching type of converter and also to deliver the rest part of the power to PA, when switching regulator cannot respond quickly. Therefore linear amplifier should have low output impedance at the frequency of the ripples of the switching-mode regulator and also wide bandwidth in order to cover the envelope frequency [8]. Most of the energy (between 70 % and 80 %) to power amplifier is delivered by the switching-mode stage of the envelope amplifier, which improves its overall efficiency [2]. The rest of the energy necessary for PA is supplied by the linear stage. Overall efficiency of the envelope amplifier is a ratio between average powers at its input (taken from the battery) and its output (delivered to PA):

$$\eta_{EA} = \frac{P_{out,avg}}{P_{in,avg}}, \qquad (2)$$

Recently was proposed a new solution for envelope amplifier architecture without linear stage [6]. It is based on interleaved two-phase switching buck converter architecture, and uses relatively complicated control technique.

III. INVESTIGATION OF PARALLEL HYBRID ENVELOPE AMPLIFIER TOPOLOGY

Parallel combined envelope amplifier architecture is analyzed and investigated. The block diagram shown in Fig. 3 is designed using CMOS 0.35 μm process. The circuit's topology consisting of linear amplifier and switching buck converter stage has been presented in Section II. The simulations of the envelope amplifier are performed by Cadence on AMS technology. This structure of the hybrid amplifier uses the advantages of both stages respectively: high possible efficiency of the switching type of converters and broadband characteristics of linear regulators.

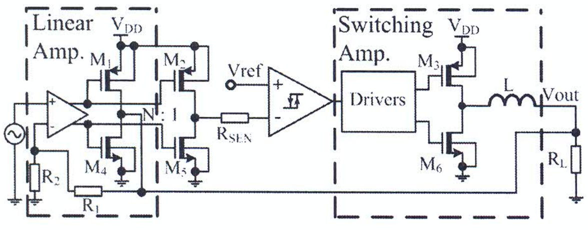

Fig. 3. Simulated block diagram of CMOS envelope amplifier.

Hysteresis control is used to regulate switching buck converter's modes of operation. Supply voltage V_{DD} is chosen to be equal to 3.6 V, which a standard output voltage of lithium-ion battery. The load resistance R_L of envelope amplifier represents the current load of RF PA. The output of the linear amplifier is formed by transistors M1 and M4. Current mirroring ratio N:1 is defined between the ratio of transistors sizes of M1-M4 to M2-M5, which in the investigated topology is equal to 250. The value of the inductance, which is inversely proportional to switching frequency f_s is equal to 250 nH. Increasing the inductor's value leads to decreasing of the output current ripple of buck converter.

In Fig.4 is presented the used circuit of comparator with hysteresis.

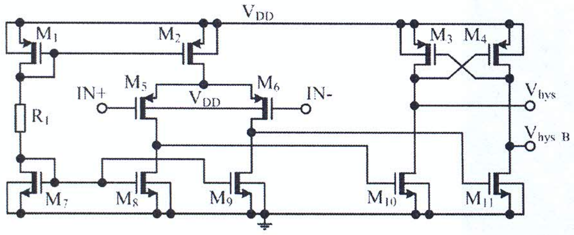

Fig. 4. Simulated circuit of comparator with hysteresis.

The switching frequency f_s of buck converter when hysteresis control is used can be calculated by the formula [1], [2]:

$$f_s = \frac{R_{sen} V_{out} \left(V_{DD} - V_{out} \right)}{2 V_{DD} N L V_{hys}}, \tag{3}$$

where R_{SEN} is a sense resistor; V_{out} is the output voltage of the envelope amplifier; V_{DD} is the supply voltage; N is current mirroring ratio; L is the filter inductance in Fig. 3 and V_{hys} hysteresis of comparator. Both stages, linear amplifier and switching-mode buck converter, have been investigated separately in order to evaluate their performance limit. The maximum switching frequency f_s of the buck converter is 80 MHz to address the wide bandwidth of LTE envelope. The switching frequency f_s is selected to be high in order to evaluate whether envelope amplifier can meet a possible future bandwidth increase.

The input signals of the comparator with hysteresis, when input signal frequency is equal to 20 MHz, are presented in Fig. 5. The sinusoidal signal shown in Fig. 5 is V_{ref}, while V_{sen} is output voltage signal of the transistors M_2 and M_5. The sinusoidal signal emulates fast changing LTE envelope and it is used in this simulations as a test signal to evaluate the tracking speed of the buck converter. This test signal does not represent the shape of the real envelope signal, but it is used nevertheless because of its simplicity for circuit simulation.

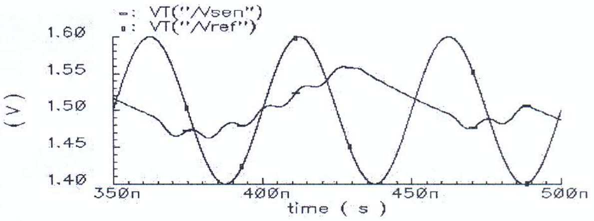

Fig. 5. Input signals of the comparator with hysteresis.

The schematic of the driver used in switching-mode regulator is presented in Fig. 6 [9]. This topology prevents the short-circuit losses, providing a short gap time when NMOS and PMOS transistors are both switched-off.

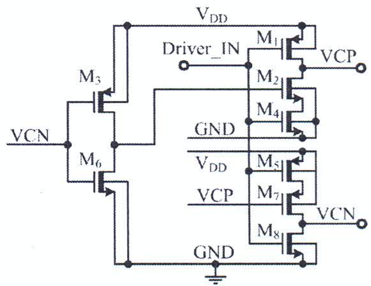

Fig. 6. Schematic of the switching-mode buck convertre's driver [9].

Simulations results of control pulses VCP and VCN, which regulate respectively PMOS and NMOS output transistors of the buck converter, are shown in Fig. 7.

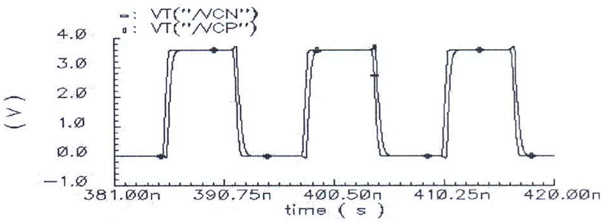

Fig. 7. Driver's output control sygnal.

The pulse width of VCP is larger than VCN signal, thus the PMOS transistor is switching-off before switching-on of the NMOS transistor. The obtained simulations results show that maximum efficiency of the switching-mode buck converter stage is 88%.

The circuit of the investigated linear amplifier is shown in Fig. 8 [10], [11]. This stage includes source-coupled differential amplifier and class-AB output stage formed by transistors M5 and M18. The linear amplifier is optimized for resistance load of 10 Ω, which is practical equivalent value of PA used as a load [1], [10].

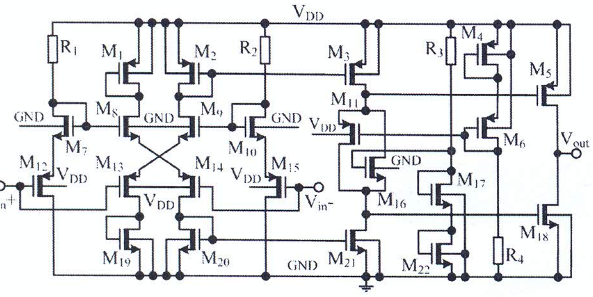

Fig. 8. Sumulated linear amplifier cicuit's topology[7].

Simulation results show that this stage could deliver output power up to 1.5 W, with maximum efficiency of 47%. The linear amplifier is used as an active filter to suppress the output ripple formed by switching-mode regulator. This is achieved thanks to the low output impedance of the linear amplifier. The bandwidth of the linear amplifier should be wide – around 6 times of the signal bandwidth [10].

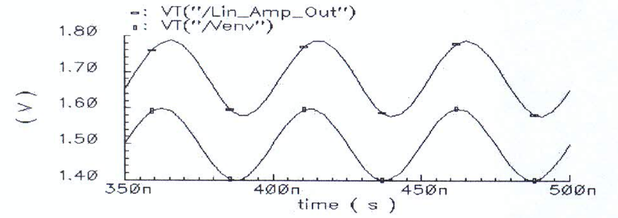

Fig. 9. Simulated resuls of envelope signal, which is the upper sinusoidal signal in the figure and linear amplifier's output signal.

In Fig. 9 are shown simulation results of linear amplifier's output signal, when the frequency of the envelope signal is 20 MHz. The output power delivered to the load by the linear amplifier itself is equal to 270 mW. The maximum simulated efficiencies of the stand alone linear amplifier and stand alone dc-dc converter are respectively: 47% and 88%. Switch-mode converter delivers approximately 80% of output power, while the rest is supplied by the linear amplifier [2]. Using simple calculation based on obtained efficiency data, the estimated efficiency of the presented envelope amplifier is 79.8%.

IV. Conclusions

In this paper are presented investigation results of parallel hybrid topology of envelope amplifier, designed on AMS CMOS 0.35 μm process. Possible circuit's architectures of envelope amplifiers for LTE applications are discussed. Maximum simulated efficiency of the envelope amplifier is 79.8%. The obtained results are similar to those reported in other literature.

Acknowledgment

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