Monolithic Buck Converter for CMOS Process Technologies

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***Abstract*—Monolithic switching buck (step-down) converter is designed on standard 0.35-µm CMOS process. Different control techniques such as Pulse-Width Modulations (PWM) and Pulse-Frequency Modulations (PFM) are investigated. The received results show that PFM control indicates higher efficiency at light-loads compare to standard constant frequency PWM control. Efficiency of about 76 % is achieved for the PWM control at switching frequency of 150 MHz for voltage conversion from 3.6 down to 1.2V.**

I. INTRODUCTION

The market of handheld portable electronic devices such as cellular phones is rising very fast. The requirement to increase the battery life and the system run-time of these devices becomes stringent. To reduce the power dissipations is necessary subsystems to operate at its optimum supply voltages. A highly efficient DC-DC converter covering large load range has to be designed. Step-down voltage conversion is widespread used in most of the applications. The buck converters have a possibility to achieved higher efficiency compare to linear regulators [1]. Another important issue is to decrease the size and price of the converters. One of the major problems here is large silicon area which is occupied by the monolithic passive devices. In addition, the available inductors in 0.35-µm CMOS process have low quality factor.

The custom designed monolithic voltage converters for individual loads have high efficiency and their volumes are small. The standard PWM control, which is constant frequency method, is widely used to maintain a fixed voltage to output of the converter. When the converter operates with high load, the circuit work in the basic mode and high efficiency could be achieved. In most of the portable electronic devices, a light-load operation or standby mode is a key to achieve longer battery life, and at this mode the system should also indicate high efficiency. Because of the switching losses dominating at the light-load conditions, the efficiency of the converter goes down dramatically. This is a big problem when the PWM control technique is used. One of the solutions to decrease the switching losses is lower the switching frequency, but this will be increase the size, respectively the cost, of the filter components and especially of the inductor. The PFM control method can be used as an alternative of PWM control when the battery powered electronic devices are in standby mode [2]. By combining of these two control methods high efficiency buck converter could be designed at wide range of the load.

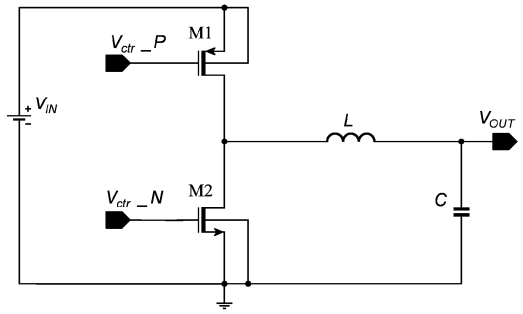

Figure 1. Synchroneous buck converter schematic.

This paper presents a power efficiency investigation of two different control techniques applied to monolithic buck converters designed on 0.35-µm CMOS process. The investigation assumes off-chip filtering components. In Section II are shown the simulation results for the power buck stage. The designed PWM and PFM controls of the buck converter are presented in Section III.

II. EFFICIENCY INVESTIGATION

Figure 1 shows the circuit of a buck converter implemented on standard CMOS 0.35-µm technology. The NMOS and PMOS transistors, which are forming the power stage, are synchronously controlled in a way that when one of the transistors is switched-on the other is switched-off. In the following, the efficiency performance of the power stage is evaluated assuming ideal drivers with the goal to select an appropriate switching frequency and filtering components.

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At high switching frequencies the losses in the transistors are inadmissibly large and the efficiency of the converter decreases. The efficiency of the converter can be expressed as:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \quad (1)$$

where P_{OUT} is the average output power, P_{IN} is the average input power, and P_{LOSS} are all power losses occurring in the power transistors, as well as in the controlling stages. To obtain high converter efficiency, all conversion losses should be kept to a minimum.

The conducting losses in the transistors are proportional to the switching frequency *fs* and the *rms*-value of the current flowing through the device [3]. This relationship is repeated bellow:

$$P_{MOS} = k_1 i_{rms}^2 + k_2 f_s \quad (2)$$

where k_1 and k_2 is are technology dependent coefficient, which are taking into account the size of the power MOS, as well as the resistive and the capacitive losses associated with the MOS structure. Small inductor ripple current will result in smaller *rms*-value of the current through the MOS structure, and it will respectively lead to better efficiency.

For the efficiency investigation of the buck converter an input voltage of 3.6V is chosen for the converter, since this is the normal voltage for Lithium-Ion battery cell that is typically used in battery-powered devices. The output voltage V_{out} is regulated to 1.2V, which on the other hand is determined by the breakdown voltages of advanced CMOS processes.

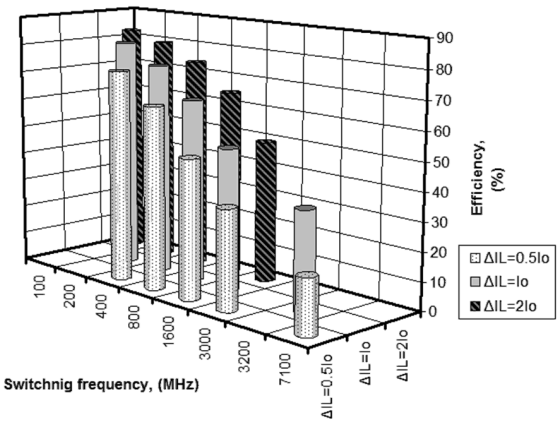

Figure 2. Efficiency as a function of switcing frequency f_s and inductor current ripple ΔI_L.

In Figure 2 presents the efficiency as a function of the switching frequency f_s and the inductor current ripple ΔI_L. The investigation shows degraded efficiency performance of the converter when the switching frequency f_s is increased. The value and respectively the size of the filter inductor L is reverse proportional to the inductor current ripple ΔI_L, i.e. smaller inductor can be used if bigger ripples are allowed. On the other hand the energy stored in the inductor is proportional to the physical size of the inductor [4].

$$E_{L_f} = 0.5 L_f \left(I_o + 0.5 / \Delta I_L\right) \quad (3)$$

The preferred value of ΔI_L depends on the inductor size and efficiency requirements of the converter applications. As can be seen from Figure 2, the best efficiency results are achieved when $I_o \leq \Delta I_L \leq 2I_o$, where I_o is dc output current of the converter. The efficiency of converter is slightly improved at larger current ripples, because the converter approaches the Zero-Voltage Switching (ZVS) conditions and part of the capacitive losses are restored [4].

III. PWM AND PFM CONTROL LOOP ARCHITECTURES

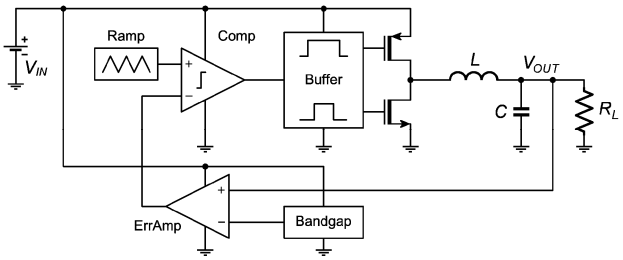

Figure 3. PWM block diagram

The block diagram of the switching-mode DC-DC buck converter system using standard PWM control loop is shown in Figure 3. The system consists of bandgap reference, error amplifier, ramp generator, comparator, buffer and power buck stage. The power losses in the controlling stages are minimized in order to improve the overall converter efficiency η. The nominal supply voltage of the converter is 3.6 V and steps-down to 1.2. The system operates at switching frequency *fs* of 150 MHz.

The bandgap voltage reference provides a stable voltage for the whole converter system that is independent from the power supply, load current, and temperature variations. This stage consumes only 0.27 mA, which helps to improve η.

The error amplifier determines the control voltage, which amplifies the difference between the output voltage V_{out} and the reference voltage V_{ref}. The ramp generator is a part of the regulation system, which performs the Pulse-Width Modulation (PWM) control. This stage determines the switching frequency *fs* of the buck converter. The control pulses for the power transistors are generated by comparing the sawtooth signal generated by the ramp generator and the control signal from the error amplifier. The comparator generates rectangular pulses whose duty-cycle is a function of the output voltage, and the PWM control loop regulates the output to the desired value.

The buffer stage delivers the controlling pulses for the power transistors. The short-circuit losses are prevented by providing a short gap time during which the NMOS and the PMOS transistors are both switched-off [5]. Thus, power losses generated due to this phenomenon are avoided.

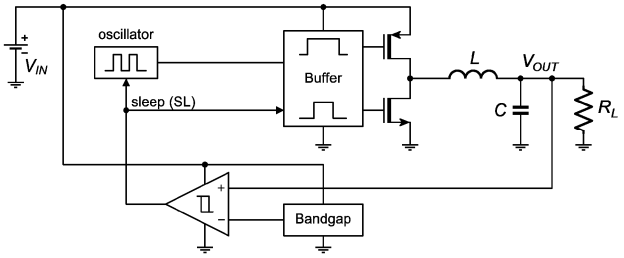

Figure 4. PFM block diagram

The block diagram of the converter utilizing a PFM control technique is shown in Figure 4. Here, a generator with a fixed duty-cycle (50%) is used to drive the power transistors. The voltage regulation is achieved by turning on and off the control loop. When the output voltage exceeds a predefined value, the comparator generates a control signal, which puts the whole system in sleep mode. In sleep mode, the filtering capacitor *C* delivers power to load, while all active blocks are disabled, except the comparator and the bandgap. When the output voltage goes below certain value, the comparator wakes up the system and the normal operation is restored. This technique allows minimization of the static control block consumption in light-load conditions, thus the overall efficiency is improved.

The output level-detect comparator should have a hysteresis in order to provide the control loop functionality. Two comparators without hysteresis and a logic circuit can also be used, but with the expense of more silicon area, and respectively higher static power consumption. The schematic of the comparator with the build-in hysteresis is shown in Figure 5. The input-output characteristic of the comparator shows a hysteresis region of about 150mV (see Figure 6).

The implemented light-load control technique allows bigger voltage ripples at the output compared to the traditional PWM control. The output ripples can be controlled by designing the opening of the comparator's hysteresis. The hysteresis should have a reasonable value for the tolerated output ripples, and to give enough time for the system to go in power-efficient sleep mode. The output voltage and the power transistor driving pulses for two loads are shown in Figure 7 and Figure 8, where it is shown how in light-load the systems stays longer in sleep mode.

The nominal supply voltage of the two converters is 3.6 V and steps-down to 1.2. The two systems operate at the same switching frequency of 150 MHz to allow easy comparison. The same bandgap voltage generator is used as in the PWM controlled system. The fixed duty-cycle generator in the PFM controlled system is realized with a ring oscillator whose power supply is switched off by the sleep mode control signal for minimizing the consumption in light-load conditions.

The buffer for driving the power transistors in the PFM system is shown in Figure 9, and it is based on the topology presented in [5]. The modified buffer incorporates the sleep control signal, which turns off both the NMOS and the PMOS power transistors. The additional functionality is realized with two additional logic components and one transistor, which leads to a very little increase in silicon area. In normal operating mode the buffer generates the gap timings that prevent eventual short circuit losses.

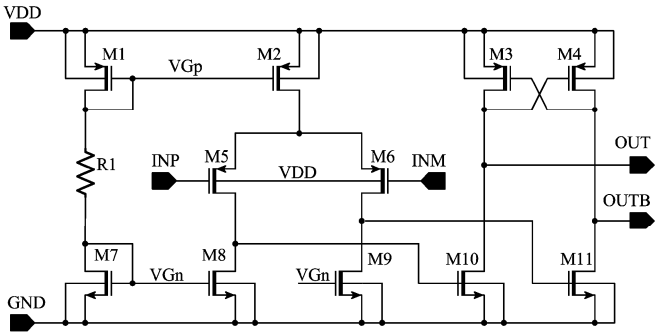

Figure 5. Comparator with hysteresis.

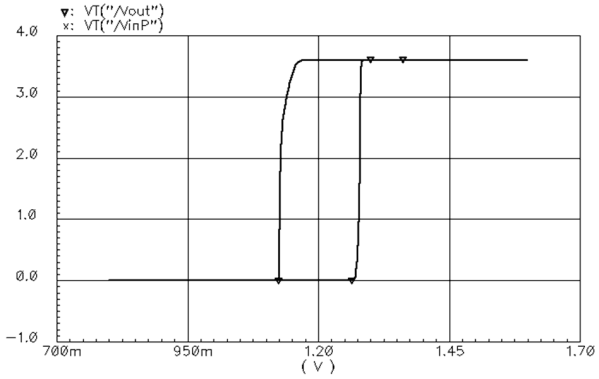

Figure 6. Input-output characteristic of the comparator (V_{INP} is swept, V_{INM}=1.2V).

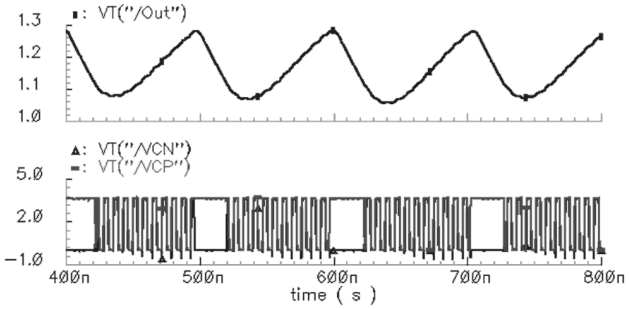

Figure 7. Output voltage and driving pulses for 30Ω load.

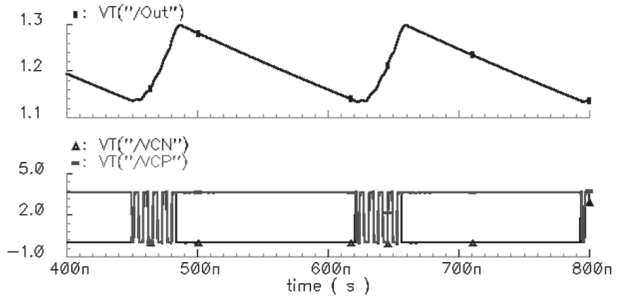

Figure 8. Output voltage and driving pulses for 200Ω load.

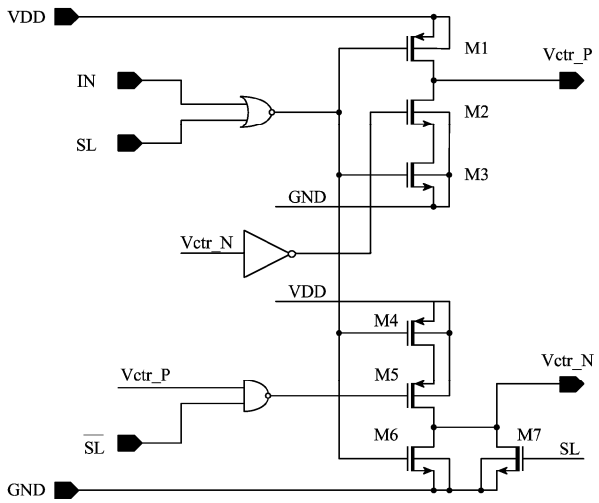

Figure 9. Buffer with dead time interval and sleep control.

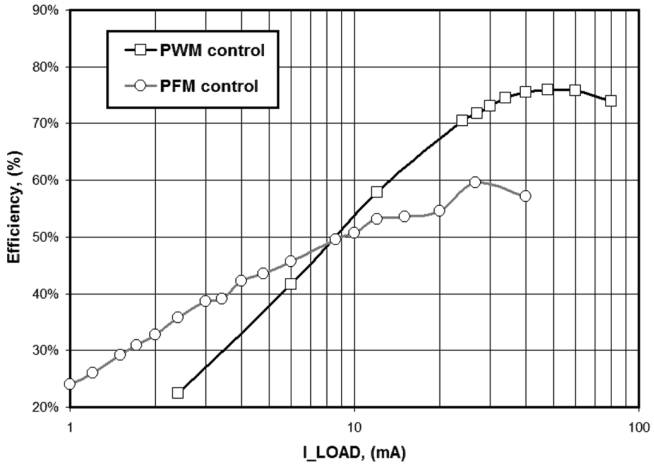

Figure 10. Efficiency comparison between the two controlling methods (PWM and PFM) as a function of the load current

IV. CONVERTER SYSTEM PERFORMANCE

The nominal supply voltage of the converter is 3.6 V and steps-down to 1.2. The blocks of the systems are presented in Section III. The systems operate at a switching frequency *fs* of 150 MHz. A filtering inductor of 250 nH and filtering capacitor of 5 nF are used in the simulations for the two systems.

Figure 8 presents the power efficiency comparison between the PWM controlled converter and the PFM controlled converter as a function of the load current. The PWM system displays better efficiency at high load currents, but it becomes worse at light-load conditions. On the other hand, the PFM performs better at light loads. The PFM system performance at light loads can be improved by minimizing the consumption of the blocks which are continuously operating in sleep mode, namely the bangap generator and the comparator.

The PFM controlled system is not able to regulate the output at large load currents, because of the pulses with fixed duty-cycle generated by the ring oscillator. An optimum DC-DC converter should incorporate both controlling techniques, and this shortcoming is not going to be visible in the final system. The layout topology of the designed PWM monolithic buck converter system is shown in Figure 11.

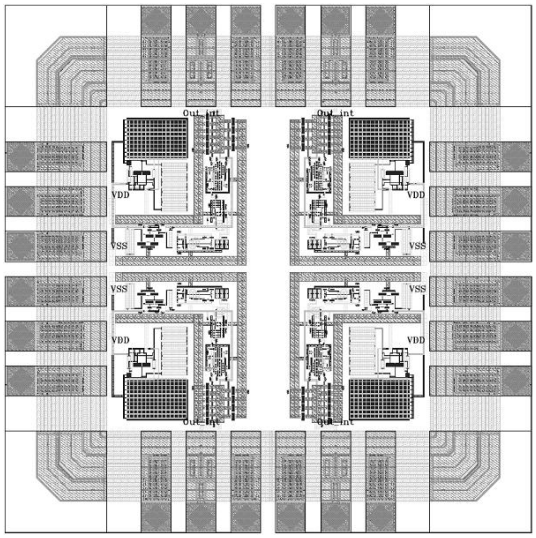

Figure 11. Layout design of the buck converter.

V. CONCLUSION

The performance of a two control loops for switching mode dc-dc converter designed on 0.35-µm CMOS process has been evaluated. The investigation shows that PFM modulation improves the converter efficiency at light loads by allowing bigger output ripples and sleep mode operation. The designed PWM DC-DC converter system achieved 76% efficiency on Cadence simulations at 50mA load current.

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