Buck Converter for Low Power Applications

Tihomir Brusev, Peter Goranov, and Marin Hristov

Abstract — Buck converter for low power applications is designed and investigated on standard 0.35-µm CMOS process. The blocks of the system, including bandgap reference, ramp generator, error amplifier, comparator, buffer and power buck stage, are optimized using CADENCE design tools. The energy losses in the controlling stages are minimized in order to improve the overall converter efficiency η. A relatively high switching frequency of about 147 MHz is used in order to decrease the size of the filtering components. Power efficiency of about 70% is achieved for voltage conversion from 3.6V down to 1.2V. The converter systems shows stable performance over temperature, input voltage, and output load variations.

I. INTRODUCTION

The tendency in microelectronics nowadays is to continuously scale down the standard CMOS process technology, which leads to decreased breakdown voltages. In battery-powered electronic devices, however, the battery voltage remain relatively constant and it should be converted to the desired voltage levels with minimum energy loss. Therefore, step-down voltage conversion is necessary in most of the applications. Switching mode dc-dc (DC-DC) buck converters have potential to achieve higher efficiency η compared to linear regulators [1]. In addition to the high efficiency, another important goal is to decrease the cost and the size of the converter, which requires integration of as many blocks as possible on a single chip.

Implementation of fully-monolithic converters faces mainly technological problems, because of the large value of the passive filter components, which will occupy huge silicon area and it is costly to be integrated on chip [2]. In addition, the available inductors in 0.35-µm CMOS process have low quality factor. A high switching frequency *fs* is a key parameter for decreasing the size, respectively the cost, of the filtering inductor and capacitor. With increasing *fs*, the switching losses in the power transistors become high and they dominate in the circuit, thus the switching frequency is upper bounded from efficiency point of view.

This paper presents a buck converter for low-power applications designed and investigated on 0.35-µm CMOS process. The investigation assumes off-chip filtering components. In Section II are shown the simulation results for the power buck stage. The rest of the building blocks of the converter system, such as bandgap voltage reference, error amplifier, ramp generator, comparator and buffer stages are presented in Section III. The performance of the whole buck converter system is presented in Section IV.

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II. POWER BUCK STAGE EVALUATION

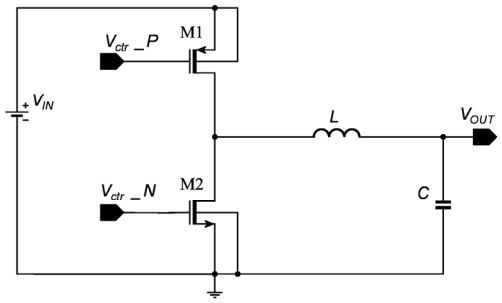

Fig. 1. Synchroneous buck converter schematic.

Fig. 1 shows the circuit of a buck converter implemented on standard CMOS 0.35-µm technology. The NMOS and PMOS transistors, which are forming the power stage, are synchronously controlled in a way that when one of the transistors is switched-on the other is switched-off. In the following, the efficiency performance of the power stage is evaluated assuming ideal drivers with the goal to select an appropriate switching frequency and filtering components.

The most important parameters in the dc-dc buck converters are efficiency, output voltage ripple and inductor current ripple. At high switching frequencies the losses in the transistors are inadmissibly large and the efficiency of the converter decreases. This tendency can be observed from the simulation results given in Table I for four different filtering inductors. The efficiency of the converter can be expressed as:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \qquad (1),$$

where P_{OUT} is the average output power, P_{IN} is the average input power, and P_{LOSS} are all power losses occurring in the power transistors, as well as in the controlling stages. To obtain high converter efficiency, all conversion losses should be kept to a minimum.

The conducting losses in the transistors are proportional to the switching frequency *fs* and the *rms*-value of the current flowing through the device [3]. This relationship is repeated bellow:

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$$P_{MOS} = k_1 i_{rms}^2 + k_2 f_s \quad (2),$$

where k_1 and k_2 is are technology dependent coefficient, which are taking into account the size of the power MOS, as well as the resistive and the capacitive losses associated with the MOS structure. Small inductor ripple current will result in smaller *rms*-value of the current through the MOS structure, and it will respectively lead to better efficiency.

TABLE I
EFFICIENCY AS A FUNCTION OF SWITCHING FREQUENCY F_S

Buck converter	L=10nH	L=50nH	L=250nH	L=300nH
Vout , (V)	1.2	1.2	1.2	1.2
ILoad, (mA)	25	25	25	25
fs, (MHz)	1600	325	147	140
fc, (MHz)	80	35	16	14.5
P_{IN}, (mW)	71.96	39.8	34.5	35
P_{OUT}, (mW)	29.2	29	28.9	28.9
P_{MOS}, (mW)	42	10	5.6	5.4
η=P_{OUT}/P_{IN},(%)	41	72.8	83.7	82.5

In this work, an input voltage of 3.6V is chosen for the converter, since this is the normal voltage for Lithium-Ion battery cell that is typically used in battery-powered devices. The output voltage V_{out} is regulated to 1.2V, which on the other hand is determined by the breakdown voltages of advanced CMOS processes. The inductor *L* and capacitor *C* determine the corner frequency *fc* of the low-pass filter.

The investigations show, that buck converter achieves the best efficiency results when the circuits work at the boundary between continuous and discontinuous conduction mode. At this mode of operation the main transistor *M1* is switching-on at zero current and switching losses are decreasing. In addition, as Table I and (2) suggest, lowering the switching frequency and using larger inductor helps to obtain better efficiency. Therefore, we selected an inductor of 250 nH and 147 MHz frequency for our buck converter system investigation.

III. BUILDING BLOCKS OF THE CONVERTER

A. Bandgap voltage reference

The schematic of the bandgap voltage reference is shown in Fig. 2 [4]. The voltage reference provides a stable voltage for the whole converter system that is independent from the power supply, load current, and temperature variations. The PN-junctions of vertical PNP transistors have been used to extract the temperature information. A lateral PNP transistor, or any other PN junction, can also be used since a speed is not required for the bandgap operation. The line regulation of the output voltage VREF is 12mV/V when power supply voltage is changing from 3V to 4V. Temperature simulation shows that in output voltage stays within 6.5mV range as the temperature varies from -50° up to 70°. The reference voltage generator consumes only 0.27 mA, which helps to improve η.

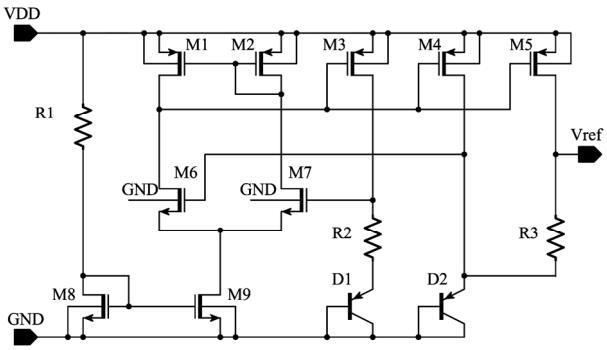

Fig. 2. Bandgap voltage reference.

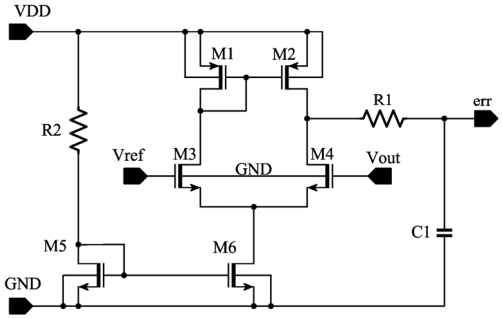

Fig. 3. Schematic of the Error amplifier.

B. Error amplifier

The error amplifier shown in Fig. 3 determines the control voltage, which amplifies the difference between the output voltage V_{out} and the reference voltage V_{ref}. The two amplifier inputs take the signals from the converter output and from the bandgap voltage reference. The error amplifier consists of one differential pair with dynamic load. Any changes of the output voltage will be reflecting to the output DC level of the amplifier. An additional filtering using *R1* and *C1* attenuates the output voltage ripples, and reduce their effect on the performance of the system.

The reference voltage of 1.2V provides enough drain-source voltage for the transistor M6 to keep it always in the saturation region. A high voltage gain is required from the error amplifier in order to improve the regulation by keeping the difference between the output and the reference voltage small. The high voltage gain is achieved by sizing the transistors M3 and M4 for a large gm, whereas a small gm is chosen for M1 and M2. The stage operates with small quiescent current of 97μA for minimum energy losses in the control system.

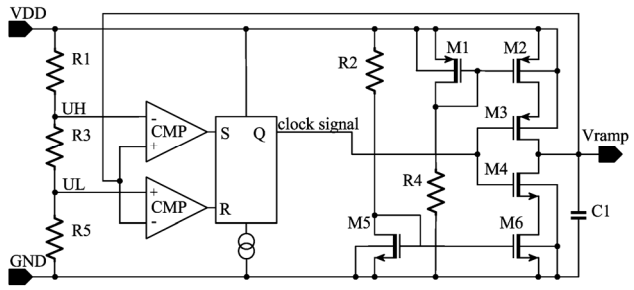

Fig. 4. Ramp generator.

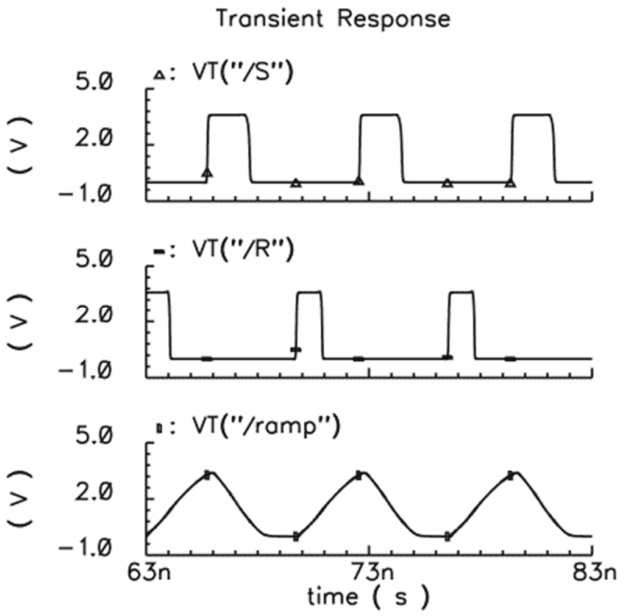

Fig. 5. Voltages of the RS flip-flop inputs and the output of ramp generator.

C. Ramp generator

The ramp generator shown in Fig. 4 determines the switching frequency *fs* of the buck converter. The generator is a part of the regulation system, which performs the Pulse-Width Modulation (PWM) control. The control pulses for the power transistors of the buck converter are generated by comparing the sawtooth signal generated by the ramp generator and the control signal taken out of the error amplifier.

The generator itself consists of two comparators, one RS flip-flop, and one output stage. The sawtooth-like waveform is received over the capacitor *C1*. The two switched current mirrors form the output stage, and they determine the charging and discharging current of *C1*, respectively the slop of the ramp signal. To achieve high switching frequency, either the charging and discharging current should be made big, or the charging capacitor should be small. From efficiency point of view, a relatively small capacitance of 300 fF is used. The capacitance can be made even smaller, but this will make the switching frequency of the converter sensitive to process variations.

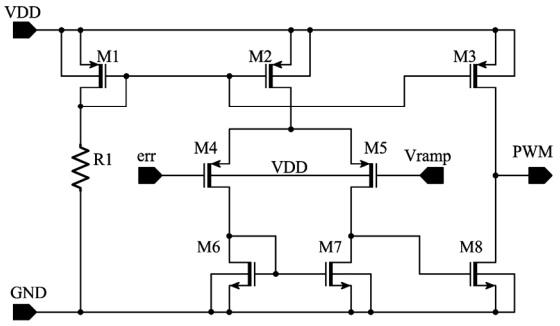

Fig. 6. Comparator.

The switched current mirrors of the output stage are driven by a static RS flip-flop realized with cross-coupled CMOS inverters. The switching current of the RS flip-flop is limited by a current mirror in order to minimize the power losses. The flip-flop is designed for minimum power consumption in order not to deteriorate the efficiency of the converter.

The comparators form the input signal of the RS flip-flop. Their architectures are constructed from differential pairs and buffers. The design is conformable to the technologies limitations of the process used. Fig. 5 shows the simulated waveforms of the RS flip-flop inputs, and the output of the ramp generator.

D. Comparator and buffer

Fig. 6 shows the schematic of the CMOS comparator, which consist of differential pair, a current mirror and an output stage. The comparator is used for creating for the PWM modulation in the feedback control loop of the converter. The comparator inputs are connected to the output of the error amplifier and to the output of the ramp generator. The differential pair is designed to provide high gain. In order to obtain square-wave signals that are driving the power MOS transistors, CMOS inverters are added to the output of the comparator. The inverters are inserted in the buffer stage of the control system. The switching losses coming from the inverters may account for significant losses since on one hand they operate at the converter frequency, and on the other hand they drive the main switching transistors.

The buffer stage shown in Fig. 7 delivers the controlling pulses for the power transistors [5]. The input signal of the buffer is taken from the output of the comparator. In the special case of a simple CMOS inverter is used as a buffer, short circuit energy losses may appear due to simultaneous conduction of the NMOS and PMOS power transistor in Fig. 1. The utilized buffer topology prevents the short-circuit losses by providing a short gap time during which the NMOS and the PMOS transistors are both switched off. Thus, power losses generated due to this phenomenon are avoided.

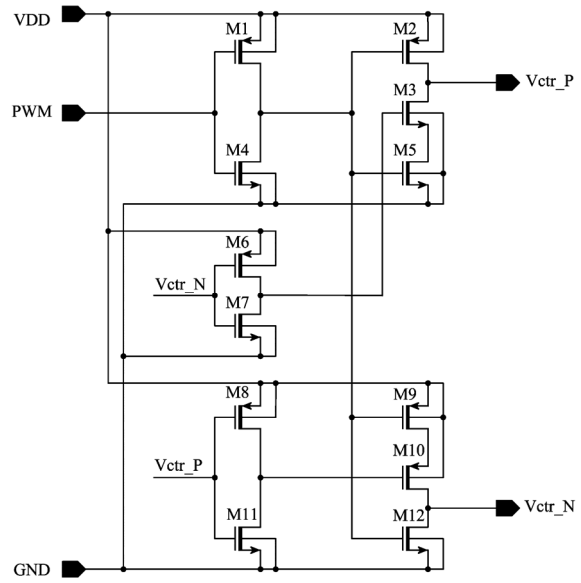

Fig. 7. Electrical schematic of the buffer, which prevents short-circuit losses.

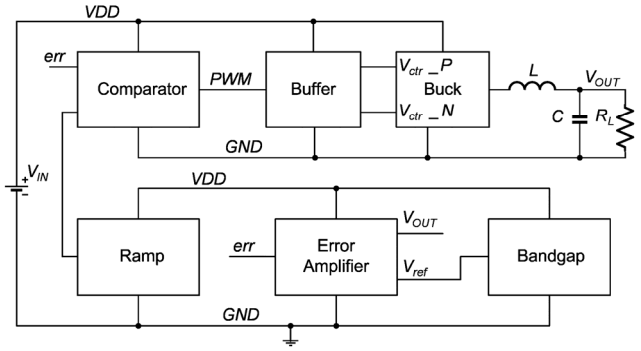

Fig. 8. Block diagram of the buck converter system.

The sizes of the MOS transistors used in the buffer are optimized to satisfy the switching frequency requirements and the requirement for small power consumption of the stage.

IV. Converter System Performance

The block level of the switching-mode DC-DC buck converter system is presented in Fig. 8. The nominal supply voltage is 3.6 V and steps-down to 1.2. The blocks of the systems are presented in Section III. The system operates at switching frequency *fs* of 147 MHz. A filtering inductor of 250 nH and filtering capacitor of 400 pF are used in the simulations.

The characteristics of the output voltage V_{out} and output power P_{out} as a function of load resistor *RL* are illustrated in Fig. 9. The output voltage retains nearly constant level, which shows that system is able to regulate the output voltage to the desire value at various load conditions. The temperature analysis shows only 3mV deviation from nominal output voltage when the temperature varies from -50° up to 70°. The obtained simulated results show that temperature changes in the wide range does not disturb the proper work of the switch-mode dc-dc converter. The simulated efficiency of the designed system with off-chip filter inductor is 70% at 25mA load current.

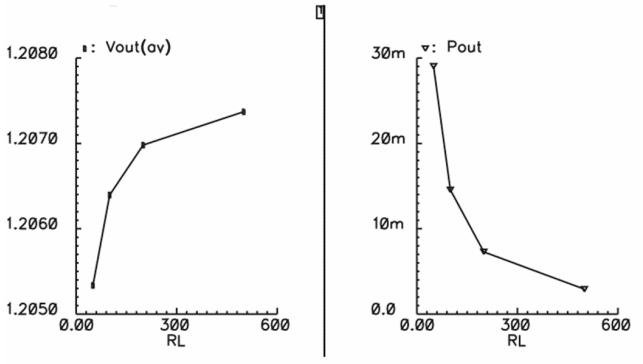

Fig. 9. Simulated load characteristic of the buck converter.

V. Conclusion

The performance of a switch-mode dc-dc converter designed on 0.35-µm CMOS process has been evaluated. The investigation shows that careful optimization is needed for all building blocks of the system, and not only for power stage. When the targets are low-power applications and high integration, then all power losses occurring in the system have to be minimized carefully. Using the available 0.35-µm CMOS technology, the designed DC-DC converter system achieved 70% efficiency on Cadence simulations.

Acknowledgement

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