CAPACITORS DC-DC CONVERTERS FOR RF IMPLEMENTATION

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Two separate capacitor's dc-dc converters for RF implementation are analyzed. The goal of this work is to be skipped the negative effects of the integrated inductors, which can destroy the circuit's parameters. Simulations results demonstrated in this paper were done with AMS CMOS 0.35 µm process. Presented architectures are suitable for low power applications. Silicon area can be saved by use of the investigated capacitor's dc-dc converter and fully monolithic design is possible to be realized.

Keywords: monolithic dc-dc converter, CMOS 0.35 µm technology, efficiency

1. INTRODUCTION

The main goal of this paper is efficiency investigation of dc-dc converter which can be fully implemented on the chip. This task is very important today, because battery powered electronic devises become widespread used. Requirements for energy wasting are strongly. Many efforts are focused to increasing of battery life. Basic switch mode dc-dc converters used huge passive components in the filter to work in proper manner. This imposes inductor to be offchip. Huge inductor spends large silicon area and is not suitable for IC implementation. Other big disadvantage of integrated inductors is their low *Q* factor. The idea of this research is investigation of the dc-dc converter without inductor. Two different architecture are considerate in this paper. They are designed on CMOS AMS 0.35 µm technology. First of all this process was chosen, because of the possibilities for real implementation of IC. The main idea of the investigation of these circuits is to be skipping the inductor. Switched capacitor's circuits are going to save space and from other hand will be solved problem with low *Q* factor. The investigated circuit's architectures are 4T Bridge and Luo switched capacitors dc-dc converters. Received results shows that capacitors dc-dc converters topologies indicates better results compare to the fully monolithic basic switch-mode dc-dc converters.

2. PROBLEM STATEMENT

2.1 4T Bridge dc-dc converter

In Fig. 1 is shown 4T Bridge capacitor dc-dc converter schematic. Four switches in the circuit constitute two different switch pairs. They are respectively *SW1-SW4* and *SW2-SW3*. These couples of switches are controlled synchronously. This method of control is known as PFM (Pulse Frequency Modulation). In Fig. 2 are illustrated control pulses of the switch pairs, which are named $V_{Contrl.\ 1}$ and $V_{Contrl.\ 2}$, respectively for *SW1-SW4* and for *SW2-SW3*.

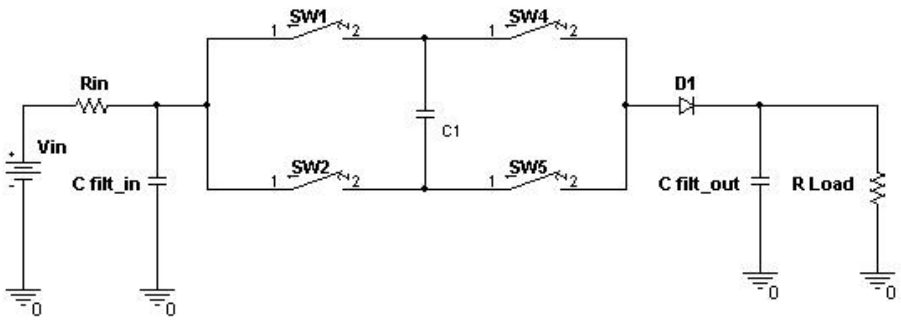

Fig. 1 4T Bridge dc-dc converter.

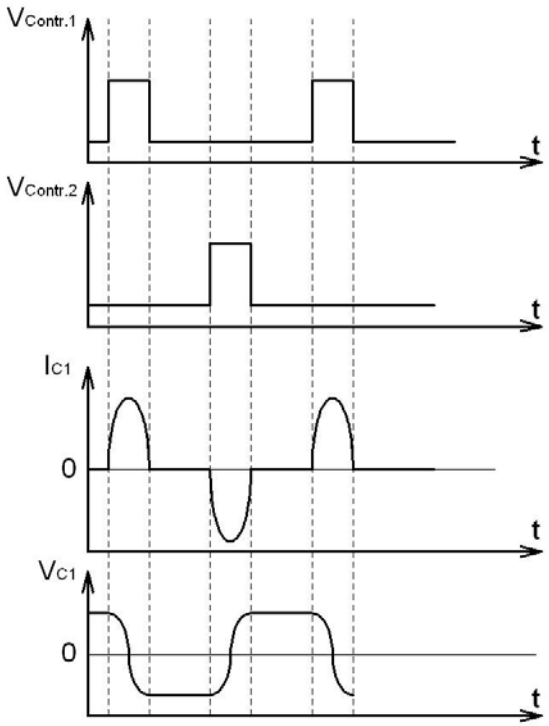

Fig. 2 Control voltages of the two switch pairs; Current through the capacitor (I_{C1}) and voltage across the capacitor (V_{C1}).

In the first half of the period when *SW1-SW4* couple is "on" and *SW2-SW3* is "off" we have the equivalent circuit shown in Fig. 3. The current flows from the input through *SW1*, *C1*, *SW4* and output. If the switches are ideal capacitor *C1* is charged to *Vin* (Fig. 2). In the practice switches are real transistors and the have losses. Actual level of the capacitor's is lower the *Vin*. After the switching "off" of *SW1-SW4*, we have pause and both switching pairs are "off".

Labels in the brackets of Fig. 3 are for the case when *SW2-SW3* is "on" and *SW1-SW4* is "off". The current through capacitor *C1* change his direction when flows form the input through *SW2*, *C1*, *SW3* and output. Nevertheless, that current through the capacitor *C*1 change his polarity, output current retain the same direction. By varying the switching frequency of the switch pairs is regulated the average output voltage.

Capacitors *Cfilt_in* and *Cfilt_out* are filter capacitors, respectively in the input and the output. The role of the input capacitor is to remove ac part of the input signal.

Cfilt_out has to remove the output voltage ripple. In the ideal case both of the capacitors have to be huge. This issue from requirements of dc-dc converter. Output voltage ripple has two time bigger frequency compare to the switching frequency *fs*.

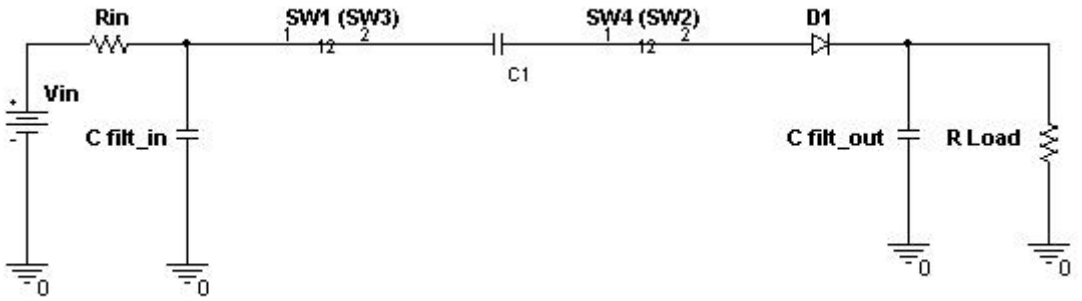

Fig. 3 Equivalent circuit for 4T dc-dc converter.

The efficiency of the converter can express as:

$$\eta = \frac{P_{OUT}}{P_{IN}} \tag{1}$$

where P_{OUT} is output power of the converter,

$$P_{OUT} = \frac{V_{OUT\,(av)}}{R_{Load}{}^{2}} \tag{2}$$

and P_{IN} is input power,

$$P_{IN} = I_{IN\,(av)} \times V_{dd} \tag{3}$$

2.2 Switched capacitor circuit

In Fig. 4 is presented switched capacitors dc-dc converter circuit. This circuit includes only capacitors and switches. Capacitors *C1* and *C2* are equal.

In the first half of the period *SW1*, *SW4* and *SW7* are closed. Other switches are opened. In this case capacitors *C1* and *C2* are charged via the circuit *Vin-SW1-C1-SW4-SW7* and the voltage across them is increasing. The equivalent resistance is equal to the sum of "*ron*" resistance of the opened switches and "*rc*" – equivalent resistance of two capacitors. In second half of the period switches *SW2*, *SW3*, *SW5* and *SW6* are closed. All other switches are opened. In this case capacitor *C1* and *C2* are discharged respectively via *Vout-SW2-C1-SW5* and *Vout-SW3-C2-SW6*. Voltage across the capacitors *C1* and *C2* is decreasing. Capacitors *C1* and *C2* transfer energy form the input to the output. Switched capacitor's circuit illustrated in Fig. 4 can provide to the output average voltage two times smaller then input voltage. This kind of converters could have at the output voltage three, four and so on times smaller then the input voltage.

Capacitors *C1* and *C2* are charged in series during the first half of the period. The input current flows through the capacitors and the charges accumulated on them should be equal. In other hand these capacitors are discharged in parallel during the second half of the period and respectively output current is amplified by two.

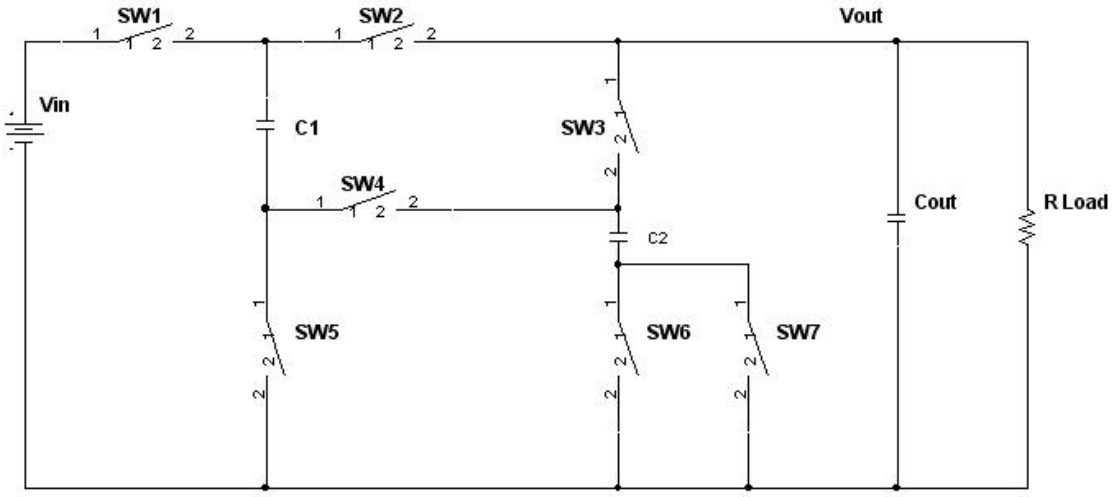

Fig. 4 Switched capacitor dc-dc converter.

3. RESULTS

3.1 4T dc-dc converter

In the Fig. 5 is given the simulated circuit of the 4T dc-dc converter. Circuit is investigated on CMOS 0.35 μm process.

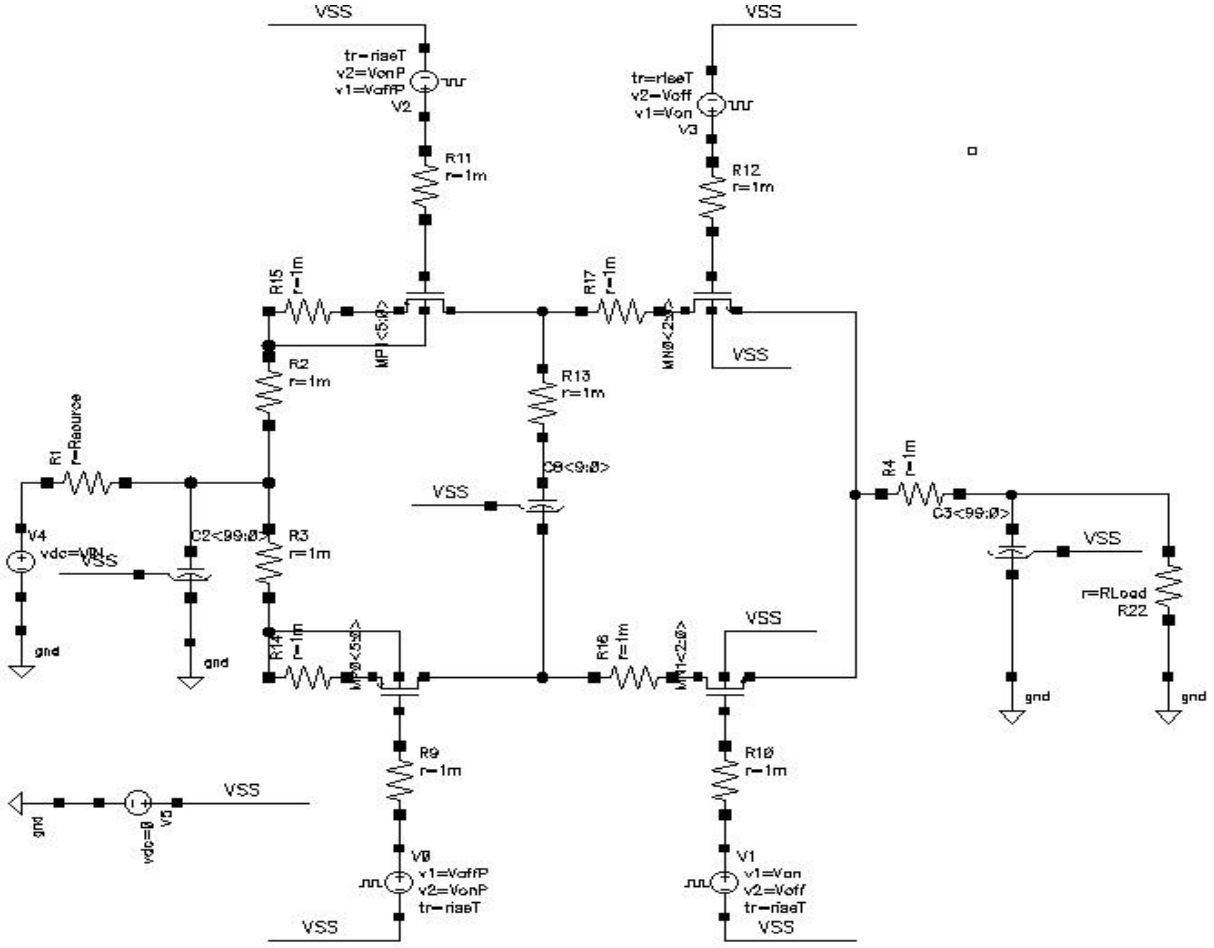

Fig. 5 4T Bridge dc-dc converter schematic simulated on CMOS 0.35 μm process.

In the table bellow are presented received simulations results of the above illustrated circuit. Input voltage *Vin* is equal to 3V and the transistors are regulated in such way, that output voltage *Vout* to be 1.3 V.

Table 1

4T Bridge Converter	C=150 pF	C=300 pF
V_{OUT} (av) [V]	1.3	1.3
I_{Load} (av) [mA]	43.5	44
f_S [MHz]	40	20
P_{IN} [mW]	130.7	133
P_{OUT} [mW]	56.9	59
η [%] (P_{OUT} /P_{IN})	43.6	44.3

3.2 Switched capacitors dc-dc converter.

In the Fig. 6 is given the simulated circuit of the switched capacitors dc-dc converter.

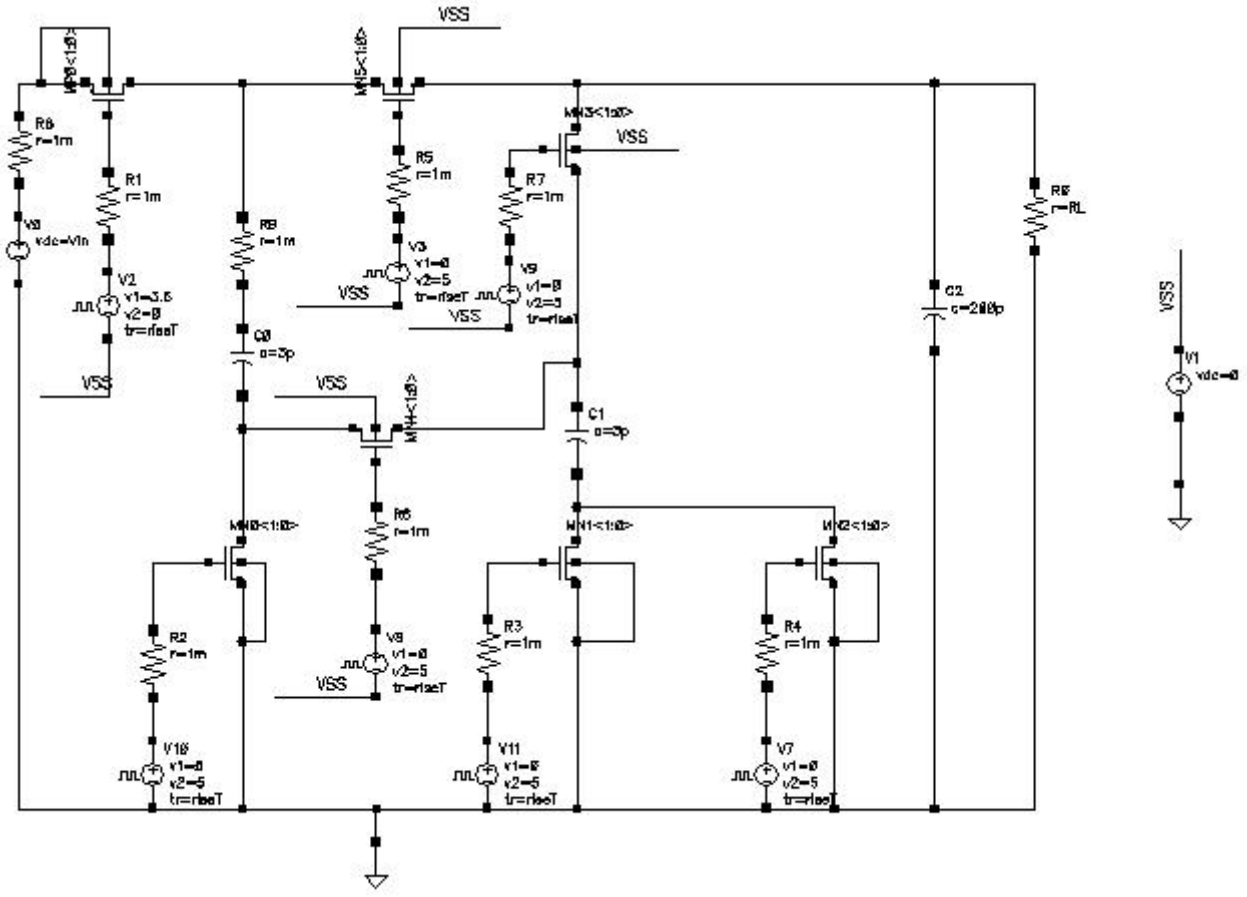

Fig. 6 Efficiency vs. Input Voltage (with ideal inductor) – f=const.

In the table bellow are presented received simulations results of the circuit illustrated in Fig. 6. Input voltage *Vin* is equal to 3.6 V.

Table 2

Switched Capacitor	Ideal Cap	Real Cap
V_{OUT} (av) [V]	1.36	1.33
I_{Load} (av) [mA]	4.86	4.76
f_S [MHz]	1000	1000
P_{IN} [mW]	13.17	14.54
P_{OUT} [mW]	6.6	6.34
η [%] (P_{OUT} /P_{IN})	50	43.6

4. CONCLUSIONS

Two different capacitors dc-dc converters were considerate and analyzed with AMS CMOS 0.35 μm process. From the efficiency point of view the second, switched capacitors structure shows better result. Compare to the first 4T Bridge dc-dc converter, switched capacitors circuit can work at higher switching frequency *fs* – 1 GHz with good efficiency result. These two dc-dc converters give many advantages compare to fully monolithic switch-mode dc-dc converters which used standard integrated inductors. Investigated architectures can save silicon area which can be spend by the inductor without make worse the parameters of the considerate circuits. Area which can be occupied by such kind of converter is approximately 1000x1000 μm or 1 mm^2. The switched capacitors converter can provide to the output only average voltages multiples to the input voltage. This is negative feature, because the control of the output voltage can not be realized.

5. ACKNOWLEDGMENTS

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6. REFERENCES

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