Comparison between routing algorithms applied in NoC architectures for smart Ethernet switches routing schemes

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***Abstract**: In this paper we evaluate different routing algorithms in respect to the average latency, total latency, average throughput, and global throughput. Performance of the Network on Chip (NoC)-based Ethernet smart switches has been rapidly improved and they are required to fulfill some special standards, lowest possible time delay and overall latency, an increased traffic speed through the network switch, and also an increased bandwidth and throughput. We are using Noxim discrete event simulator specialized for NoC architectures simulations. Random selection, buffer level have been used to evaluate the above mentioned parameters. We evaluate NoC model of mesh 8x8 structures which is the most used model nowadays. The state-of-the-art methods for simulation and performance evaluation results of some basic NoC's topologies are also presented here.*

***Keywords:** Ethernet, routing, smart switches, Network on chip, Noxim, throughput, latency.*

1. INTRODUCTION

Evaluation and overview of the basic and most common used topologies of Network on Chip (NoC) with the respective routing algorithms applied on it will be presented in this paper. Evaluation of the basic parameters average latency and average throughput, global average latency, and global average throughput of the NoC will be done using a dedicated simulator for performance evaluation [9]. NoC structures can integrate various Intellectual Properties (IP's) cores on a single silicon chip as shown in Fig.1. A resource could be either a soft processor core, hard coded processor, special Digital Signal Processors (DSP) cores, Field Programmable Gate Array (FPGA) block, or other dedicated unit such as mixed-signals block, or a specific memory block (RAM, ROM, etc)[8]. Fig.1 presents a basic 4X4 NoC topology, where the communication between the participating blocks is performed through the associated router nodes Ri.

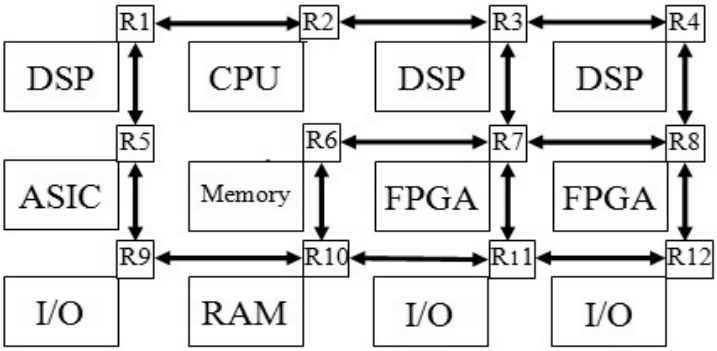

Fig. 1: Basic NoC structure diagram.

EVALUATED ROUTING ALGORITHMS APPLIED IN NOC

Basically, there are three general types of algorithms applied in NoC and they are:

Deterministic routing algorithms

They always generate the same single routing path for a given pair of source and destination address, typically the shortest one. When source routing is used the source node implements pure routing function returning a unique path without consideration any information about the traffic.

Oblivious routing algorithms

This type of algorithms does not take into consideration any other information except the addresses, equally to deterministic routing. The routing decisions are oblivious to the status of network traffic. Any deterministic routing is oblivious, but oblivious routing is not necessarily deterministic [1]. Every time when this algorithm is determining shortest path between source and destination there are two options to select and they are randomly and cyclically. Non deterministic algorithms can distribute uniformly the communication load in situations where adaptive solutions are too expensive or slow.

Adaptive routing algorithms

They use information about network traffic and/or channel status to avoid congested of faulty regions of the network. Source node adaptive routing is useful only when the traffic status does not change too fast, otherwise the source node may have obsolete information and a global status is costly to monitor. On other hand, adaptive routing can easily be combined with distributed routing, since routers can react on local congestions using some heuristics, history tables, or probing the neighborhood. While begin able to avoid deadlocks, adaptive routing must take care of livelocks. Adaptive routing can be decomposed into two functions:

A. Routing function which delivers a set of possible output channels.

B. Output selection function which selects one of free output channels among them using local status information.

Algorithms used for NoC simulations

We will consider and evaluate several routing algorithms that are used in NoC. Deterministic and adaptive algorithms will be evaluated and combination of both deterministic and adaptive algorithm like DyAD is.

Dynamical Adaptive Deterministic routing algorithm

Dynamical Adaptive Deterministic switching [4], shown on Fig.2. Actually, this algorithm is an extension of the Adaptive routing scheme. The adaptive algorithms are working on finding the shortest path.

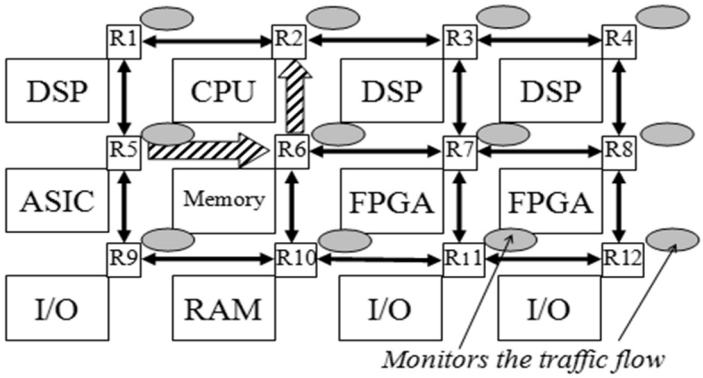

Fig. 2: DyAD routing on Torus NoC topology.

Routers Ri can be generally classified as deterministic and adaptive. In deterministic routing (also called oblivious routing), the path is completely determined by the source and the destination addresses.

On the other hand, a routing technique is called adaptive if, given a source and a destination addresses, the path taken by a particular packet depends on dynamic network conditions e.g. congested links due to traffic variability. The main advantage of using deterministic routing is its simplicity of the routers design. Because of the simplified logic, the deterministic routing provides low latency when the network is not congested. However, as the packet injection rate increases, deterministic routers are likely to suffer from throughput degradation as they can't respond dynamically to the network congestion [8]. In contrast, the adaptive routers avoid congested links by using alternative routing paths which leads to higher throughput. However, due to the extra logic needed to decide on a good routing path, the adaptive routing shows higher latency at low levels of network congestion.

XY routing algorithm

Compared current horizontal address Cx with Dx (when Cx<Dx) routed to EAST, when Cx>Dx and if Cx=Dx, header flit is already horizontally aligned then Dy is compared to Cy [6]. Flit will be routed to South when Cy<Dy, to North when Cy>Dy [10]. If the chosen port is busy, the header flit as well as all subsequent flits of this packet will be blocked [7] – Fig.3. The routing request for this packet will remain active until a connection is established in some future execution of the procedure in this router. However it is deterministic routing algorithm, which means that the routing algorithm provides a routing path for a pair of source and destination. Moreover, XY routing algorithm cannot avoid from deadlock appearance.

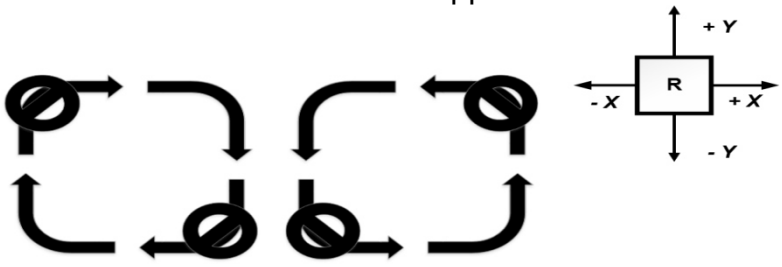

Fig.3: Allowed turns in XY routing algorithm.

Odd-Even routing algorithm (OE)

OE routing algorithm is a distributed adaptive routing algorithm which is based on odd-even turn model. It exerts some restrictions, for avoiding and preventing from deadlock appearance. Odd-even turn model facilitates deadlock-free routing in two-dimensional (2D) meshes with no virtual channels. Explaining some definitions are necessary in order to represent this algorithm. In a two-dimension mesh with dimensions X*Y each node is identified by its coordinate (x, y). In this model, a column is called even if its x dimension element is even numerical column. Also, a column is called odd if its x dimension element is an odd number. A turn involves a 90-degree change of traveling direction. A turn is a 90-degree turn in the following description. There are eight types of turns, according to the traveling directions of the associated channels – Fig.4, Fig.5. A turn is called an ES turn if it involves a change of direction from East to South. Similarly, we can define the other seven types of turns, namely EN, WS, WN, SE, SW, NE, and NW turns, where E, W, S, and N indicate East, West, South, and North, respectively.

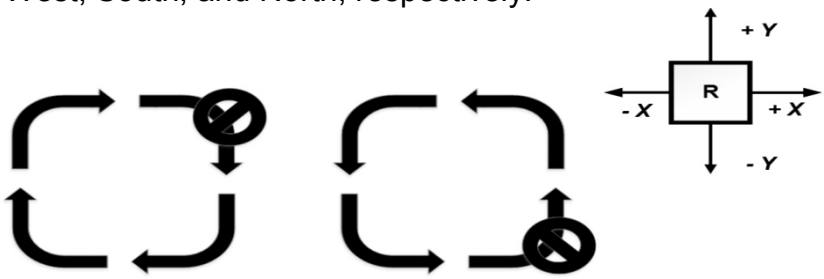

Fig. 4: The allowed turn for Even columns in Odd-even routing.

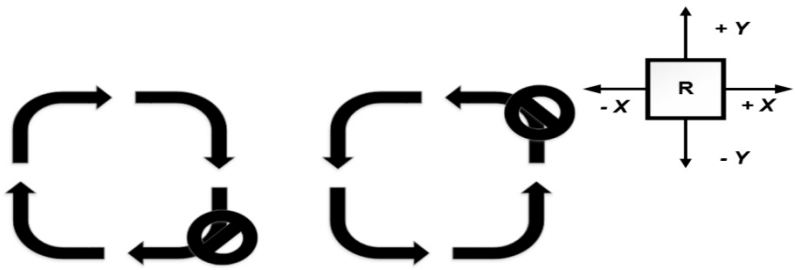

Fig. 5: The allowed turn for Odd columns in Odd-even routing.

As a whole, there are two main theorems in odd-even algorithm: Theorem1: NO packet is permitted to do EN turn in each node which is located on an even column. Also, No packet is permitted to do NW turn in each node that is located on an odd column. Theorem 2: NO packet is permitted to do ES turn in each node that is in an even column. Also, no packet is permitted to do SW turn in each node this is in an odd column. OE routing algorithm is more complex than XY routing algorithm. However, it is one kind of adaptive routing algorithm. For a pair of source and destination, it can provide a group of routing paths and it can prevent from dead lock appearance. That is in an even column. Also, no packet is permitted to do SW turn in each node this is in an odd column. OE routing algorithm is more complex than XY routing algorithm. However, it is one kind of adaptive routing algorithm. For a pair of source and destination, it can provide a group of routing paths and it can prevent from dead lock appearance.

West-First Routing (WF)

The west-first routing is partially adaptive routing algorithm in which 90° turns are allowed [1]. In this routing, the packets have to be moved first in the west direction after first movement in the west direction it can take turns in north, south and east direction respectively. This algorithm posses two options for the path travelled by each packet and that can be minimal or non-minimal. In comparison with XY routing algorithm West-First routing algorithm allows more turns, it allows six turns out of eight turns shown in Fig.6. West-First algorithm has two forbidden turns at any node in a mesh network and they are South to West Turn and North to West turn respectively. Packets cannot take South to West Turn and North to West turn. The West-first algorithm is as follows:

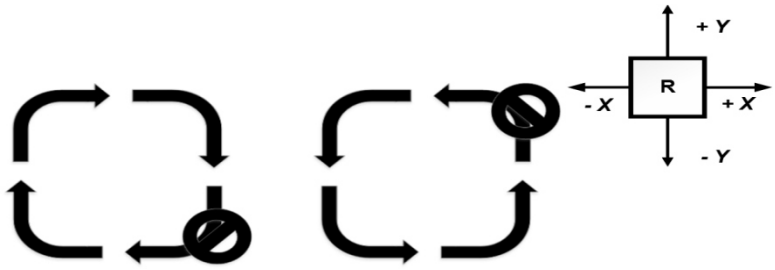

Fig. 6: The allowed turn for West-First routing.

North-Last routing (NL)

North-Last routing algorithm is partially adaptive routing algorithm in which 90° turns are allowed. In this algorithm the packets will be routed in North direction at the last. North-Last routing algorithm allows more turns then XY routing algorithm, it allows six turns out of available eight turns shown in Fig.7. This algorithm allows more turns then XY routing algorithm, it allows six turns out of available eight turns shown in Fig.7. This algorithm has two forbidden turns at any node in a mesh network: North port to West port or North port to East port. In other words, the packets can't take North to West Turn and North to East. In any situation we have to take such path that ends in North directions after transverse in any other directions. The North-last algorithm is as follows:

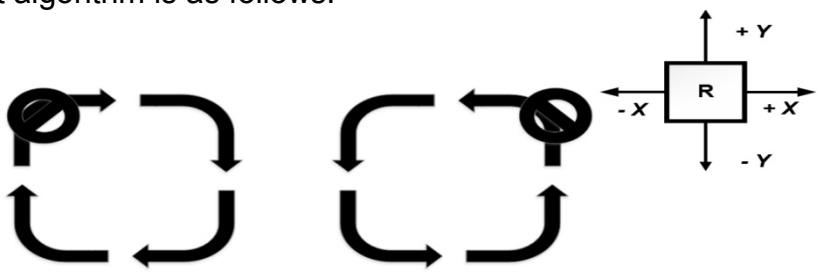

Fig. 7: The allowed turn for North-last routing algorithm.

Negative-First routing (NL)

Negative-First Routing is partially adaptive routing algorithm in which two 90° turn can be avoided [1]. In this routing algorithm the turn towards west (-X) and south (-Y) are taken as negative direction first and the negative path is taken first and then east or north turn are taken respectively to the destination. Negative-First algorithm allows more turns then XY routing algorithm, it allows six turns out of available eight turns

shown on the Fig. 8. This algorithm puts two turn restrictions at any node in a mesh network and combinations East port to South port or North port to West port. Packets can't take East port to South port or North port to the West port.

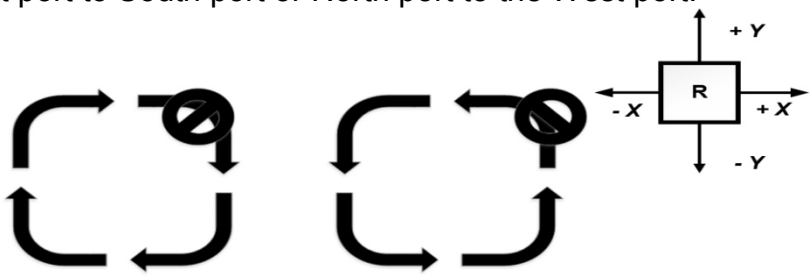

Fig. 8: The allowed turn for Negative-First routing algorithm.

EXPERIMENTAL RESULTS AND DISCUSSION

To evaluate the specific parameters average latency, average throughput and dynamic consumed energy of NoC we are using Noxim simulator.

Evaluation will be made on the most used NoC-Torus topology under different workload, using synthetic workload. Basically in the synthetic traffic, the source and the destination nodes are driven by stochastic bit-complement injection process, and it is important to mention that this intend model the characteristics of realistic workloads.

So, there are different types of synthetic pattern that are used in NoC design includes the following cases about traffic loads:

A. Uniform random traffic in which the source and destination process are chosen via a uniform random process.

B. Bit reversal traffic in this traffic bit reversal permutation is used to solve routing path for the packet along with unique path of length log N.

Simulator scenarios

In this paper we will examine only the most used NoC structure and that is Torus. To conduct our research Noxim simulator was set with the following parameters:

A. Torus k=8 n=2 e.g. 8x8 was evaluated for average throughput and average latency with uniform random traffic under fixed packet size and variable injection rate. XY, Odd-Even, West-First, North-Last, Negative-First routing algorithm and DyAD routing algorithm are used in this case.

Results and discussion

Results from the conducted research: Average latency (cycles) vs Injected packet rate are given in Fig.9 of Torus k=8 n=2 e.g. 8x8 for uniform random traffic and for XY, Odd-Even, West-First, North-Last, Negative-First, and DyAD routing algorithms. Table 1 presents all numeric data from the conducted simulations.

We can also notice that DyAD routing algorithm it has an activation level and will become in adaptive routing mode and respectively his latency will be rapidly increased because he will try to route packets via different paths. If we want to keep routing latency low we should try to avoid greater traffic that threshold activation level

of DyAD routing algorithm and to keep him to work only in deterministic routing e.g. shortest path.

Also we can notice that XY algorithm which is wide used goes in congestion mode and that is visible on the last and highest injected packet rate shown on Fig.9. In that case packet may not reach his destination address.

Conclusions and future work

From the following results we can continue with our research direction to evaluate results from conducted research on some reconfigurable platform and we will try to confirm that XY algorithm is most used in modern NoC.

DyAD routing algorithm is used when there is a need for energy consumption reduction and when flexible routing in needed in respect of the average injection ratio e.g. network load. With comparison of the tested algorithms we can use unmanaged or XY algorithm or DyAD if we want to achieve managed routing in our NoC.

Also deadlock can be noticed from Fig.9 on XY routing algorithm and the injected packet will never reach his destination, XY routing algorithm can't deal with deadlock as well. So our proposal is to use DyAD algorithm to avoid deadlock occurrence.

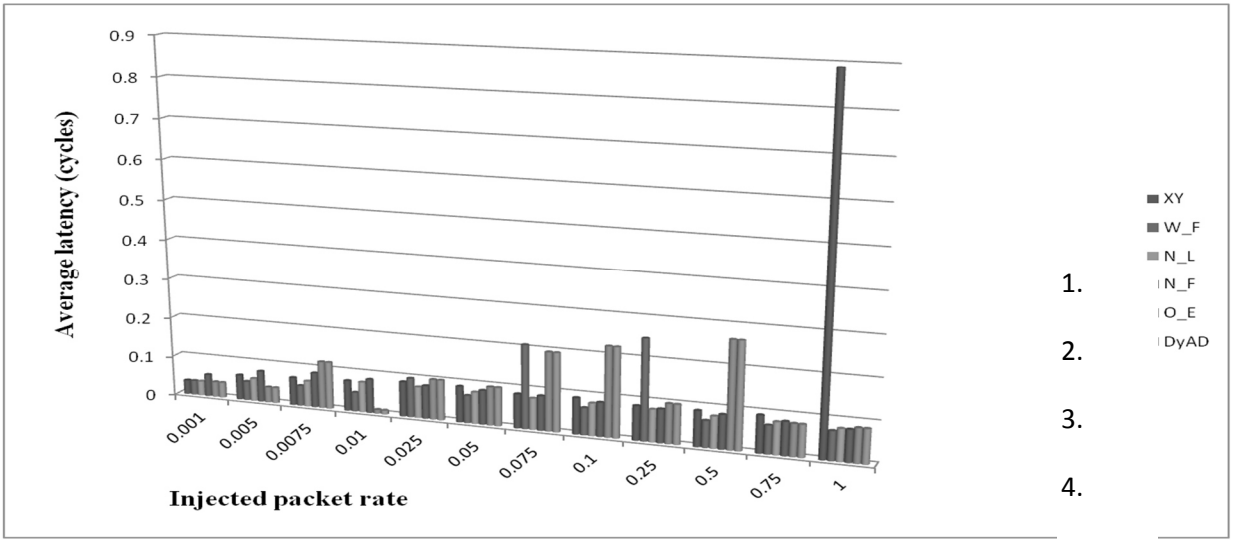

Fig. 9. Experimental results for all routing algorithms under consideration. The average latency for all routing algorithms (1 to 6, from left to right) is shown in groups for different injection packet rates.

Tab.1: NoC parameters under different Injection ratio.

ROUTING ALGORITHM	BUFFER DEPTH	FLIT SIZE	INJECTION RATE	TOTAL RECEIVED PACKETS	TOTAL RECEIVED FLITS	GLOBAL AVERAGE DELAY (CYCLES)	GLOBAL AVERAGE THROUGHPUT (FLITS/CYCLE)	AVERAGE TROUGHPUT (FLITS/CYCLE/IP)	MAX DELAY (CYCLES)	TOTAL ENERY (J)	DYNAMIC ENERGY (J)	STATIC ENERGY (J)
TRAFFIC BIT REVERSAL Routing XY_8_64bit	4	32	0.001	23855	855999	1042.33	0.0354	0.0351	67612	3.71E-04	3.34E-05	3.38E-04
	4	32	0.005	33325	1199823	15899.4	0.06197	0.0622	98847	3.73E-04	3.56E-05	3.38E-04
	4	32	0.0075	36368	1316319	18900	0.0692	0.0696	98629	3.72E-04	3.40E-05	3.38E-04
	4	32	0.01	40291	1444958	19761	0.0753	0.0756	98731	3.73E-04	3.67E-05	3.38E-04
	4	32	0.025	45757	1644051	34460.8	0.0866	0.0869	99163	3.72E-04	3.43E-05	3.38E-04
	4	32	0.05	46218	1663529	43145.2	0.0891	0.0897	99818	3.73E-04	3.54E-05	3.38E-04
	4	32	0.075	45922	1653947	46380.9	0.0843	0.0849	99938	3.73E-04	3.53E-05	3.38E-04
	4	32	0.1	47189	1702186	47524.2	0.0894	0.09	99708	3.75E-04	3.71E-05	3.38E-04
	4	32	0.25	46557	1672806	50247	0.0851	0.085	99869	3.73E-04	3.55E-05	3.38E-04
	4	32	0.5	47857	1718470	51227.1	0.0876	0.0882	99789	3.73E-04	3.56E-05	3.38E-04
	4	32	0.75	48154	1725726	51342.5	0.0916	0.0922	99872	3.73E-04	3.55E-05	3.38E-04
	4	32	1	48042	1733840	51761.9	0.0887	0.89	99918	3.74E-04	3.65E-05	3.38E-04
TRAFFIC BIT REVERSAL WEST_FIRST_8_64	4	32	0.001	24087	870622	1134.96	0.0357	0.0357	68249	3.70E-05	3.33E-05	3.38E-04
	4	32	0.005	28004	1010984	14533.8	0.0484	0.0475	98253	3.65E-05	2.76E-05	3.38E-04
	4	32	0.0075	28729	1032186	12119.3	0.0586	0.05077	97566	3.62E-05	2.38E-05	3.38E-04
	4	32	0.01	26243	951942	26243	0.0652	0.0477	98141	3.57E-05	1.89E-05	3.38E-04
	4	32	0.025	36610	1317879	29688	0.117	0.0976	99441	3.60E-05	2.22E-05	3.38E-04
	4	32	0.05	39339	1412716	42437	0.0681	0.0685	99835	3.64E-05	2.63E-05	3.38E-04
	4	32	0.075	34694	1245637	44065.3	0.209	0.208	99468	3.59E-05	2.08E-05	3.38E-04
	4	32	0.1	36105	1296421	47820	0.0671	0.0672	99675	3.60E-04	2.24E-05	3.38E-04
	4	32	0.25	35728	1285374	49584.9	0.248	0.25	99660	3.60E-04	2.24E-05	3.38E-04
	4	32	0.5	36182	1297396	48981.2	0.0819	0.066	99798	3.61E-04	2.33E-05	3.38E-04
	4	32	0.75	35210	1264481	50074.6	0.0809	0.07	99772	3.59E-04	2.11E-05	3.38E-04
	4	32	1	39195	1413587	50333.4	0.0796	0.072	99802	3.64E-04	2.66E-05	3.38E-04
TRAFFIC BIT REVERSAL NORTH_LAST_8_64bit	4	32	0.001	24487	878691	272.766	0.0361	0.0361	28590	3.72E-04	3.41E-05	3.38E-04
	4	32	0.005	36178	1296164	17708.8	0.0573	0.057	97596	3.75E-04	3.71E-05	3.38E-04
	4	32	0.0075	40238	1445466	21937.4	0.0646	0.0642	99526	3.76E-04	3.87E-05	3.38E-04
	4	32	0.01	42285	1521317	19951.4	0.0809	0.0755	97899	3.75E-04	3.78E-05	3.38E-04
	4	32	0.025	49513	1780033	34937.6	0.0786	0.0777	98437	3.77E-04	3.88E-05	3.38E-04
	4	32	0.05	50346	1806753	44040.8	0.0792	0.0789	99523	3.77E-04	3.94E-05	3.38E-04
	4	32	0.075	49348	1781565	46980	0.0786	0.0781	99787	3.77E-04	3.88E-05	3.38E-04
	4	32	0.1	50969	1840509	48455.4	0.0806	0.0807	99652	3.77E-04	3.97E-05	3.38E-04
	4	32	0.25	49028	1761743	48658.8	0.081	0.0802	99760	3.76E-04	3.83E-06	3.38E-04
	4	32	0.5	50396	1810296	49835.3	0.0795	0.0787	99643	3.76E-04	3.86E-05	3.38E-04
	4	32	0.75	51346	1853511	51730.6	0.0799	0.0799	99866	3.76E-04	3.86E-05	3.38E-04
	4	32	1	50591	1822986	52024.6	0.0794	0.0792	99889	3.76E-04	3.86E-05	3.38E-04
TRAFFIC BIT REVERSAL NEGATIVE_FIRST_8_64bit	4	32	0.001	37122	1337578	5324.14	0.055	0.0552	95840	3.87E-04	4.96E-05	3.38E-04
	4	32	0.005	52033	1874537	20971.8	0.814	0.0776	99262	3.85E-04	4.76E-05	3.38E-04
	4	32	0.0075	57862	2084276	25237	0.0906	0.087	98611	3.86E-04	4.85E-05	3.38E-04
	4	32	0.01	56029	2018116	30552.4	0.0874	0.0846	98371	3.84E-04	4.67E-05	3.38E-04
	4	32	0.025	55087	1980500	42548.1	0.0892	0.0825	99678	3.82E-04	4.45E-05	3.38E-04
	4	32	0.05	56735	2046609	46251.1	0.0913	0.0851	99623	3.84E-04	4.66E-05	3.38E-04
	4	32	0.075	57129	2051198	47499.7	0.0937	0.086	99832	3.84E-04	4.77E-05	3.38E-04
	4	32	0.1	56060	2019135	48402.7	0.0914	0.0843	99613	3.83E-04	4.51E-05	3.38E-04
	4	32	0.25	55672	1999820	50348.8	0.0879	0.083	99873	3.84E-04	4.58E-05	3.38E-04
	4	32	0.5	56731	2040691	51071.5	0.088	0.0845	99882	3.84E-04	4.67E-05	3.38E-04
	4	32	0.75	55179	1986943	51928.8	0.0845	0.0829	99786	3.83E-04	4.55E-05	3.38E-04
	4	32	1	52707	1895912	49868.1	0.0861	0.0791	99794	3.80E-04	4.20E-05	3.38E-04
TRAFFIC BIT REVERSAL ODD_EVEN_8_64bit	4	32	0.001	25743	927408	2520.74	0.038	0.0381	46575	3.64E-04	3.64E-05	3.38E-04
	4	32	0.005	20057	723270	10888.7	0.455	0.0386	97623	3.86E-04	1.79E-05	3.38E-04
	4	32	0.0075	23552	847861	7803.02	0.1262	0.1174	97539	3.55E-04	1.71E-05	3.38E-04
	4	32	0.01	26849	967586	29480.28	0.0945	0.00951	99181	3.55E-04	1.74E-05	3.38E-04
	4	32	0.025	35072	1255564	31352.3	0.1198	0.1	99018	3.59E-04	2.12E-05	3.38E-04
	4	32	0.05	33844	1218785	41694	0.0962	0.0957	99934	3.57E-04	1.95E-05	3.38E-04
	4	32	0.075	33061	1189027	44527.7	0.1969	0.1955	99218	3.54E-04	2.01E-05	3.38E-04
	4	32	0.1	30692	1103808	46220.5	0.227	0.223	99142	3.54E-04	1.60E-05	3.38E-04
	4	32	0.25	35890	1289602	50796.2	0.103	0.098	99650	3.56E-04	2.16E-05	3.38E-04
	4	32	0.5	33621	1212370	50737	0.286	0.265	99717	3.56E-04	1.85E-05	3.38E-04
	4	32	0.75	37169	1344393	52443.4	0.0826	0.0799	99817	3.61E-04	2.29E-05	3.38E-04
	4	32	1	37718	1361217	51667.3	0.0104	0.085	99732	3.61E-04	2.27E-05	3.38E-04
TRAFFIC BIT REVERSAL Routing DYAD_8_64 bit	4	32	0.001	2221	4441	23.56	0.0019	0.0019	65	6.66E-05	3.61E-06	6.62E-05
	4	32	0.005	20057	40102	23.59	0.0029	0.0029	73	3.86E-05	3.65E-06	3.38E-05
	4	32	0.0075	21552	41247	23.63	0.0035	0.0035	78	4.82E-05	3.68E-06	3.38E-05
	4	32	0.01	22952	45908	24.948	0.018	0.019	82	6.99E-05	3.73E-06	6.62E-05
	4	32	0.025	50589	101176	186.133	0.03	0.04	9181	7.39E-05	7.65E-06	6.62E-05
	4	32	0.05	64858	129715	368.165	0.06	0.06	9487	7.45E-05	8.25E-05	6.62E-05
	4	32	0.075	71706	143410	571.775	0.08	0.09	9631	7.47E-05	8.52E-06	6.62E-05
	4	32	0.1	76743	153483	624.802	0.12	0.13	9354	7.48E-05	8.65E-06	6.62E-05
	4	32	0.25	95619	191236	1398.88	0.23	0.26	6147	7.50E-05	8.82E-06	6.62E-05
	4	32	0.5	103500	207000	2636.93	0.25	0.28	7623	7.54E-05	9.18E-06	6.62E-05
	4	32	0.75	103500	207000	3255.41	0.26	0.29	8120	7.55E-05	9.25E-06	6.62E-05
	4	32	1	103500	207000	3573.28	0.26	0.29	8371	7.54E-05	9.24E-06	6.62E-05

REFERENCES

[1.] Dally W, Towles B. Route packets, not wires: on-chip interconnection networks. Proceedings of the design automation conference, 2001, pp 684-689.

[2.] Dally WJ. 2004 Principles and practices of interconnection networks. San Francisco, USA, Morgan Kaufmann.

[3.] Guerrier P, Greiner A. A generic architecture for on-chip packet-switched interconnections. Proceeding of the design, automation and test in Europe conference and exhibition, 2000, pp 250–256.

[4.] Jingcao Hu; Marculescu, R. "DyAD – Smart Routing for Network-on-Chip", *Proceedings of the 41st annual Design Automation Conference*, June 07-11, 2004, pp.260 -263.

[5.] S. Kumar, A. Jantsch, et al, A Network on Chip Architecture and Design Methodology. Proceedings of the IEEE Computer Society Annual Symposium on VLSI, 2002, pp.105-112.

[6.] Parag Parandkar, Jayesh Kumar Dalal and Sumant Katiyal, Performance Comparison of XY, OE and DY Ad Routing Algorithm by Load Variation Analysis of 2-Dimensional Mesh Topology Based Network-on-Chip, BIJIT - BVICAM's International Journal of Information Technology, 2012, pp.391-396.

[7.] Marculescu R, Jingcao H, Ogras UY. Key research problems in NoC design: a holistic perspective. Proceedings of the 3rd IEEE/ACM/IFIP international conference on hardware/software codesign and system synthesis, 2005, pp.69-74.

[8.] I Saastamoinen, et al, Interconnect IP Node for Future System-on-Chip Designs, Proceedings of the First IEEE Int. Workshop on Electronic Design, Test and Applications, 2002, pp.116-120.

[9.] D. Sylvester and K. Keutzer, Getting to the Bottom of Deep Submicron, Proceedings of the Int. Conference on Computer-Aided Design, 1998, pp.203-211.

[10.] Bhupendra Kumar Soni and Dr.Girish Parmar, Analysis of Different Routing Algorithm for 2D-Torus Topology NoC Architecture under Load Variation, International Journal of Advanced Engineering Research and Science (IJAERS), 2016, pp.250-255.