Investigation of Power Losses in Synchronous Buck DC-DC Converter with Zero Voltage Switching

Elitsa Emilova Gieva, Tihomir Sashev Brusev, George Vasilev Angelov,
Rostislav Pavlov Rusev and Marin Hristov Hristov
Department of Microelectronics, Faculty of Electronic Engineering and Technologies,
Department of Technology and Management of Communication Systems, Faculty of Telecommunications
Technical University of Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria
gieva@ecad.tu-sofia.bg, brusev@ecad.tu-sofia.bg, angelov@ecad.tu-sofia.bg, rusev@ecad.tu-sofia.bg,mhristov@ecad.tu-sofia.bg

Abstract – **In this paper a synchronous buck dc-dc converter with Zero Voltage Switching (ZVS) for low power applications is presented and investigated in Cadence with a CMOS 0.35 μm technology. Power losses in the converter's components are evaluated and analyzed. The results obtained show that the efficiency of the standard switching-mode buck dc-dc converter can be increased by about 3.6 % if ZVS technique is used.**

Keywords – **Power losses, synchronous buck dc-dc converter, zero voltage switching, Cadence.**

I. Introduction

Switching-mode dc-dc converters are part of envelope amplifiers, which are used to deliver the desired energy to the transmitter's power amplifier (PA) in modern battery powered wireless communication devices [1]. The last generation mobile phones have great functionality, because the signal spectrum is used very effectively [2]. The reason is that orthogonal frequency division multiplexing (OFDM) modulation is performed. The information is transferred using several sub-carrier frequencies. The output signal has big variation of the amplitude. Therefore, in order to prevent distortion of the transmitted information, the power amplifier should be linear. The disadvantage of linear PAs is that those circuits have low efficiency performance.

One of the problems of modern smart phones is that battery has to be recharged more often. The battery energy can be saved if efficiency of envelope amplifier is increased. The function of envelope amplifiers is to supply dynamically changeable voltage to drain or collector of PA's RF transistor as a function of envelope signal [3]. The switching-mode buck dc-dc converters are usually used when low frequency and dc voltages have to be delivered to PAs. The rest of the power is supplied by fast tracking speed linear amplifiers. Both linear amplifier and switching-mode converter stages can operate in different hybrid envelope amplifier architectures [2].

Switching-mode converters ensured almost 80% of overall transmitter's PA energy [3]. The efficiency of envelope amplifier is calculated by:

$$\eta_{EA} = \frac{P_{out(av)}}{P_{in(av)}}, \tag{1}$$

where η_{EA} – efficiency of the envelope amplifier, $P_{out(av)}$ – average output power, $P_{in(av)}$ is the average input power.

The power losses in the MOS transistors of synchronous buck dc-dc converter are discussed in Section II *A*. In Section II *B* power losses in the low-pass filter of the converter are considered. The effect of zero voltage switching (ZVS) technique on the switching power losses in the main PMOS transistors is described in Section II *C*. Investigation results of power losses and efficiency of the buck dc-dc converter with ZVS are presented in Section III.

II. Power Losses in the Switching-Mode Buck DC-DC Converter

A. Power losses in the MOS transistors of buck dc-dc converter

The schematic of synchronous buck dc-dc converter is shown in Fig. 1.

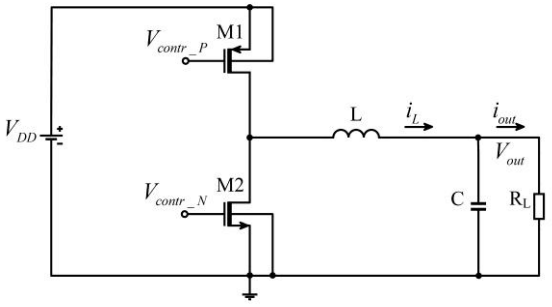

Fig. 1. Synchronous buck dc-dc converter.

The efficiency of the whole buck converter system can be expressed by:

$$\eta = \frac{P_{out}}{P_{out} + P_{losses}}, \tag{2}$$

where P_{out} is the output power of the dc-dc converter; P_{losses} are total power losses in the dc-dc buck converter. Most of the power losses in the converter are indicated in the output MOS transistors *M1* and *M2*. Those losses can be divided into conduction and switching power losses [4]:

$$P_{loss,MOS} = P_{sw} + P_{cond}. \tag{3}$$

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On the other hand, the switching power losses in the output MOS transistors *M1* and *M2* are equal to [2]:

$$P_{sw} = f_s . C_{tot} . V_{DD}^2, \quad (4)$$

where C_{tot} is the output total capacitance of the MOS transistors, f_s is the switching frequency of the buck converter, V_{DD} is the power supply. The conduction losses can be calculated by [4]:

$$P_{cond} = I_{source}^2 . r_{on,p} + I_{sink}^2 . r_{on,n}, \quad (5)$$

where I_{source} and I_{sink} are the sourcing and sinking current of the MOS transistor respectively, while $r_{on,p}$ and $r_{on,n}$ are the on-resistances of PMOS and NMOS transistors.

B. Power losses in the low-pass filter of buck dc-dc converter

The other distributor of losses in the buck dc-dc converter is the filter inductor *L*. The total power dissipated in filter inductor, assuming that the inductor parasitic impedance scale linearly with the inductance [5], is equal to:

$$P_{ind} = b\left[\frac{I^2}{\Delta i_L f_s} + \frac{\Delta i_L}{3 f_s} + \frac{C_{L0} V_{DD}^2}{R_{L0} \Delta i_L}\right], \quad (6)$$

where *b* is a coefficient depending from the parasitic capacitance and parasitic series resistance of the filter inductor, C_{L0} and R_{L0} are respectively the parasitic stray capacitance and parasitic series resistance per 1 nH inductance, Δi_L is the inductor current ripple.

The other source of the power losses in the switching-mode buck dc-dc is filter capacitor *C*. They are obtained due to the effective series resistance of the capacitance R_C. If monolithic capacitor is implemented utilizing the gate oxide capacitance of a MOSFET transistor, the total power dissipation of filter capacitor [5] is equal to:

$$P_{cap} = d \cdot f_s \cdot \Delta i_L, \quad (7)$$

where *d* is a coefficient depending on technology, effective series resistance of the filter capacitor for MOSFET transistor with channel width of 1 μm, gate oxide capacitance, channel length of the MOSFET transistor.

C. Zero Voltage Switching

The circuit of synchronous single phase switching-mode buck dc-dc converter with ZVS is shown in Fig. 2. The advantage of those type of circuits is that the main power transistor *M1* can be switched on and off respectively at zero voltage [6].

The zero voltage switch-off of the main PMOS transistor *M1* of dc-dc converter is because of the capacitor C_r. The Zero voltage switching-on state of the PMOS transistor *M1* is ensured by the diode D_r.

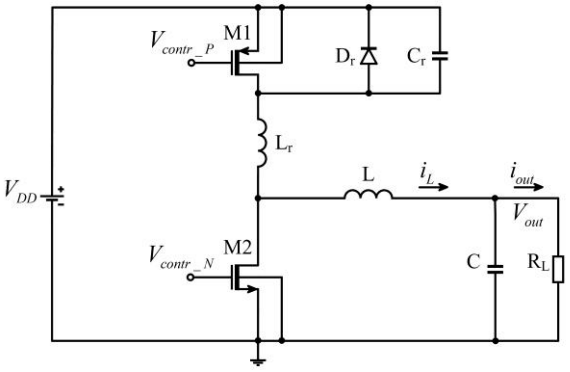

Fig. 2. Synchronous buck dc-dc converter with ZVS.

The function of this component is to clamp to zero capacitor voltage V_c, when transistor *M1* is at switch-off state [6]. The effect of ZVS will leads to zero switching power losses of main PMOS transistor *M1*. Thus the total power losses in the MOS transistors of synchronous dc-dc converter could be decreased. They are equal to [5]:

$$P_{tot,MOS} = a\sqrt{\left(I^2 + \frac{\Delta i_L^2}{3}\right) f_s}, \quad (8)$$

where Δi_L is the inductor current ripple, *I* is a dc current supplied to the load, and *a* is a coefficient depending on the equivalent series resistance of the transistors, the input total capacitance of the MOS transistors C_{tot}, and the power supply V_{DD}.

III. INVESTIGATION OF POWER LOSSES AND EFFICIENCY OF BUCK CONVERTER WITH ZVS

Synchronous buck dc-dc converter with Zero Voltage Switching is investigated in Cadence with a CMOS 0.35 μm technology.

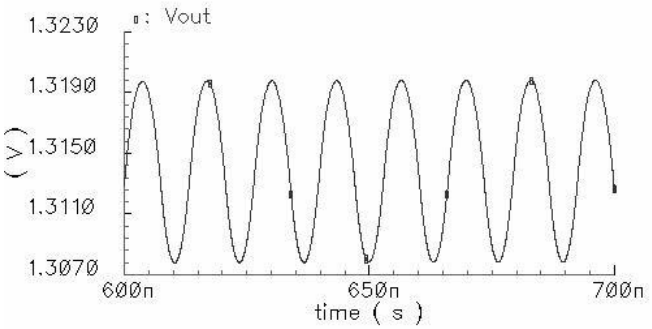

Fig. 3. The output voltage V_{out} of buck dc-dc converter with ZVS.

The supply voltage V_{DD} is chosen to be equal to 3.6 V, which is the standard output voltage of lithium-ion batteries. The main power PMOS transistor *M*1 is formed by four "*modprf*" transistors connected in parallel. Their sizes (W/L) respectively are equal to 150/0.35 μm. The NMOS transistor *M*2, which replaces the diode in the standard buck dc-dc converter circuit, is formed by two "*modnrf*" transistors connected in parallel. Their sizes

(W/L) respectively are equal to 150/0.35 μm. The mode of operation of transistors *M1* and *M2* is regulated by two pulse generators V_{contr_P} and V_{contr_N} , respectively. The value of the filter inductor of the investigated circuit is equal to 300 nH. The filter capacitor is equal to 5 nF. The value of resonant inductors L_r is equal to 30 nH, while resonant capacitor C_r is equal to 5 pF. The switching frequency *fs* of the investigated buck dc-dc converter with ZVS is equal to 76 MHz.

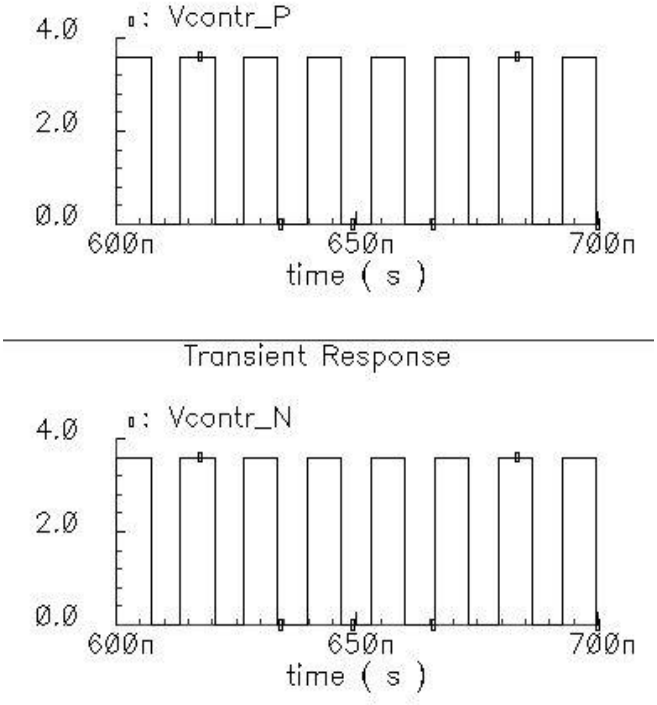

Fig. 4. The waveforms of V_{contr_P} and V_{contr_N}.

The average value of output voltage $V_{out(av)}$of buck dc-dc converter with ZVS is regulated to be equal to 1.3 V. The waveform of output voltage V_{out} is shown in Fig. 3. The waveforms of control pulses V_{contr_P} and V_{contr_N}, which regulate respectively transistors *M*1 and *M*2, are shown in Fig. 4.

TABLE 1. POWER LOSSES IN FILTER INDUCTOR *L* AND FILTER CAPACITOR *C* OF DC-DC CONVERTER WITH ZVS AS A FUNCTION OF THE LOAD R_L

	R_L=10 [Ω]	R_L=15 [Ω]	R_L=20 [Ω]	R_L=30 [Ω]	R_L=48 [Ω]
P_{out} [mW]	116.9	112.65	84.5	56.3	35.2
P_{ind} [mW]	3.4	3.1	2.8	2.1	1.9
P_{cap} [mW]	0.24	0.21	0.19	0.11	0.06

The power losses in filter inductor *L* and filter capacitor *C* of the buck dc-dc converter with ZVS are investigated. The average value of output voltage $V_{out(av)}$ is equal to 1.3 V. The results are shown in Table 1. The waveform of control signal V_{contr_P}, which determine the mode operation of PMOS transistor *M*1, and voltage and the capacitor's voltage V_{Cr} are shown in Fig. 5. As can be seen from the picture, the PMOS transistor is switching on at zero voltage, while *M*1 is switching-off at voltage higher than zero. The reason is the fact that *M*1 is non-ideal switch.

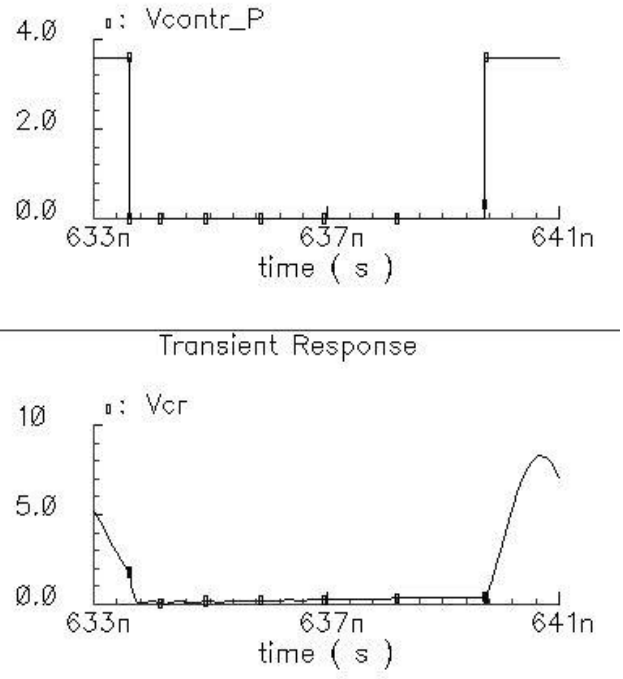

Fig.5. The waveforms of V_{contr_P} the capacitor's voltage V_{Cr} .

The total power losses in PMOS and NMOS transistors and the efficiency of the buck dc-dc converter with ZVS as a function of the load R_L are investigated. The results are shown in Table 2. The results presented in Table 1 and Table 2 show that power losses in the MOS transistors dominate in buck dc-dc converter.

TABLE 2. POWER LOSSES IN PMOS AND NMOS TRANSISTORS AND EFFICIENCY OF DC-DC CONVERTER WITH ZVS AS A FUNCTION OF THE LOAD R_L

	R_L=10 [Ω]	R_L=15 [Ω]	R_L=20 [Ω]	R_L=30 [Ω]	R_L=48 [Ω]
P_{out} [mW]	116.9	112.65	84.5	56.3	35.2
P_{NMOS} [mW]	22.5	21.7	16.3	10.9	6.87
P_{PMOS} [mW]	14.2	13.63	10.25	6.84	4.56
Eff. [%]	69.95	71.15	75.43	80.15	82.68

In Table 3 the total power losses in PMOS and NMOS transistors and efficiency of standard synchronous buck dc-dc converter without ZVS as a function of the load R_L are presented. The average value of the output voltage $V_{out(av)}$ is equal to 1.3 V.

TABLE 3. POWER LOSSES IN PMOS AND NMOS TRANSISTORS AND EFFICIENCY OF DC-DC CONVERTER AS A FUNCTION OF THE LOAD R_L

	R_L=10 [Ω]	R_L=15 [Ω]	R_L=20 [Ω]	R_L=30 [Ω]	R_L=48 [Ω]
P_{out} [mW]	116.9	112.65	84.5	56.3	35.2
P_{NMOS} [mW]	23.4	22.7	16.7	11.5	7
P_{PMOS} [mW]	17.8	16.3	13.6	9.5	8.3
Eff. [%]	67.6	69.7	73.5	78.6	79.8

Power losses in the main PMOS transistor *M*1 as a function of the load R_L are graphically presented in Fig. 6, respectively when buck dc-dc converter work with and without ZVS.

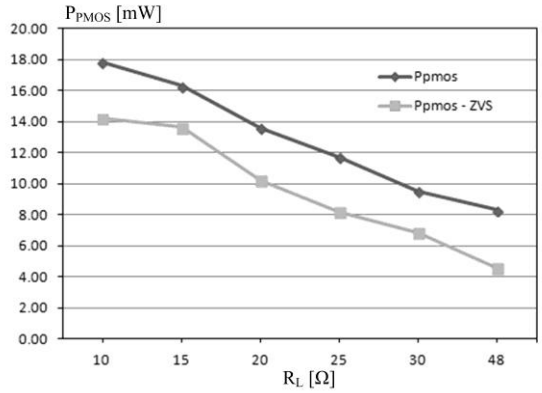

Fig. 6. The power losses in NMOS transistor *M1*, when buck dc-dc converter work with and without ZVS.

Power losses in NMOS transistor *M*2 as a function of the load R_L are graphically presented in Fig. 7, respectively when buck dc-dc converter work with and without ZVS.

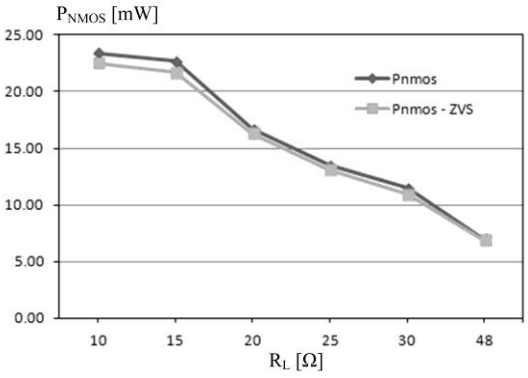

Fig. 7. The power losses in NMOS transistor *M2*, when buck dc-dc converter work with and without ZVS.

The efficiencies of investigated buck dc-dc converter are presented graphically in Fig. 8, when circuit works with and without ZVS. The results presented in Fig. 6 and Fig. 7 show that ZVS leads to decreasing of total power losses in the main PMOS transistor *M*1 of synchronous buck dc-dc converter. This effect helps to increasing of converter's efficiency when ZVS technique is used. The investigations in this paper show that if buck dc-dc converter with ZVS is used as switching-mode converter in the envelope amplifier's hybrid architectures, battery energy of portable electronic devices could be saved. The received results indicate that efficiency of buck dc-dc converter is improved by approximately 1.9% to 3.6%, when the load R_L changes from 10 Ω to 48 Ω.

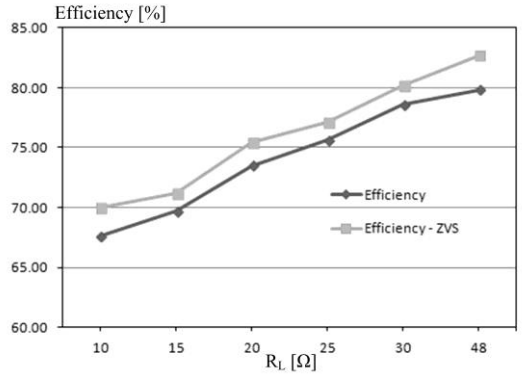

Fig. 8. Efficiency as a function of the load R_L with and without ZVS.

IV. CONCLUSION

A synchronous buck dc-dc converter with Zero Voltage Switching for low power applications has been proposed. Power losses in the converter's components have been investigated and analyzed in Cadence with a CMOS 0.35 μm technology. Battery energy of portable wireless communication devices could be saved if the buck dc-dc converter with ZVS is used as switching-mode converter in the envelope amplifier's hybrid architectures. The results obtained show that the efficiency of the standard switching-mode buck dc-dc converter can be increased by approximately 3.6 % if the ZVS technique is implemented.

V. ACKNOWLEDGEMENT

The research in this paper was carried out within the framework of Contract No. DUNK 01/03 date 12.2009.

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