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Welcome to IEEE – PEMC 2016

Dear conference participants,

It is a great honour and pleasure to welcome you to the 17th IEEE-PEMC2016 conference, held in the beautiful city of Varna.

The Power Electronics and Motion Control (PEMC) conference was founded in the second half of the past century, more precisely 46 years ago, with a slightly different name and a more local orientation. That conference had a great and powerful driver, Professor Istvan Nagy, who gradually shaped and established it into a well-known and internationally recognized scientific event. Also, this internationalization was symbolically expressed by the East-West bridge of the previous logo. After the fall of the East-West physical and psychological barriers, the PEMC conference edition of the 1990 made its first big step into the wider international collaboration, attracting colleagues from a wide spectrum of countries.

Unfortunately for all of us, soon after our last meeting in Antalya, in 2014, we lost Professor Nagy, the man who gave everything to this conference. It is sad that we lost such a great man, but at the same time we were lucky to be able to collaborate with him and to be powered by his positive way of thinking. Even in his last days, he answered phone calls from his hospital bed... He will always teach us on his own example that the good which men do lives after they are gone from our lives. We see that from the seeds he planted, from the life he dedicated to the PEMC, strength for learning, research and development has sprung in all fields of energy and electronics. Therefore, we would like to dedicate this edition of our conference to the memory of Professor Istvan Nagy!

The recent times appear to be challenging for the economies. Our universities neglect the importance of the conference meetings, supporting exclusively the journal publications. The price of attending a conference has become prohibitive so we need to carefully select where to apply the university and research centre funds. In this difficult situation we are even prouder, since at this 17th edition, we have 268 submitted papers, while 195 papers are to be presented. We have now more participants, coming from a greater number of countries (more than 45), in comparison to PEMC 1990 (32 countries), almost equal to the immediately preceding PEMC 2014 (51 countries), held in better, financially more comfortable times.

Another important milestone achieved in this year's edition is that PEMC officially became a conference of the progressive and truly international Industrial Electronics Society (IES) of IEEE. The name IEEE-PEMC is officially reserved for our conference since July 2015. In response to the changes taking place in the conference and in the world at large, we will maintain our PEMC Council as an important advisory board but in the same time we will strictly follow the financial and administrative rules of the IEEE and IES.

The 17th PEMC International Conference is the first edition to open under the name IEEE-PEMC conference and we would like to congratulate everybody that made this possible. In the first place the congratulations go to the participants who contributed with their papers. Without your high PEMC 2016 quality articles, we would not be here today. We would like to express our deepest gratitude to the "army" of voluntary hard working reviewers whose effort contributed for the outstanding quality of the paper selection process. In order to make this conference possible many people abdicated of their personal research, family life, and free time and worked day and night, some of them were paid, many others were not... Special thanks go to all those who contributed with their time and effort for the success of this conference! Last but not least we would like to acknowledge the participation of our reliable industrial friends and colleagues.

We expect that Bulgaria, with its many thousands of years of history, beautiful nature and friendly people will become a frequent venue for the IEEE conferences. We expect to be imaginative in creating new models of conferences, with high value and contribution to humanity. We will be responsive to the changes and provide the environment and culture that fosters talented young human resources for a new and more advanced world.

Please have a look at the conference program and booklet to find out the most important themes for you. We also hope the industrial visitors will draw their conclusions about the research perspectives and applications. We expect next time more companies will send representatives and exhibitors. We wish you a productive conference and hope you enjoy your stay in the beautiful Varna town, a multicultural city with a great selection of outstanding places to visit and to remember!

Welcome to IEEE-PEMC 2016!

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A Study of Parallel Structures of DC-DC Converters for Application in Wind Energy Conversion Systems

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***Abstract*-This paper presents the results of the modeling and comparison of parallel structures of DC-DC converters for application in wind energy conversion systems with low power. Three different topologies with boost capabilities are studied: boost, non-inverting buck-boost and SEPIC converter. The simulation models are created using a Matlab/Simscape environment. Waveforms of currents and voltages in the circuits are analyzed. Current and voltage stress of the components in different converters are compared. The problem of operation of both converters in the structure with non-equal duty ratios is also considered.**

I. Introduction

The stochastic nature of wind has imposed a wider use of wind energy conversion systems (WECS) operating with variable speed because such systems are able to extract the maximum available power at different wind speeds [1], [2], [3], [4]. These WECS mostly use doubly-fed induction generators (DFIG) or synchronous generators (SG) [5]. The use of synchronous generators with permanent magnets (PMSG) is on the increase [6]. The systems that rely on PMSG are subject to growing interest due to their advantages - simplified system control, lower maintenance costs, eliminating the excitation system, etc. [5]. In the WECS based on synchronous generators power electronic converters are used to meet the requirements of the load. The load can be the electrical grid or an isolated consumer. One common structure of power converters for SG consists of a non-controlled rectifier and a DC-DC converter as shown in Fig. 1 [7]. This concept originated with high-power WECS, but nowadays is also used in low-to-medium power wind turbines. The DC-DC converter performs the MPPT algorithm and stabilizes the output DC voltage to a value convenient for operation of an inverter or a DC load (like a battery) [8].

One direction of development for power electronic converters is the connection of two or more converters in parallel [9]. This technique is more frequently used in high-power WECS. However, it can also be applied in small wind generators with power under 10kW [10]. The advantages of parallel converters are: their higher reliability, lower price, increased efficiency [11], [12].

The aim of this study is to develop mathematical and simulation models of paralleled DC-DC converters for application in WECS. The results of the simulations are used to reveal the advantages and drawbacks of each of the studied DC-DC converters.

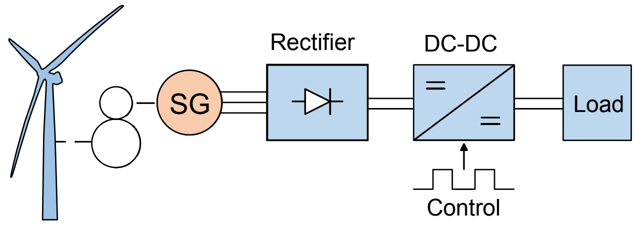

Fig. 1. General structure of WECS with rectifier and DC-DC converter.

II. DC-DC Converters with Boost Capabilities

In order to expand the range of speeds at which the wind turbine operates, it is necessary for the electronic converter to be able to increase the voltage of the generator and the rectifier to a level that is convenient for the charge. The topologies that are found to be appropriate are [13], [14]:

- Boost converter;
- Non-inverting buck-boost converter;
- Single-ended primary-inductor converter (SEPIC).

The studied circuits consist of two parallel connected identical converters with common input and output voltage and interleaved PWM control.

The mathematical modeling of the converters is done under the following assumptions: the resistances of the components are neglected, the transistors and diodes are ideal switches.

A. Parallel Boost Converters

The circuit of an interleaved boost converter is shown in Fig. 2. MOSFET transistors are used as power switches because the voltages are relatively low – under 200V.

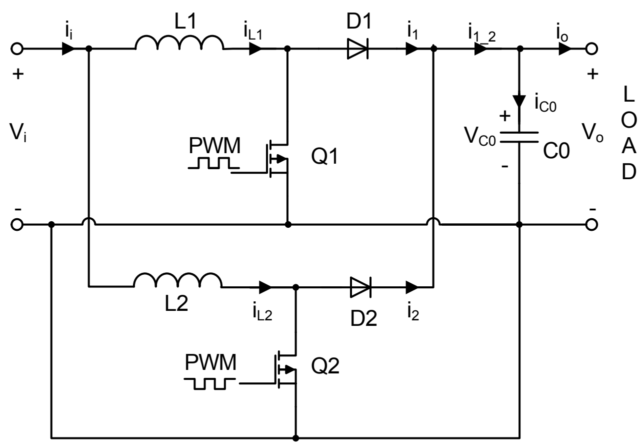

Fig. 2. Two parallel boost converters with common input and output voltage.

When the transistor Q1 is ON the equations for the currents and voltages in the circuit of the first converter are

$$\left| \begin{aligned} \frac{di_{L1}}{dt} &= \frac{1}{L1} V_i \\ \frac{dV_o}{dt} &= \frac{1}{C0}(-i_o) \end{aligned} \right. \tag{1}$$

where i_{L1} is the current in the inductor L1, V_i – the input voltage, V_o – the output voltage, i_o is the output load current.

When the transistor Q1 is OFF the equations are

$$\left| \begin{aligned} \frac{di_{L1}}{dt} &= \frac{1}{L1}(V_i - V_o) \\ \frac{dV_o}{dt} &= \frac{1}{C0}(i_{L1} - i_o) \end{aligned} \right. . \tag{2}$$

It has to be mentioned that the output voltage is equal to the capacitor voltage $V_o = V_{C0}$.

The same equations, (1) and (2), are also valid for the second converter.

When the converters operate in parallel the current in the capacitor Co is

$$i_{C0} = i_{1\_2} - i_o \ . \tag{3}$$

where the current i_{1_2} is the sum of the two currents through the diodes D1 and D2 respectively.

The current i_{1_2} can be expressed as follows:

$$i_{1\_2} = i_{D1} + i_{D2} = i_{L1} + i_{L2} \text{ when Q1 and Q2 are OFF} \tag{4}$$

$$i_{1\_2} = i_{D1} = i_{L1} \quad \text{when Q1 is OFF and Q2 is ON} \tag{5}$$

$$i_{1\_2} = i_{D2} = i_{L2} \quad \text{when Q1 is ON and Q2 is OFF} \tag{6}$$

$$i_{1\_2} = 0 \quad \text{when Q1 is ON and Q2 is ON.} \tag{7}$$

The total input current is equal to the sum of the currents in the two inductors

$$i_i = i_{L1} + i_{L2} \ . \tag{8}$$

The total output current is

$$i_o = \frac{V_o}{R_L} \ . \tag{9}$$

where R_L is the equivalent load resistance.

The relation between the input and output voltage for the boost converter in steady state is

$$V_o = V_i \frac{1}{1-D} \tag{10}$$

where D is the duty ratio of the control pulses.

B. Parallel Buck-Boost Converters

The studied circuit of parallel buck-boost converters is shown in Fig. 3, where a topology of non-inverting buck-boost converter with two transistors and two diodes is used [15]. The transistors Q11 and Q12 operate with common control signal. The switches in the second converter also operate with common control signal but shifted at ½ period from the control signal of the first converter. The equations that describe the converter operation are the following.

When both transistors Q11 and Q12 are ON, the equations for the currents and voltages in the circuit of the first converter are

$$\left| \begin{aligned} \frac{di_{L1}}{dt} &= \frac{1}{L1} V_i \\ \frac{dV_o}{dt} &= \frac{1}{C0}(-i_o) \end{aligned} \right. . \tag{11}$$

When the transistors Q11 and Q12 are OFF the equations become

$$\left| \begin{aligned} \frac{di_{L1}}{dt} &= \frac{1}{L1}(-V_o) \\ \frac{dV_o}{dt} &= \frac{1}{C0}(i_{L1} - i_o) \end{aligned} \right. . \tag{12}$$

Here the output voltage is also equal to the capacitor voltage $V_o = V_{C0}$.

The equations (11) and (12) are also valid for the second converter. The capacitor C0 current is expressed by (3).

The total input current is the sum of the input currents of the two converters

$$i_i = i_{i1} + i_{i2} \ . \tag{13}$$

For the current i_{1_2} we have:

$$i_{1\_2} = i_{D1} + i_{D2} = i_{L1} + i_{L2} \tag{14}$$

when Q11, Q12, Q21 and Q22 are OFF.

$$i_{1\_2} = i_{D1} = i_{L1} \tag{15}$$

when Q11, Q12 are OFF and Q12, Q22 are ON.

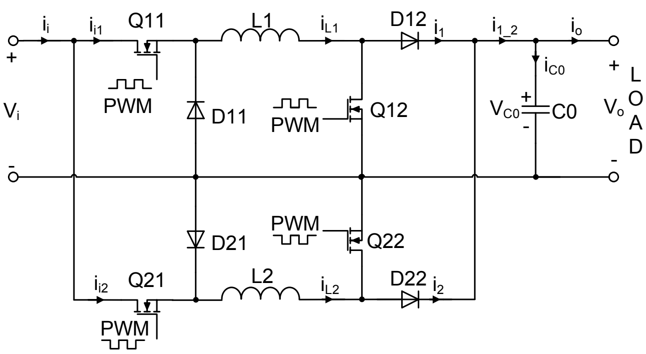

Fig. 3. Circuit of two parallel buck-boost converters with common input and output voltage.

$$i_{1\_2} = i_{D2} = i_{L2} \tag{16}$$

when Q11, Q12 are ON and Q21, Q22 are OFF.

$$i_{1\_2} = 0 \tag{17}$$

when Q11, Q12, Q21 and Q22 are ON.

The output voltage depends on the input voltage and duty ratio D

$$V_o = V_i\left(\frac{D}{1-D}\right) . \tag{18}$$

C. Parallel SEPIC Converters

The SEPIC converter is similar to the buck-boost converter in its relation between output and input voltage. But in the same time it provides non-pulsed input current like the boost converter. The circuit of parallel SEPIC converters is shown in Fig. 4. The transistors Q1 and Q2 operate with interleaved control signals. This converter has more state space variables than the already considered two converters. The mathematical model consists of the following equations.

When the transistor Q1 is ON the equations for the currents and voltages in the circuit of the first converter are

$$\left| \begin{aligned} \frac{di_{L11}}{dt} &= \frac{1}{L11}V_i \\ \frac{di_{L12}}{dt} &= \frac{1}{L12}V_{C1} \\ \frac{dV_{C1}}{dt} &= -\frac{1}{C1}i_{L12} \\ \frac{dV_o}{dt} &= -\frac{1}{C0}i_o \end{aligned} \right. \tag{19}$$

When the transistors Q1 is OFF the equations become

$$\left| \begin{aligned} \frac{di_{L11}}{dt} &= \frac{1}{L11}\left(V_i - V_{C1} - V_o\right) \\ \frac{di_{L12}}{dt} &= -\frac{1}{L12}V_o \\ \frac{dV_{C1}}{dt} &= \frac{1}{C1}i_{L11} \\ \frac{dV_o}{dt} &= \frac{1}{C0}\left(i_{L11} + i_{L12} - i_o\right) \end{aligned} \right. \tag{20}$$

The equations (19) and (20) are also valid for the second converter. The capacitor C0 current is expressed by (3).

The total input current is the sum of the input currents of the two converters

$$i_i = i_{L11} + i_{L21} . \tag{21}$$

For the current i_{1_2} we have:

$$i_{1\_2} = i_{D1} + i_{D2} = i_{L11} + i_{L12} + i_{L21} + i_{L22} \tag{22}$$

when Q1 and Q2 are OFF

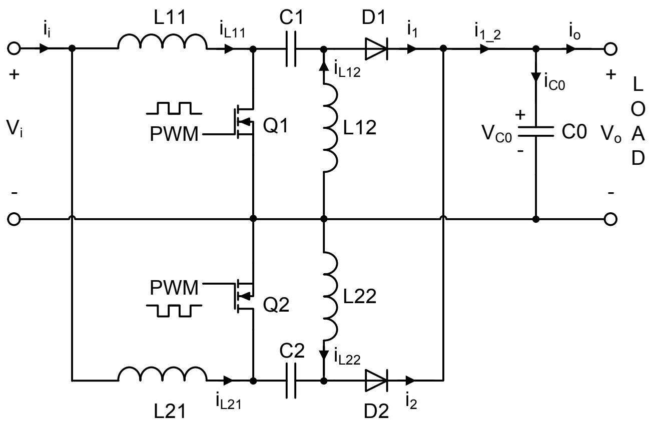

Fig. 4. Circuit of two parallel SEPIC converters with common input and output voltage.

$$i_{1\_2} = i_{D1} = i_{L11} + i_{L12} \quad \text{when Q1 is OFF and Q2 is ON,} \tag{23}$$

$$i_{1\_2} = i_{D2} = i_{L21} + i_{L22} \quad \text{when Q1 is ON and Q2 is OFF,} \tag{24}$$

$$i_{1\_2} = 0 \quad \text{when Q1 is ON and Q2 is ON.} \tag{25}$$

The voltage conversion ratio is expressed by (18) – it is the same as the ratio in the buck-boost converter.

III. Simulation Results

The converters are modeled using the shown circuits in Fig. 2, Fig. 3 and Fig. 4. The simulation models are created using a Matlab/Simscape environment. The circuits' parameters were chosen to be identical in order to obtain comparable results. The used parameters are: input voltage $V_i = 40V$, output voltage $V_o = 160V$, transferred power 800W, L1 = L2 = 1mH, C0 = 1000µF, forward voltage drop in diodes 0.8V, switching frequency 25kHz.

A. Parallel Boost Converters

Fig. 5 and Fig. 6 show waveforms of the currents and voltages obtained by simulation in the parallel boost converters operating in interleaved mode. The duty ratio of control pulses

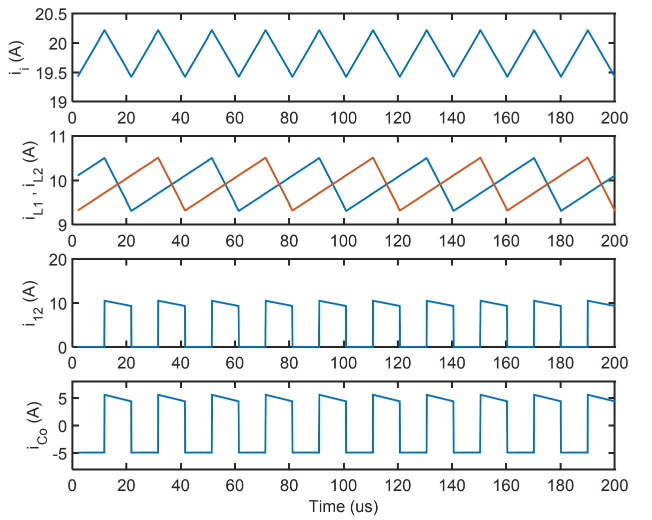

Fig. 5. Simulated waveforms for parallel boost converters. From top to bottom: total input current, inductor currents, current before the capacitor C0, current in the capacitor C0.

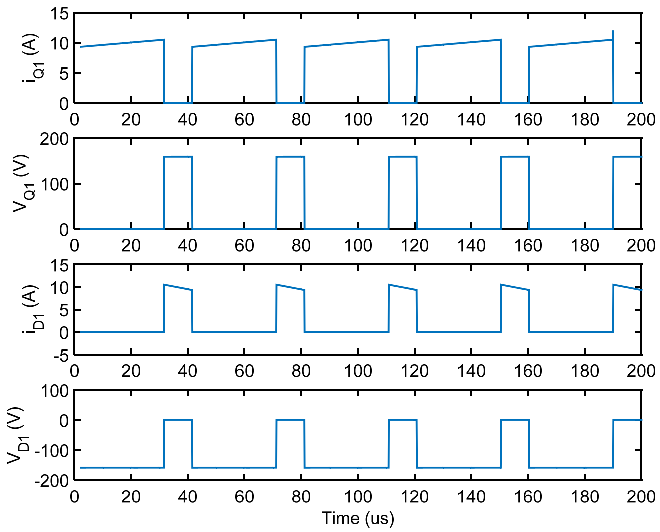

Fig. 6. Simulated waveforms for parallel boost converters. From top to bottom: current in transistor Q1, voltage over transistor Q1, current in diode D1, voltage over diode D1.

is D = ¾ or 75% in order to boost the input voltage 4 times – from 40 to 160V.

The input currents i_{L1} and i_{L2} are equal and the total input current is continuous with ripples smaller than 1A from peak to peak. The ripples in the input current have a frequency which is two times higher than that of the ripples in the input current of each converter. The current through the capacitor C0 is with almost rectangular form and the capacitor is relatively heavily loaded.

From the principle of operation and the circuit on Fig. 2 it is clear that the maximum voltage over the transistors Q1, Q2 and the diodes D1, D2 is equal to the output voltage. This is proven also by the waveforms shown in Fig. 6.

B. Parallel Buck-Boost Converters

Fig. 7 and Fig. 8 show the waveforms of the currents and voltages obtained by simulation of the parallel buck-boost

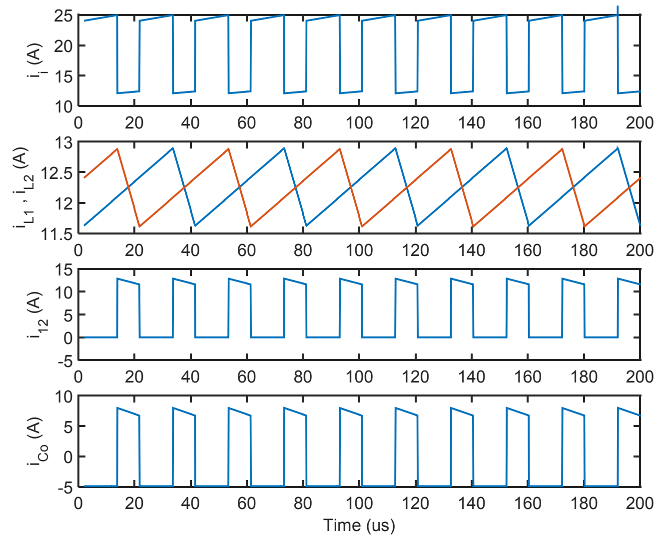

Fig. 7. Simulated waveforms for parallel noninverting buck-boost converters. From top to bottom: total input current, currents in the inductors L1 and L2, current before the capacitor C0, current in the capacitor C0.

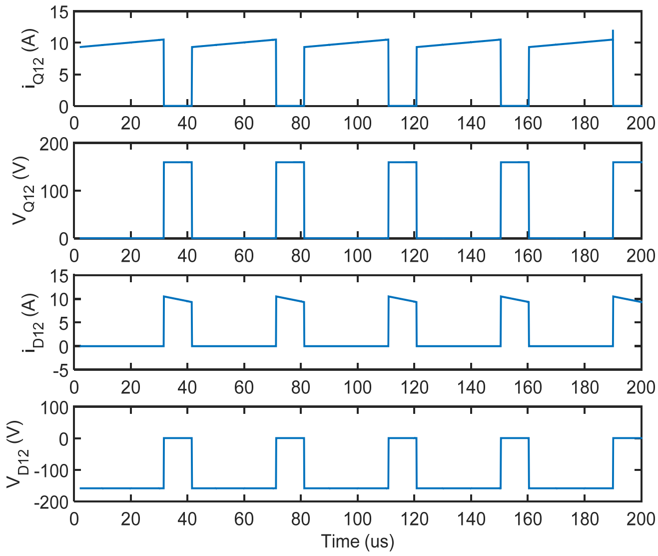

Fig. 8. Simulated waveforms for parallel buck-boost converters. From top to bottom: current in transistor Q12, voltage over transistor Q12, current in diode D12, voltage over diode D12.

converters operating in interleaved mode. The duty ratio of control pulses here is D = ⅘ or 80% in order to obtain output voltage of 160V according to (18).

C. Parallel SEPIC Converters

The inductances of the chokes in this converter (shown in Fig. 4) are: L11 = L12 = L21 = L22 = 0.5mH due to their doubled number. The idea is to keep the converter volume approximately equal to the one of the other converters under study. The capacitors C1 and C2 are 22μF. The duty ratio of control pulses here is D = ⅘ or 80% for output voltage of 160V according to (18). Fig. 9, Fig. 10 and Fig. 11 show the waveforms of the currents and voltages resulting from the simulation of the parallel SEPIC converters operating in interleaved mode.

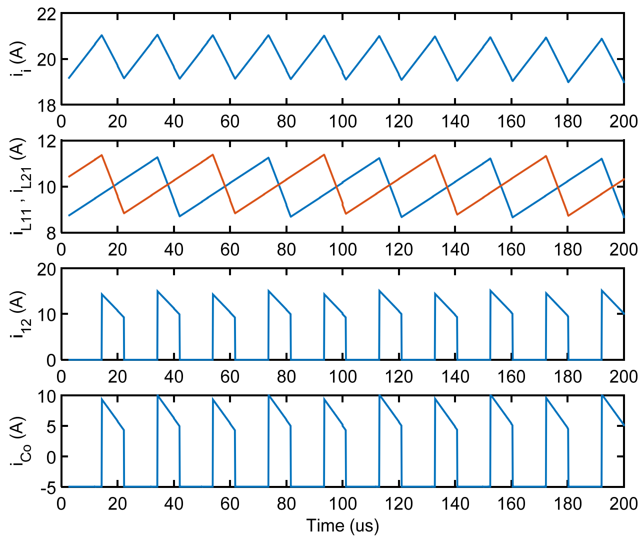

Fig. 9. Waveforms for the parallel SEPIC converters in interleaved mode. From top to bottom: total input current, input currents of the two converters (equal to the L11 and L21 inductors' currents), current before the capacitor C0, current in the capacitor C0.

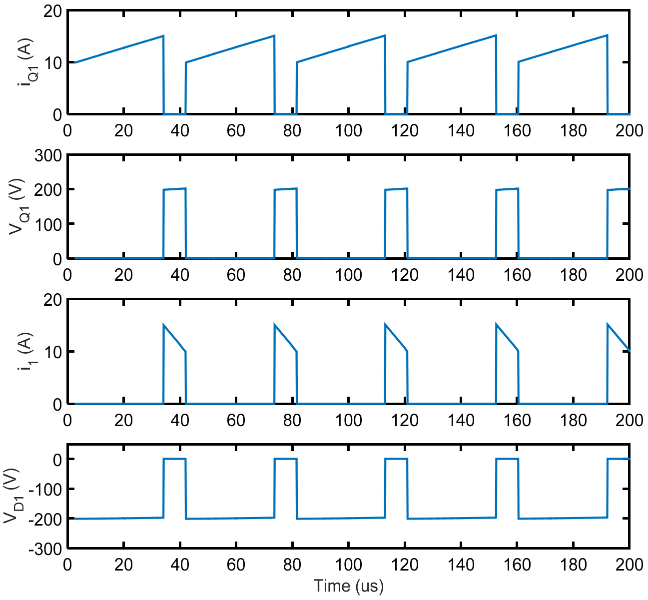

Fig. 10. Waveforms for the SEPIC converter. From the top: current in transistor Q1, voltage over transistor Q1, currents in diode D1, voltage over diode D1.

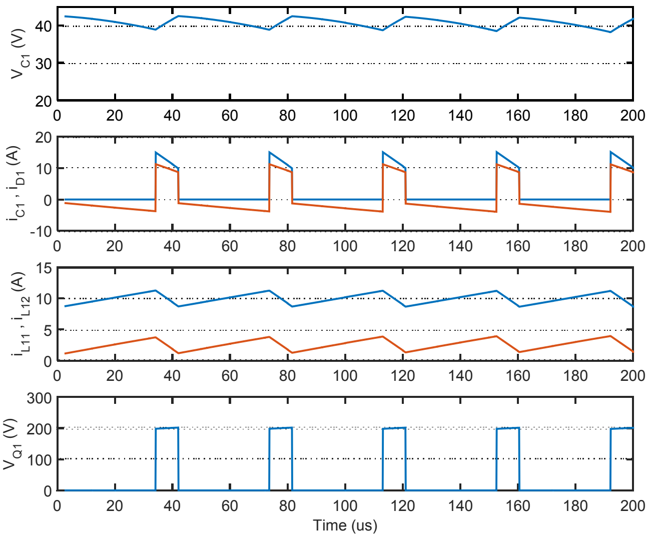

Fig. 11. Waveforms for the SEPIC converter. From the top: voltage over the capacitor C1, currents in diode D1 (blue line) and capacitor C1 (orange line), currents in inductors L11 (blue line) and L12 (orange line), voltage over transistor Q1.

As it can be seen from Fig. 11 the current i_{L11} is considerably higher than the current i_{L12}. From the equality between the input and output power of the studied converter, the ratio between the average values I_{L12} and I_{L11} of these two currents can be derived

$$I_{L12} = \frac{1-D}{D} I_{L11} . \tag{26}$$

D. Comparisons and Problems

The currents' RMS values in some of the main components in the converters' circuits are calculated on the basis of the realized simulations. The results, provided in Table 1, show that:

- The input current of a parallel boost converter has the smallest ripples compared to the other topologies studied in this work.
- The input current of a parallel noninverting buck-boost converter is continuous but still has superimposed rectangular pulses and, consequently, it requires a compulsory input filter capacitor with sufficiently low equivalent series resistance (ESR).
- The RMS current in the output capacitor C0 is smallest in the parallel boost converters, followed by the SEPIC and the noninverting buck-boost converter.
- In the SEPIC converter the additional capacitor C1 (C2) carries considerable RMS current and should have very low losses.
- The RMS current in the inductor (L1 or L11) is highest in the buck-boost converter and in the other two topologies these currents are practically equal (the difference between them is under 1%).
- The voltage stress of the switching transistor is highest in a SEPIC converter – 200V in the studied case, compared to 160V in the other two converters. The same is also true for the diodes.

Another problem that arises in the parallel structures of interleaved DC-DC converters is the non-equal duty ratio of control pulses. It can be shown that a very small difference of the pulse width leads to a considerable difference in the currents of the converters. To prove this statement Fig. 12

TABLE I
CURRENTS' RMS VALUES IN SOME COMPONENTS IN THE CONVERTERS

Converter/Co mponent	Total input current (A)	Current in the capacitor C0 (A)	Current in the capacitor C1 (A)	Current in the inductors L1 or L11 (A)
Boost	19.72	4.94	-	9.87
Buck-Boost	20.51	7.75	-	12.26
SEPIC	19.86	6.14	5.02	9.95

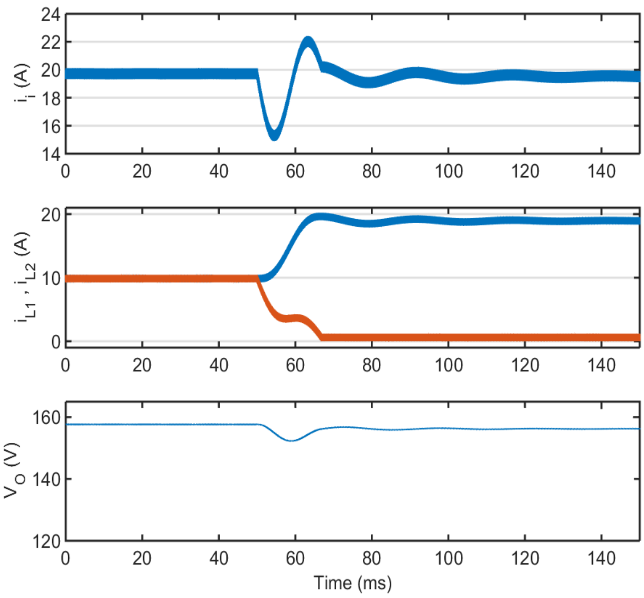

Fig. 12. Waveforms for the parallel boost converters when the duty cycle of the pulses of the second converter is reduced by 1% - from 75 to 74%. From the top: total input current, currents in inductors L1 (blue line) and L2 (orange line); output voltage V_o.

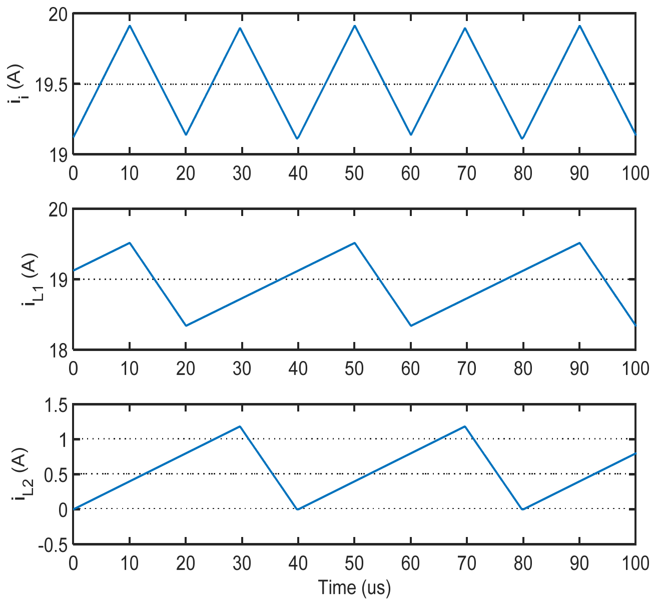

Fig. 13. Waveforms for the parallel boost converters when the first converter operates with duty cycle 75% and the second converter - with 74%. From the top: total input current, current in inductor L1, current in inductor L2.

shows results of simulation of the parallel boost converter where at the time t = 50ms the duty cycle of the pulses of the second converter is reduced by 1% - from 75 to 74%. The difference in the pulse width is only 0.4µs. As a result, the input current average value of the second converter decreases to 0.55A, while the current of the first converter increases to 19.45, as shown in Fig. 12. Fig. 13 illustrates the input currents after the transient in the steady state when the converters operate with different duty ratios. The converter with lower duty ratio operates in discontinuous current mode.

IV. Conclusions

The presented paper studies and compares different topologies of parallel DC-DC converters. The chosen structures are appropriate for wind energy conversion systems with variable speed. Three circuits are studied - boost, non-inverting buck-boost and SEPIC converter. All are able to increase the output voltage to adapt it to the system's needs. The parallel converters consist of two identical converters with common input and output voltages and interleaved PWM control. The circuits are modelled and simulated in a Matlab/Simscape environment. Using simulations the waveforms of currents and voltages in the circuits are obtained. On the basis of the results the maximum voltages over the transistors and diodes in the circuits are found. Besides, the RMS values of currents in important components of the circuits are calculated. The comparison shows that despite his flexibility and low number of semiconductor components the SEPIC converter requires transistor and diodes with higher voltage rates than those of the other two converters at the same current rates. The total input current displays the smallest ripples at parallel boost converter but the difference with the SEPIC is not big. On the other hand the parallel buck-boost still has a pulsed component in its total input current that has to be filtered by an input capacitor. The output filter capacitor is least loaded in parallel boost converters.

The study shows that the above mentioned converters can easily operate in parallel with interleaved control. This type of control improves the input current quality in all cases and facilitates its filtering. Further research includes the development of control techniques for equalization of current sharing, modeling of the common operation of DC-DC converters with synchronous generator and diode rectifier and experimental approval of the theoretical results.

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