Development and Implementation of Digital Phase Locked Loop on Xilinx FPGA

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Abstract – **The subject of the article is development and an implementation of a digital Phase Locked Loop on programmable logic devices from the FPGA XILINX family. The synthesized structural diagram includes 4 MHz reference crystal oscillator, frequency pre-divider, phase frequency detector, digital filter, digitally controlled oscillator and programmable frequency divider. Different types of phase frequency detectors are developed and tested as well as different solutions for digitally controlled oscillators and programmable frequency dividers. The synchronization time, the phase jitter and the overall stability are tested for each individual configuration and different frequency relations.**

Keywords – **Digital Phase Locked Loop, Digitally Controlled Oscillator, Phase Frequency Detector, Digital Filter, Programmable Frequency Divider, FPGA.**

I. Introduction

The phase synchronizers are widely used in today's electronics for generating signals with different random frequencies from a single reference crystal oscillator where the stability of the generated frequencies is equal to that of the reference oscillator. That gives flexibility for user configurable frequency with a defined step. The traditional analog Phase Locked Loops (PLL) have significant drawbacks as slow synchronization when starting and expensive components for the Voltage Controlled Oscillator (VCO) and the filter [1]. Therefore the completely digital type of PLL is preferred.

The VCO is replaced by Digitally Controlled Oscillator (DCO) and the analog filter is replaced with a digital one. The digital PLL also maintains a fixed phase difference but due to the discrete frequency step of the DCO, there is uncertainty of the phase. For that reason sometimes the digital PLL is called Frequency Locked Loop (FLL) [2]. The FLL has a number of advantages over the standard analog PLL:

– completely digital design – everything except the reference oscillator is implemented on the chip;
– high synchronization speed even when the DCO frequency is far from the desired;
– longer service life – less aging components

The FLL is implemented on a Field-Programmable Gate Array (FPGA) integrated circuit of Xilinx Spartan-3A family.

The FPGA logic devices are used to implement any logical function.

A Hardware Description Language (HDL) or logical diagrams are used for configuring of the FPGA.

II. Structure of the Frequency Locked Loop

The structural diagram of the Frequency Locked Loop is represented on Fig. 1. The reference frequency from the 4 MHz crystal oscillator is applied directly to the FPGA to be divided by the frequency divider *M*, defining the desired frequency step. The frequency is then applied to the *Fi* input of the phase frequency detector. The output signal from the DCO is divided by the programmable frequency divider *N* and is applied to the F_0 input of the detector.

The phase frequency detector generates two signals indicating the difference in phase and frequency [3]. These two signals are applied to the digital integrator along with a clock signal. The digital integrator generates the *16 bit* digital code *F* controlling the DCO. The output frequency of the DCO equals the frequency step *Fi* multiplied by the coefficient *N*. The DCO consists of external 16 MHz RC oscillator and a *16 bit* programmable frequency divider.

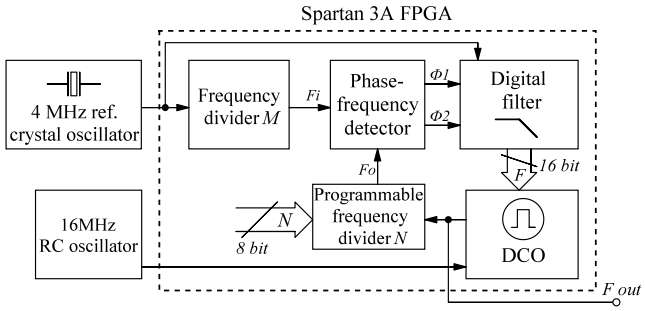

Fig. 1. Frequency Locked Loop structural diagram

III. Structure of the Digitally Controlled Oscillator

The first examined version of the DCO consists of a programmable frequency divider. Its logical diagram is represented on Fig. 2. The programmable frequency divider is built using one *16 bit* reversible parallel loadable binary counter and a T-type flip-flop. The counter is permanently configured for counting down and the Terminal Count (TC) output is connected with the synchronous load input PL. Every time, when the counter reaches zero, TC goes high and the next clock pulse loads the counter with the value *F* applied to the parallel load inputs. Then the process of counting down starts again. The TC signal is also connected to the T input of the flip-flop so every time the counter loads the *F* number, the flip-flop toggles its output level.

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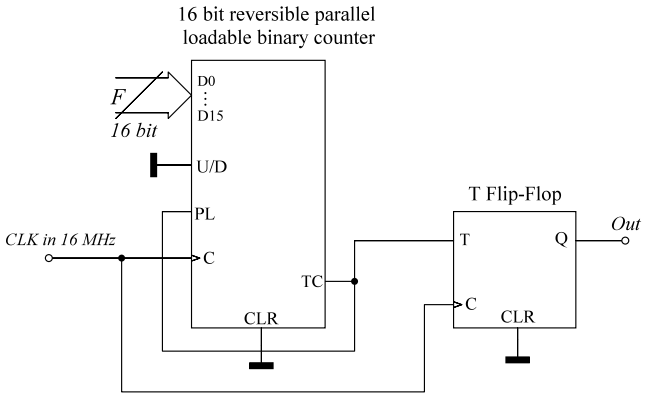

Fig. 2. Logical diagram of the programmable frequency divider for the first DCO version.

The output signal of the DCO is square wave signal with 50% duty cycle and frequency given by the Eq. (1):

$$F_{out} = \frac{F_{in}}{2(1+F)} \tag{1}$$

The range of the output frequencies when using 16 MHz input clock signal is from 122 Hz to 8 MHz with period step of 250 ns. The usable frequency range with reasonably small frequency step is up to about 100 kHz [2].

This configuration is simple and effective but has a drawback. If the frequency has to be changed from low to high value quickly, the value of *F* applied to the parallel load inputs of the counter is changed, but the counter will continue the countdown until it reaches zero and the new value is loaded. So the worst case delay of the frequency change is half period of the lower frequency. This can be a problem when a quick and relatively large frequency jump is required and can lead to problems with synchronization. Due to that reason a second version of the programmable frequency divider is developed. The structural diagram is represented on Fig. 3:

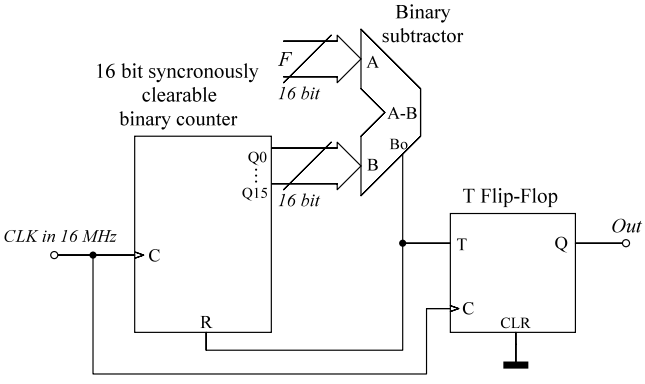

Fig. 3. Structural diagram of the programmable frequency divider for the second DCO version.

The structure includes a standard synchronously clearable *16 bit* binary UP counter, *16 bit* binary subtractor and a T-type flip-flop. The *16 bit* value *F* is connected to the A input of the subtractor, and the *16 bit* output of the binary counter is connected to the B input. The subtractor performs A-B and outputs the difference and the borrow signal [4]. The difference is not used while the borrow signal is connected to the synchronous clear input of the counter and the T input of the flip-flop. The counter increments on every clock cycle of the input signal. Once it exceeds the number F, the borrow output of the subtractor goes high and on the next clock cycle the counter resets to zero and starts to count up again. At the same time the T-type flip-flop toggles its output level. The resulting frequency is given by the Eq. (2):

$$F_{out} = \frac{F_{in}}{2(2+F)} \tag{2}$$

The operation is almost equivalent to that of the previous divider. The frequency range is slightly different from 122 Hz to 4 MHz with the same period step of 250 ns. The reaction to step frequency change from low-to-high in this case is faster. When the number *F* is changed with its new value lower than the previous and the counter has reached a higher value, the borrow output goes high immediately and resets the counter. In this case the change in frequency happens with worst case delay of half period of the higher frequency. This reduces significantly the response time of the DCO to large frequency steps and makes the FLL operation more stable.

IV. Structure of the Phase Frequency Detector and Digital Loop Filter

There are different topologies for phase detectors with different phase angle ranges in which they produce linear output. Most of them has periodical phase-to-voltage response with 180º period and they are not sensitive to frequency differences [3]. That is why they are only applicable when the DCO frequency range is narrow.

The startup process within large range of frequency differences is difficult and can lead to false synchronization to a harmonic frequency. Due to this fact in the FLL a phase frequency detector is used. This type of detector indicates not only the phase difference but also the difference of the frequencies [3]. This allows the FLL to lock successfully at the exact frequency and phase from random DCO frequency at the startup.

The phase frequency detector will be examined along with the digital filter. The combination of the two modules generates the control code *F* for the DCO based on the difference in frequency and phase of the two input signals. The digital filter in this case is digital integrator built with a reversible *16 bit* binary counter [5].

The logical diagram of the phase frequency detector with the integrator is shown on Fig. 4. The phase frequency detector consists of two D-type flip-flops (**A** and **B**) with permanent logical "1" applied to the D inputs and common asynchronous reset signal [3]. The two signals to be compared are applied to the clock inputs of the two flip-flops. When one of the flip-flops receives a rising edge on its clock input, the corresponding Q output goes high. The high level through the XOR gate goes to the Count Enable (CE) input of the counter and it starts counting [6]. This state continues until the other flip-flop receives rising edge and sets its Q output in logical "1". With both Q outputs in

high state the AND gate generates logical "1" at its output which quickly resets both flip-flops. In this configuration the two flip-flops can be both in logical "1" for just about 20 ns as this is the time needed for asynchronous reset. This could theoretically lead to 1 count error in the digital integrator every cycle. This error is eliminated by combining the Q outputs through XOR gate which excludes the short time in which both outputs are high.

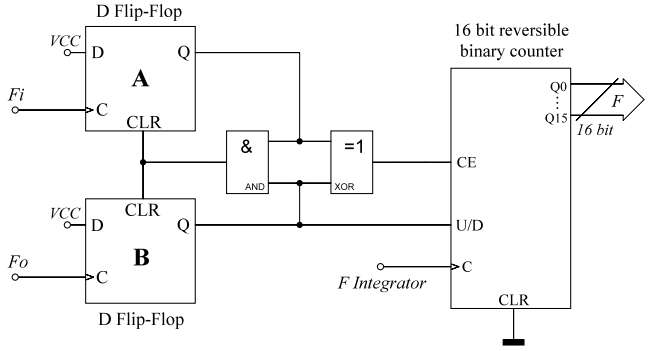

Fig. 4. Logical diagram of the phase frequency detector with digital integrator.

The direction of counting UP or DOWN depends on that which of the two flip-flops has been triggered first. The UP/DOWN signal for the counter is taken from the Q output of flip-flop **B**. If F_0 is leading F_i the **B** flip-flop will be triggered first and the counter will count *n* pulses in UP direction until the **A** flip-flop is triggered and the structure returns to its initial state. This will systematically increase the value *F* which will decrease the DCO frequency until the zero phase difference is restored.

The opposite thing happens if F_i is leading F_0. In this case the **A** flip-flop is triggered first and the counter counts *n* pulses in DOWN direction. The value *F* is decreased to restore the zero phase difference.

The amount of pulses which the digital integrator will accumulate for a period of time is dependent on its clock frequency *F integrator*. This frequency is equivalent to the time constant τ of the RC circuit in the analog filter in an analog PLL and the stability of the system depends on it [6]. The main consideration when choosing this frequency is that its period should be equal or greater than the period step of the DCO. In this case *F integrator* should be less than 4 MHz.

This type of phase frequency detector is insensitive to the duty cycle of the signal as it is edge triggered [3]. It has a simple construction and high speed of synchronization as an advantage but has higher instability when implemented in the FPGA architecture especially with higher values of frequency multiplication *N*. It is also sensitive to the clock signals routing [5]. A good stability in wide frequency range cannot be achieved without changing *F integrator*. The need of adaptive changing of this frequency makes the circuit more complex.

The second version of the phase frequency detector which is examined consists of two *16 bit* binary counters and a *16 bit* subtractor. This detector acts as phase frequency comparator and digital integrator in the same time. Its logical diagram is shown on Fig. 5. The principle of operation is the following. The two frequencies F_0 and F_i are applied to the clock inputs of the two counters. Every counter counts up with the frequency of the signal. The outputs of the two counters are subtracted from one another by the binary subtractor. The difference between them is used to control the frequency of the DCO. If one of the compared frequencies is higher than the other, the corresponding counter is running ahead of the other and the difference between them increases or decreases which changes the DCO frequency. For example if F_i is running faster than F_0 the difference A-B at the output of the subtractor will decrease. This will increase the frequency of the DCO along with F_0 frequency until the same frequency as the reference F_i is achieved.

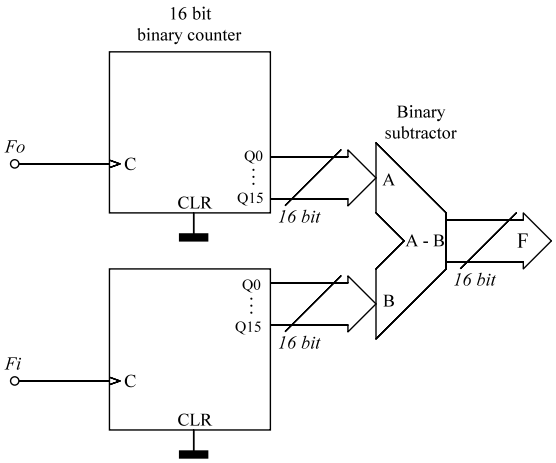

Fig. 5. Logical diagram of the phase frequency detector with counters and subtractor.

This phase frequency detector has very wide linear phase range within 65536 cycles. Unlike the first examined version, this detector is not of the integrating type. For example with a constant phase difference between the two signals F_0 and F_i the first detector will continuously increment the value *F* while the second version outputs a constant value depending on the difference in the number of cycles. A system built with the integrating detector will maintain a zero phase difference while with the non-integrating type it will maintain a constant phase difference. The advantage of this solution is the extreme stability of the FLL over almost the whole frequency range even at high F_{out} to F_i ratios. The drawbacks are the higher phase uncertainty and the very low synchronization speed at low F_{out} frequency.

V. Experimental results

The implementation of the digital frequency locked loop on the FPGA chip shows good results as expected. The design is purely digital with no analog components. The frequency stability of the output signal is the same as the stability of the reference crystal oscillator. The main factor which determines the stability of the system is the phase frequency detector and the digital filter solution. The different concepts are giving completely different results as frequency and phase stability and synchronization speed. The logical diagram of the implementation is shown on Fig. 6.

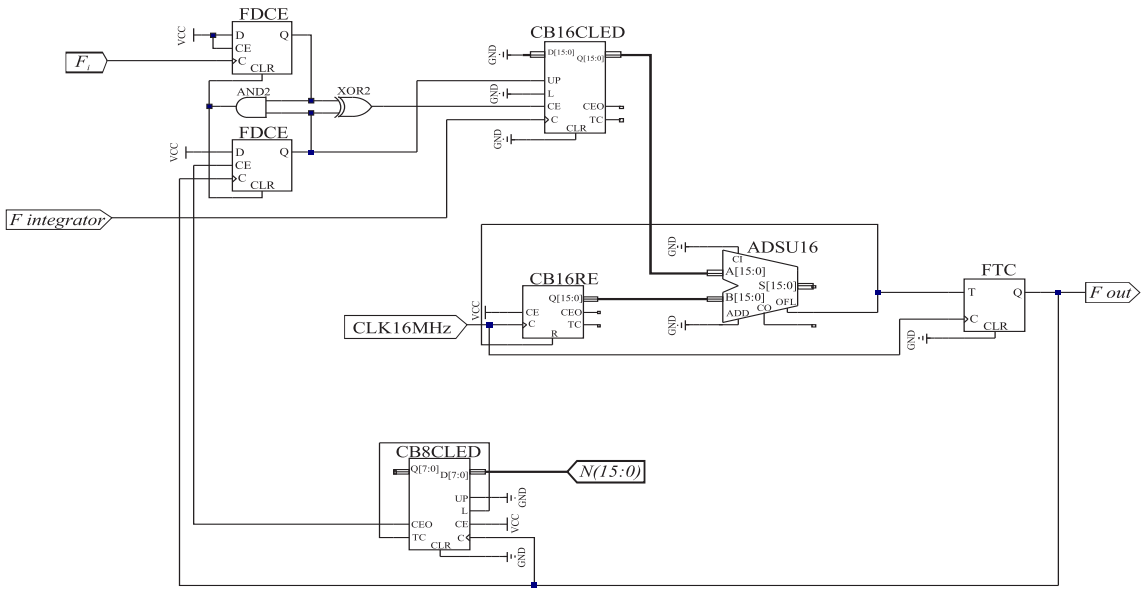

Fig. 6. Logical diagram of the digital FLL implementation

The first examined version of the detector with the two flip-flops is sensitive to the clock signal routing into the FPGA and in some configurations especially when the clock inputs of the triggers are connected to combinational pins there are problems with the synchronization. In some cases the system unlocks periodically at random intervals from 5 to 15 seconds and locks again which results in output signal frequency disturbance. The partial solution to this problem is to feed the clock pins only from clock dedicated signals and no combinational outputs. In this case the CE pins of the counters and the flip-flops are used. The sensitivity to the clock routing is still a big factor in performance with this type of detector and filter.

The second examined version of the phase frequency detector with the two counters and subtractor is very stable and insensitive to the clock signals routing but has a very low synchronization speed.

The direction for further development and achieving better performance is using the best from the two concepts. A hybrid detector is developed in which the most significant *12 bits* are generated from the fast counter integrator while the least significant *4 bits* are generated from the detector with two counters and subtractor. It can be analyzed as fast integrator with dead zone in which the other detector is active. This is going to achieve the stability of the second detector and the high synchronization speed of the first one.

VI. Conclusion

The completely digital PLL gives a good and flexible solution to clock signal generation problems in digital systems. It is a good alternative to the analog PLL with comparable phase jitter and much higher synchronization speed. It is good for systems which are turned on and off frequently or when the frequency is changed often. The absence of external parts and analog stages makes the design more reliable and stable in time. The capacitors and the analog integrated circuits in the analog filter and VCO of the standard PLL are expensive and reduce the reliability of the whole design. It is better alternative to direct digital synthesis as well, when a square wave signal is needed due to the greater simplicity of the method.

If the FLL is made adaptive it can achieve excellent performance and stability in very large frequency range.

If the DCO input clock frequency is high enough, the output period step is so small that the phase uncertainty is almost equal to that of analog PLL system.

VII. Acknowledgements

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