ПРОЕКТИРАНЕ НА ДВУФАЗЕН ПРЕВКЛЮЧВАЩ ПРЕОБРАЗУВАТЕЛ НА НАПРЕЖЕНИЕ ЗА КОМУНИКАЦИОННИ ПРИЛОЖЕНИЯ С CADENCE НА CMOS 0.35 μm ТЕХНОЛОГИЯ

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Резюме: Развитието на елетронните технологии през последните години доведе до нараствало потребление на безжични преносими комуникационни устройства захранвани от батерия, такива като: мобилни телефони, таблети и други. Ефективното използване на енергията, доставяна от захранващата батерия, е свързано с преобразуването й от подходящи токозахранващи схеми. В тази статия е представена схема на двуфазен превключващ преобразувател на напрежение, проектирана с помощта на софтуерния продукт за проектиране на интегрални схеми (ИС) Cadence. Изследвани са два метода на управление на системата на преобразувателя, съответно с широчинно-импулсна модулация и с хистерезисно управление. Получените резултати потвърждават приложимостта на двуфазния превключващ преобразувател на напрежение за комуникационни приложения.

Ключови думи: двуфазен превключващ преобразувател на напрежение, CMOS технология, Cadence.

DESIGN OF TWO-PHASE SWITCHING-MODE CONVERTER FOR COMMUNICATION APPLICATIONS WITH CADENCE ON CMOS 0.35 μM TECHNOLOGY

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Abstract: The electronic and communication technologies have developed rapidly in the last years. This leads to the fast growing market of the battery powered portable wireless communication devices, such like mobile phones, tablets and others. Design and implementation of proper power supply circuits can help to increase the system run-time using more effectively battery's energy. In this is presented two-phase switching-mode interleaved dc-dc converter designed on CMOS 0.35 μm technology with Cadence. Two different types of control respectively pulse-width modulation (PWM) and hysteresis control method have been investigated. The received results prove the applicability of two-phase switching-mode dc-dc converter for wireless communication applications.

Key words: two-phase switching-mode dc-dc converter, CMOS technology, Cadence.

I. INTRODUCTION

Nowadays portable wireless communications devices, like smart phones and tablets, can transfer large data packages in a real time. The peoples have easy access to internet; TV programs; distance controlled home air conditioning systems; and other wireless systems, only with their pocket electronic devices. The increased functionality of the mobile devices is due to the new wireless communication standard called fourth generation Long-Term Evolution (4G LTE). In this standard is used OFDM (Orthogonal Frequency-Division Multiplexing) modulation. The signal is transferred by several sub-carrier frequencies, which are summed at the output of modulator, and thus the spectrum is more effectively used.

The disadvantage of the wireless devices using 4G LTE standard is that battery must be recharged more often. The efficiency improving of the power amplifier (PA), which is the most energy consuming stage in the transmitter, will leads to increasing of the time between two consecutive battery recharges. One of the important characteristics of PAs for LTE applications is that those circuits have to be linear to avoid interference with nearby users [1]. The LTE signals have big peak to average power ratio (PAPR). Therefore in order to improve efficiency of non-efficient linear PAs, the supply voltage of the RF output transistor has to be changed as function of LTE envelope signal. The stage which provides the desire energy to transmitter's PA is called envelope amplifier. Fast and high efficient power supply circuit, which can ensure dynamically changeable voltage to PA, could increase his efficiency. The most promising method reported in the literature is envelope tracking method [2], [3]. Envelope tracking power amplifier (ETPA) system is consisted by envelope amplifier and PA. The efficiency of ETPA system is calculated by formula [4]:

$$\eta_{ETPA} = \eta_{EA} \cdot \eta_{PA},$$
(1)

where η_{EA} is the efficiency of the envelope amplifier; η_{PA} is respectively the efficiency of the PA. As can be seen from the formula above the overall efficiency of the ETPA system depends strongly not only from η_{PA}.

This paper is focused over the design of two-phase switching-mode interleaved amplifier and possibilities to be used as envelope amplifier for LTE mobile wireless applications. The investigations are performed on CMOS 0.35 μm technology of Austria-Microsystems (AMS), which is available in ECAD laboratory.

II. ENVELOPE AMPLIFIERS

The envelope amplifiers, which are used to deliver changeable voltage to RF transistor of the PA, have to have fast tracking speed because the envelope frequency of the LTE signal is increasing. In order to satisfy those requirements in most of the cases power supply circuits for battery powered portable wireless communication devices are hybrid combination between switching-mode dc-dc converter and linear amplifiers [5]. The parallel combined switching and linear regulator topology of envelope amplifier is shown in Fig.1. The load resistor R_L represents the current load of RF PA.
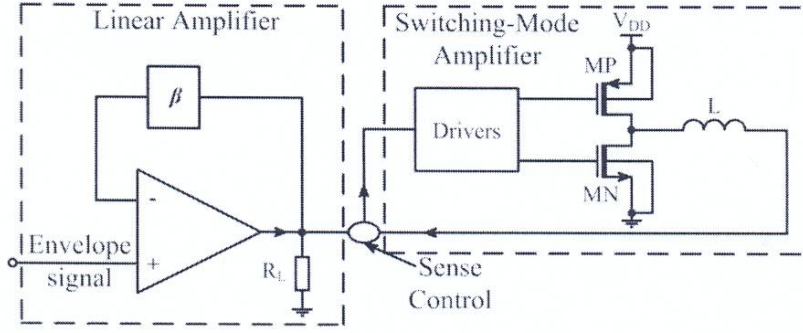
Fig.1. Parallel combined switching and linear regulator topology of envelope amplifier.

This architectures use low efficient linear amplifiers only when high frequency LTE signal is transferred. The standard PWM controlled dc-dc converters are used when low frequency and dc voltages have to be delivered to PAs. Those converters cannot be used as envelope amplifiers separately because they are low bandwidth circuits. The operating switching frequency f_s of PWM controlled dc-dc converters should be 5 to 10 times higher than the bandwidth of the LTE signal [6]. The results will be unacceptable increasing of power losses in the dc-dc converter, because they are proportional to f_s, decreasing overall efficiency in the system.

III. TWO-PHASE SWITCHING-MODE INTERLEAVED DC-DC CONVERTER

The power stage of single phase dc-dc converter is shown in Fig.2. The single phase dc-dc converters indicate high power losses in the inductor at big values of the inductor current ripple Δi_L. Multiphase converter structure helps to reduce this negative effect. The power stage of two-phase interleaved dc-dc converter is illustrated in Fig. 3. The equation of output current $\Delta i_{out.two\text{-}phase}$ of the of two-phase interleaved dc-dc converter as ratio of its single phase $\Delta i_{out.single\text{-}phase}$ counterpart is [7]:

$$\frac{\Delta i_{out.two-phase}}{\Delta i_{out.\sin gle-phase}} = \begin{cases} \dfrac{1-2D}{1-D} & , \quad D < 0.5 \\ \dfrac{2D-1}{D} & , \quad D > 0.5 \end{cases},$$

(2)

where D is duty cycle of the converter. The two-phase interleaved dc-dc converter architecture helps for reducing of the output current ripple Δi_{out} of the circuit. The reason is that the phase sifted inductor current ripples respectively of the first and second sub-converter stage Δi_{L1} and Δi_{L2} are summed at the output. Also the current stress in the switching devices and passive components is reduced [8].
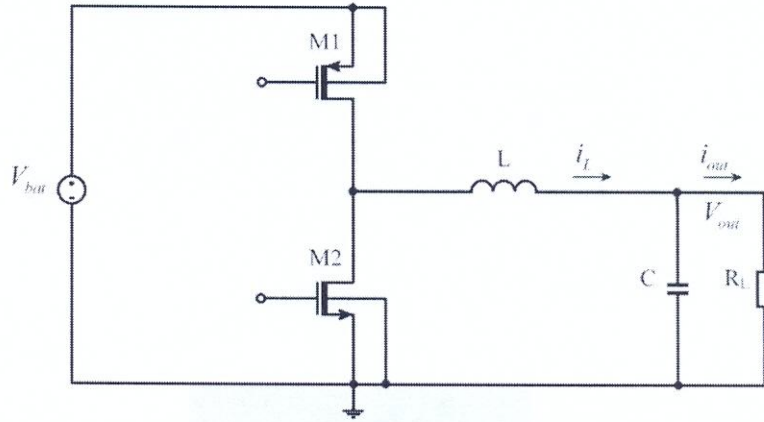
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Fig.2. Power stage of single phase dc-dc converter.

The output current ripple Δi_{out} of the two-phase interleaved buck converter with non-coupled inductors can be expressed by formula [8]:

$$\Delta i_{out} = \frac{V_{out}}{L}(1-2D)T_s,\qquad(3)$$

where T_s is switching period of converter, L is the value of filter inductors (if $L1=L2$, which is the case of the investigated dc-dc converter architecture).
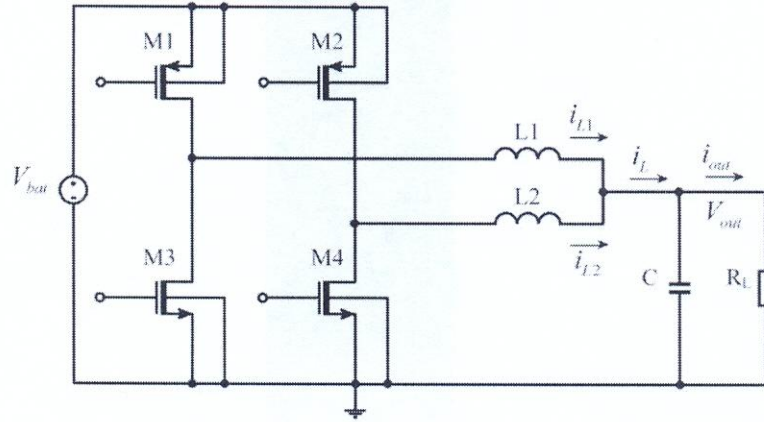

Fig.3. Power stage of two-phase interleaved dc-dc converter.

According to the formula minimum values of the output current ripple Δi_{out} can be received if duty cycle of the converter D is close to 0.5. The inductor current ripples Δi_L of the single phase buck dc-dc converter and two-phase interleaved buck converter with non-coupled inductors have equal values, and can be expressed by formula [8]:

$$\Delta i_L = \frac{V_{out}}{L}(1-D)T_s,\qquad(4)$$

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In two-phase interleaved dc-dc converters architectures the equal output current ripples those of single-phase dc-dc converters could be established with smaller values of output filter inductors respectively *L1=L2*. These phenomena could be very useful for LTE applications power supply circuit, when envelope amplifier have to be fast in order to track high frequency envelope signal. The multiphase dc-dc converter can replace the single phase switching-mode regulator in parallel hybrid envelope amplifier structure. Thus most of the energy delivered to power amplifier can be ensured from fast and high efficient switching-mode multiphase dc-dc converter. The portion distributed from low efficient linear amplifier will be smaller, compare to the case when switching-mode amplifier is single phase dc-dc converter, improving the overall efficiency of envelope tracking power amplifier system.

A. PWM Controlled two-phase interleaved dc-dc converter

Two-phase interleaved dc-dc converter PWM controlled system is designed on CMOS 0.35 µm technology. The block circuit diagram is presented in Fig.4.
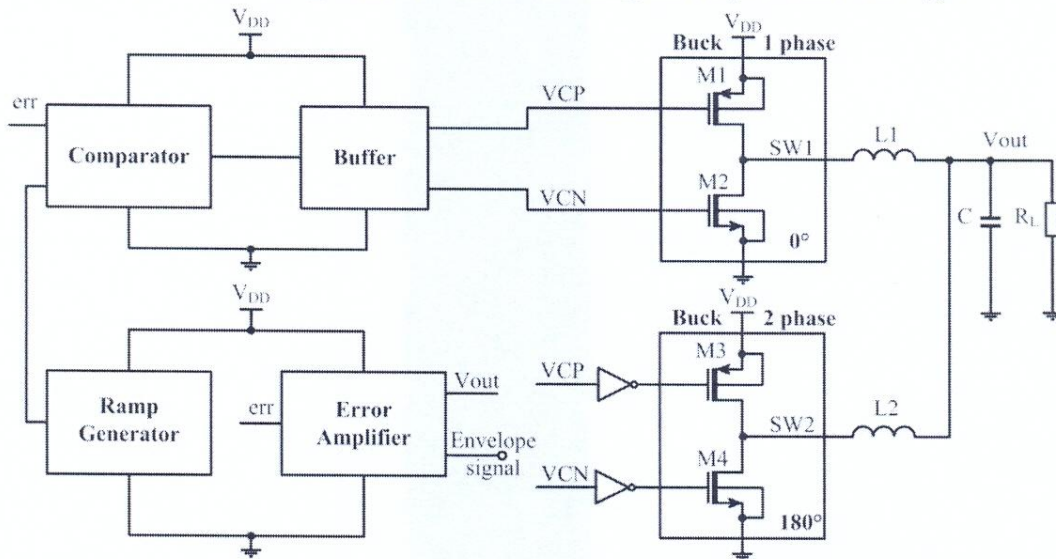

Fig.4. Block diagram of PWM controlled two-phase interleaved dc-dc converter designed on CMOS 0.35 µm technology.

Designed PWM controlled two-phase interleaved dc-dc converter include error amplifier, ramp generator, comparator, buffer and power stage. The both main transistors M1 and M3 of power stage are regulated from control signals, which are phase shifted on 180°. The buffer stage ensures short time when NMOS and PMOS transistors, respectively of the first and second buck power stages, are both switched-off. Thus the outputs stages are prevented from short-circuit losses, which can occur when the both power MOS transistors are switched-on simultaneously. Also this helps to decreasing of power losses in the main transistors of dc-dc converter. The circuit's architecture of the buffer used in the PWM controlled system is shown in Fig.5 [9].
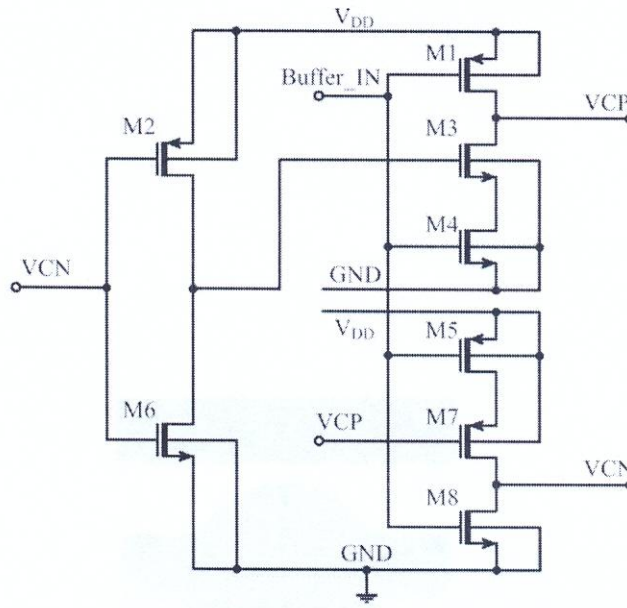
Fig.5. Buffer stage of the PWM controlled two-phase interleaved dc-dc converter.

The supply voltage V_{DD} is equal to the output voltage of the standard lithium-ion batteries, which is 3.6 V. The switching frequency f_s of the designed PWM controlled two-phase interleaved dc-dc converter determined by ramp generator is equal to 76 MHz.

The capacitance value of output filter capacitor C is equal to 5 pF. This value is chosen in order to be investigated behavior of the circuit when two-phase dc-dc converter perform the functions of switching-mode amplifier in parallel combined hybrid architecture of envelope amplifier for LTE applications.

This is the real value of equivalent capacitance of parallel combination of the power transistor of linear amplifier [10].

The values of output filter inductors $L1$ and $L2$ of investigated interleaved dc-dc converter are equal to 125 nH.

The simulation results, which show the waveforms of inductor current ripples (Δi_{L1} and Δi_{L2}) and output current ripple Δi_{out} of two-phase buck dc-dc converter, are presented in Fig.6.

As can be seen from the picture the output current ripples of the two-phase interleaved dc-dc converter Δi_{out} is decreased around 10 times compare to inductor current ripples of the separate sub-converter stages.

This confirms the statement expressed above, that multiphase dc-dc converter architecture can replace the single phase dc-dc converter in the parallel hybrid envelope amplifiers for LTE applications.
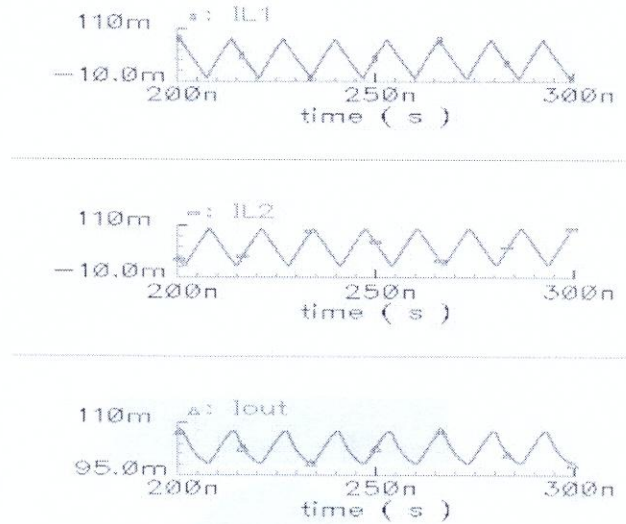
Fig.6. The waveforms of inductor current ripples (Δi_{L1} and Δi_{L2}) and output current ripple Δi_{out} of two-phase buck dc-dc converter designed on CMOS 0.35 μm technology.

To emulate the fast changing LTE envelope signal for the investigation of the designed dc-dc converter system sinusoidal signal with frequency equal to 20 MHz is used. The designed PWM controlled system can deliver to the load energy from 20 mW to 1W. The simulation results presented in the picture above are received when output power of two-phase dc-dc converter is equal to 160 mW.

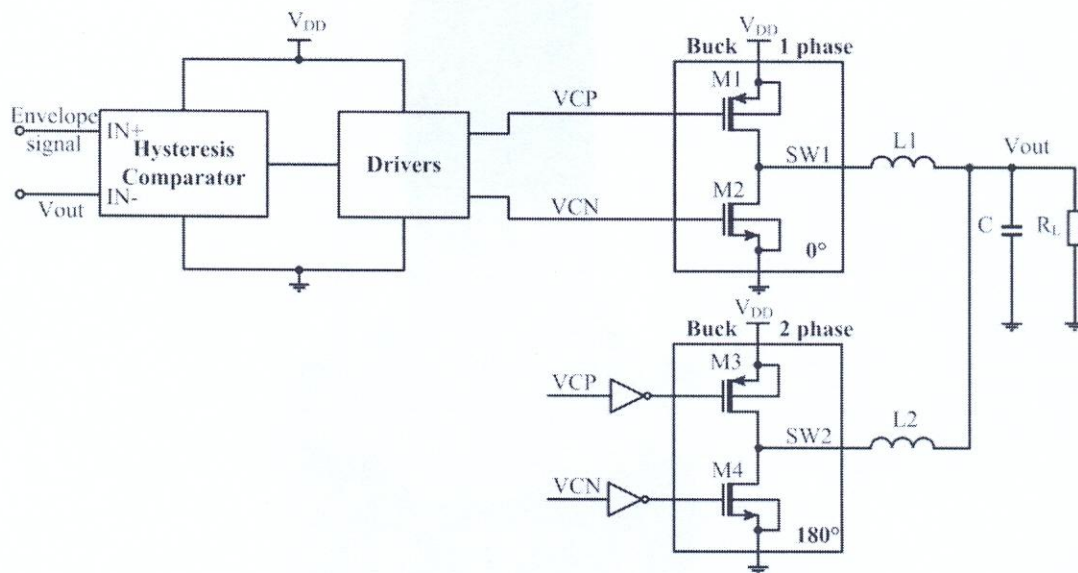### B. Hysteresis Controlled two-phase interleaved dc-dc converter

Fig.7. Block diagram of hysteresis controlled two-phase interleaved dc-dc converter designed on CMOS 0.35 μm technology.

Two-phase interleaved dc-dc converter hysteresis controlled system is designed on CMOS 0.35 μm technology. This control method allows increasing the bandwidth of the converter up to switching frequency f_s [6]. Thus using lower f_s, compare to the PWM control technique, the LTE bandwidths could be covered and power losses in the dc-dc converter will be smaller. The block circuit diagram is presented in Fig. 7. The supply voltage V_{DD} is equal to 3.6 V. The values of output filter inductors $L1$ and $L2$ of are equal to 125 nH. The value of output filter capacitor C is equal to 5 pF. The circuit of the hysteresis comparator used in the system is shown in Fig.8.
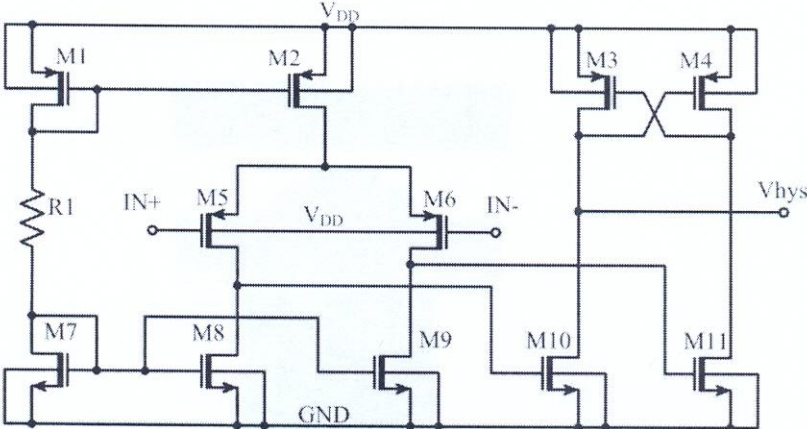

Fig.8. The schematic of the hysteresis comparator.

The designed hysteresis controlled two-phase interleaved dc-dc converter is investigated when the envelope input signal of comparator with hysteresis has a sinusoidal waveform with frequency equal to 20 MHz.
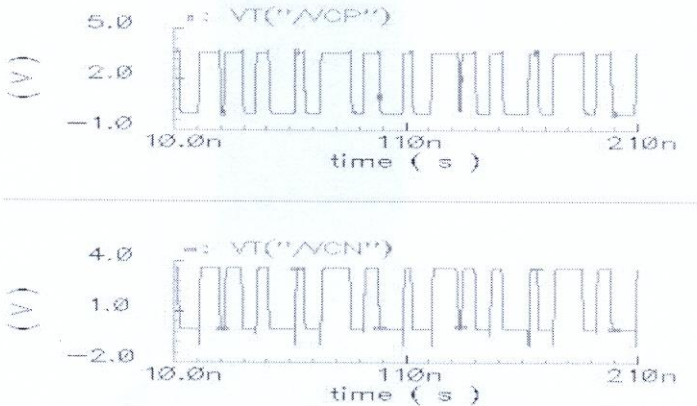

Fig.9. The waveform of the control signal VCP and VCN, when envelope sinusoidal signal has dc voltage equal to 1.2 V and amplitude equal to 500 mV.

The waveform of the control signal VCP and VCN, which regulate respectively the modes of operation of the power transistor M1 and M2 of the first sub-converter are presented in Fig.9. In this particular case the sinusoidal signal, which emulates LTE envelope signal, has dc voltage equal to 1.2 V and amplitude equal to 500 mV.
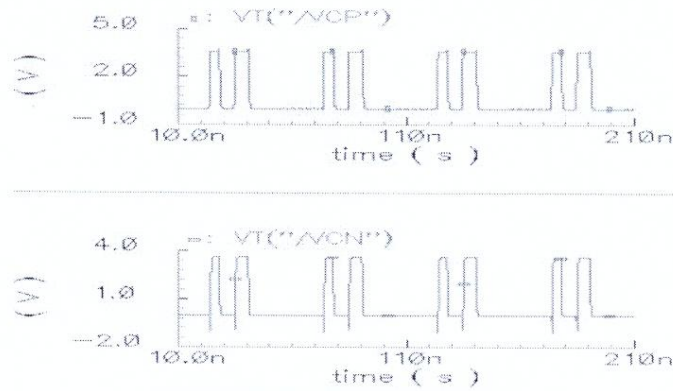
Fig.10. The waveform of the control signal VCP and VCN, when sinusoidal signal has dc voltage equal to 1.8 V and amplitude equal to 500 mV.

The waveform of the control signal VCP and VCN when sinusoidal signal applied to hysteresis comparator has dc voltage equal to 1.8 V and amplitude equal to 500 mV.

IV. CONCLUSION

In this paper is presented two-phase switching-mode interleaved dc-dc converter designed on CMOS 0.35 μm technology with Cadence. Two different controls respectively PWM and hysteresis method have been investigated. The possibilities the designed circuit to be used in parallel hybrid envelope amplifier for LTE applications, as a switching-mode amplifier, is considered. The investigation results show, that output current ripples of the two-phase interleaved dc-dc converter Δi_{out} is decreased around 10 times compare to inductor current ripples of the separate sub-converter stages in PWM controlled system. The reaction of hysteresis control system, when envelope signals with different voltage level are applied, is illustrated. The received results prove the applicability of two-phase switching-mode dc-dc converter for wireless communication applications.

ACKNOWLEGMENT

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