Layout Design of Switching-Mode Amplifier for LTE Applications

Tihomir Sashev Brusev and Rossen Ivanov Radonov

Abstract – **The layout design of hysteresis controlled switching-mode amplifier for fourth generation Long-Term Evolution (4G LTE) applications is presented in this paper. Those circuits are used in envelope amplifiers (EAs) architectures, which supply voltage to the transmitter's power amplifier (PA). The proper layout design can help to improve the overall efficiency of EA, because most of the energy delivered to PAs is supplied by a switching-mode amplifier. The design is made with Cadence using AMS CMOS 4-metal 0.35 µm technology. The investigation and comparison between efficiency results from the simulation of schematic and layout with extracted parasitic devices is performed.**

Keywords – **Switching-mode amplifiers, CMOS 0.35 µm 4-metal technology, Layout, Efficiency, Cadence**

I. INTRODUCTION

The new wireless communication standard 4G LTE allows transfer of large date packages in real time. The reason is that in LTE orthogonal frequency division multiplexing (OFDM) modulation is used. Information is transferred by several sub-carrier frequencies, which are summed at the output of the system. As a result the transmitted signal has big variation of the amplitude [1]. Therefore linearity of transmitter's PA is very important characteristic, because it helps to avoid interference with nearby users. The disadvantage of linear PAs is that they indicate low efficiency results. One of the most useful methods for efficiency improving of PA is envelope tracking method [2], [3]. Envelope amplifier in this technique, supply dynamically changeable voltage to drain or collector of PA's RF transistor as a function of envelope signal [4].

Efficiency of envelope tracking power amplifier (ETPA) system, consisted by envelope amplifier and PA, is determined by [2]:

$$\eta_{ET\,PA} = \eta_{EA}.\eta_{PA}, \quad (1)$$

where η_{EA} is the efficiency of the envelope amplifier; η_{PA} is respectively the efficiency of the PA. The formula above shows that efficiency of envelope amplifier is a key for improving $\eta_{EA\,PA}$, taking into account low efficiency of linear power amplifiers. The most popular EA's architectures, presented in the literature, are combination between linear amplifier and switching-mode amplifier [5], [6]. Advantages of fast linear amplifier stage and high efficiency switching-mode stage are used in those hybrid circuits. Transmitter's PA in LTE applications work with high peak to average power ratio (PAPR). In most of the time these circuits have to work in the back-off mode of operation. Switching-mode amplifier in hybrid EA architectures is used to deliver low frequency and dc voltages, while linear amplifier has to supply high frequency voltages to PA. The efficiency of envelope amplifier depends strongly on switching-mode amplifier's efficiency, because this stage delivers about 80% of the total output power to the PA [4].

The signals in LTE standard have bandwidths up to 40 MHz with a trend of further increase. The disadvantage of pulse-width modulation (PWM) controlled switching-mode amplifiers is that they are low bandwidth circuits. Their switching frequency f_s have to be about ten times higher than the bandwidth of the LTE signal, which leads to unacceptable efficiency degradation [7]. On the other hand hysteresis control allows increasing of switching converter's bandwidth up to switching frequency f_s [7]. Therefore this method ensures LTE bandwidths to be covered using lower f_s, increasing efficiency of switching-mode amplifier.

An integrated circuit (IC) layout of hysteresis controlled switching-mode amplifier designed with Cadence is presented in Section II of this paper. The investigation efficiency results from the simulations of schematic and layout with extracted parasitic devices are presented in Section III.

II. LAYOUT DESIGN OF HYSTERESIS CONTROLLED SWITCHING-MODE AMPLIFIER

Hysteresis control allows switching-mode amplifier to operate with lower switching frequency f_s compared to PWM control covering the equal bandwidths of LTE signals. Thus power losses in the building blocks and power transistors are decreasing. In Fig. 1 is shown a block circuit of hysteresis controlled switching-mode amplifier, which is designed using AMS CMOS 0.35 µm process.

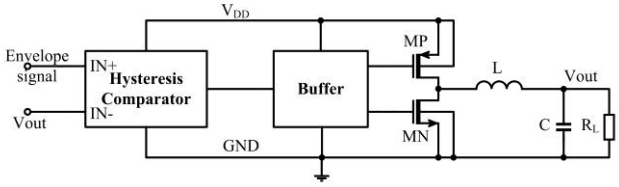

Fig. 1. Block circuit of hysteresis controlled switching-mode amplifier designed CMOS 0.35 µm process.

Wireless portable electronic devices, like mobile phones and tablets, use lithium-ion batteries. For that reason power supply voltage V_{DD} of the designed circuit is chosen to be

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equal to 3.6 V, which is standard output voltage of this type of batteries. The inductance value of filter inductor L is equal to 250 nH, while capacitance of the output filter capacitor C is equal to 5 pF, which is equivalent capacitance value of parallel combination between power transistor of linear amplifier. The resistor's value R_L represents the current load of RF power amplifier. The schematic of comparator with hysteresis is illustrated in Fig. 2. A LTE envelope signal is applied to the input "IN+". A signal sinusoidal waveform with frequency equal to 20 MHz is used as a test signal. This signal doesn't represent the real waveform of LTE signal. Nevertheless using this test fast changing LTE envelope signal could be emulated.

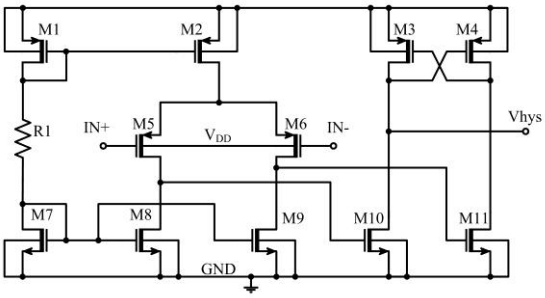

Fig. 2. Schematic of comparator with hysteresis.

The layout of the comparator with hysteresis is designed using Virtuoso layout tool of Cadence IC package and AMS CMOS 0.35 μm 4-metal technology. The layout is shown in Fig. 3.

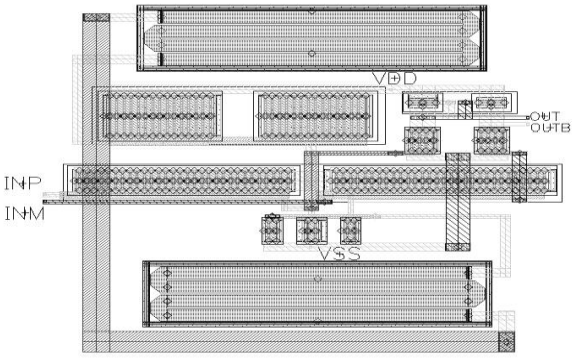

Fig. 3. Layout of comparator with hysteresis.

The circuit's topology of the buffer stage used in the hysteresis controlled switching-mode amplifier is presented in Fig. 4 [8].

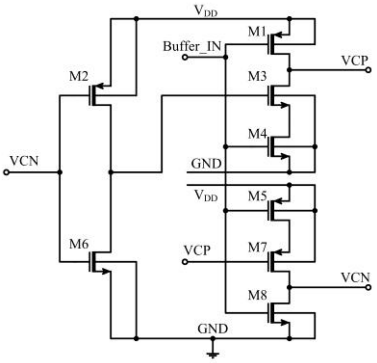

Fig. 4. Buffer circuit's topology.

The buffer's topology ensures short time when NMOS and PMOS transistors in the power stage are both switched-off. Thus power stage is prevented from short-circuit losses when both power MOS transistors are switched-on simultaneously. The layout of buffer stage is presented in Fig. 5.

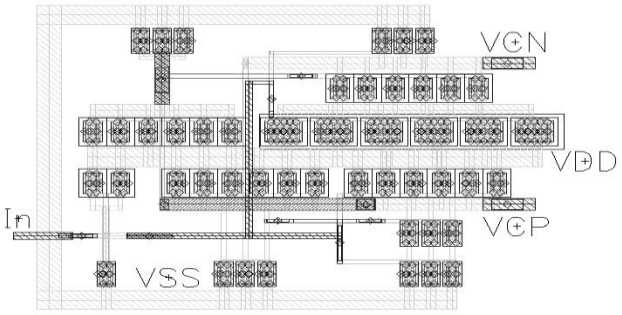

Fig. 5. Layout of Buffer.

The layout of the hysteresis controlled switching-mode amplifier designed on AMS CMOS 0.35 μm 4-metal technology is presented on Fig. 6.

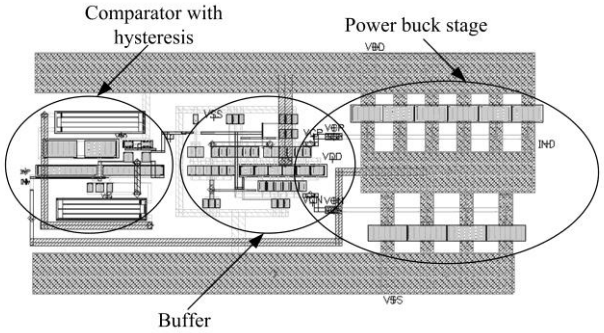

Fig. 6. Layout of hysteresis controlled switching-mode amplifier.

In order to verify the proper work of the designed switching-mode amplifier, a re-simulation of the layout design with extracted parasitic devices is performed. The results are compared with the simulation results of the designed circuit at the schematic level. The verification is made at different dc levels of the sinusoidal envelope signal.

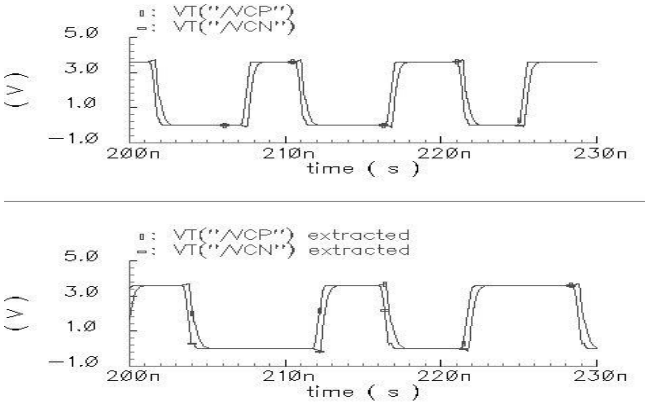

Fig. 7. Buffer's output control signals VCP and VCN of schematic and layout with extracted parasitics, when envelope sinusoidal signal has dc voltage equal to 1.2 V and amplitude equal to 500 mV.

In Fig. 7 are presented buffer's output control signals VCP and VCN, which regulate the state of power MOS

transistor, of schematic and layout with extracted parasitics, when envelope sinusoidal signal has dc voltage equal to 1.2 V and amplitude equal to 500 mV. As can be seen from the picture short gap time is ensured when both NMOS and PMOS output transistors of buck converter are switched-off. Also the control pulses obtained after re-simulation of layout with extracted parasitics are slightly larger and phase shifted compared to those obtained after schematic simulation. This is due to the parasitic capacitors formed by the inevitable overlapping of the metal layers. The same signals at different time range are shown in Fig.8. Larger time range helps to compare VCP and VCN signals at different dc voltage levels of sinusoidal envelope signal. On the other hand at larger time range short gap time cannot be seen when power MOS transistors are both switched-off.

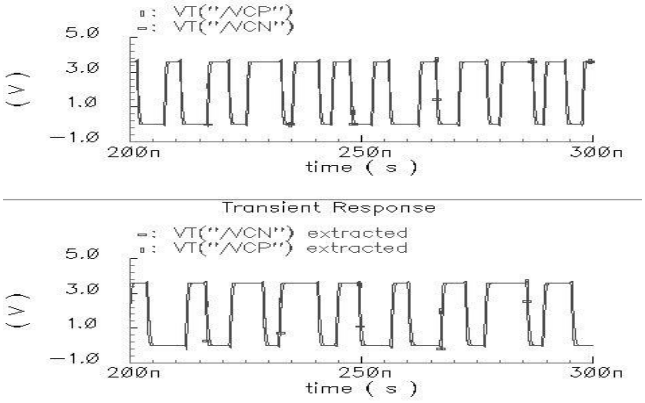

Fig. 8. VCP and VCN when envelope sinusoidal signal has dc voltage equal to 1.2 V and amplitude equal to 500 mV.

The signals VCP and VCN are shown in Fig. 9 when envelope sinusoidal signal has dc voltage equal to 1.8 V and amplitude equal to 500 mV.

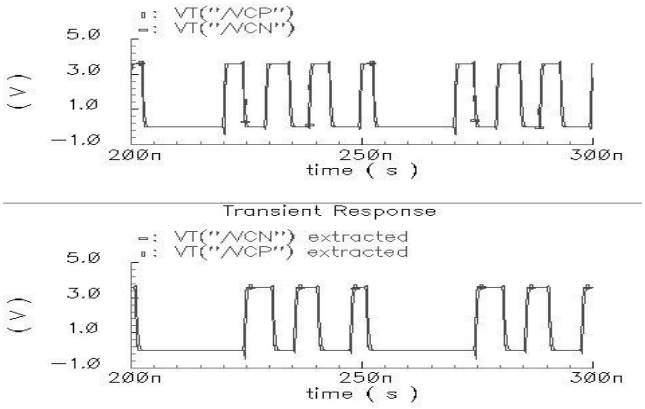

Fig. 9. VCP and VCN when envelope sinusoidal signal has dc voltage equal to 1.8 V and amplitude equal to 500 mV.

The reaction of the system can be seen in Fig. 8 and Fig. 9 when different envelope signals are applied to hysteresis comparator. The small number of pulses generated from the re-simulation of the layout with extracted parasitics, compare to those generated from simulation of the schematic are due to their greater pulse width. This fact proves that after layout design the hysteresis controlled switching-mode amplifier works properly.

III. EFFICIENCY INVESTIGATION OF THE DESIGNED SWITCHING-MODE AMPLIFIER

The efficiency of the switching-mode amplifier is calculated by formula:

$$\eta = \frac{P_{out,avg}}{P_{in,avg}}, \tag{2}$$

where $P_{in,avg}$ and $P_{out,avg}$ are the respective average input and output power of the circuit. In the Table 1 are presented the simulation results of the efficiency as a function of R_L, when the average output voltage $V_{out,avg}$ of the switching-mode amplifier is equal to 1.2 V. The values of the R_L are changed between 10 Ω and 30 Ω, because those numbers represent the practical equivalent value of PA used as a load [6].

TABLE 1. EFFICIENCY S A FUNCTION OF RL AT $V_{OUT,AVG}$=1.2 V

	R_L=10 [Ω]	R_L=15 [Ω]	R_L=20 [Ω]	R_L=25 [Ω]	R_L=30 [Ω]
Eff. [%]	47.71	55.45	59.24	61.17	61.54
Eff. [%] - layout	45.34	53.03	57.22	58.98	59.57

In Table 2 the efficiency results are given obtained after simulation respectively of schematic and layout with extracted parasitics as function of R_L, when $V_{out,avg}$=1.5 V.

TABLE 2. EFFICIENCY AS A FUNCTION OF RL AT $V_{OUT,AVG}$=1.5 V

	R_L=10 [Ω]	R_L=15 [Ω]	R_L=20 [Ω]	R_L=25 [Ω]	R_L=30 [Ω]
Eff. [%]	49.15	57.14	61.19	63.86	64.58
Eff. [%] - layout	46.45	54.74	59.81	61.67	63.47

In Table 3 are presented efficiency results as function of R_L, when $V_{out,avg}$=1.8 V.

TABLE 3. EFFICIENCY AS A FUNCTION OF RL AT $V_{OUT,AVG}$=1.8 V

	R_L=10 [Ω]	R_L=15 [Ω]	R_L=20 [Ω]	R_L=25 [Ω]	R_L=30 [Ω]
Eff. [%]	50.15	58.36	63.33	66.28	68.05
Eff. [%] - layout	46.48	56.29	61.23	64.6	66.58

It can be seen from the results presented in Table 1, Table 2 and Table 3, that the efficiency of the switching-mode amplifier obtained after re-simulation of the layout design with extracted parasitic devices is smaller in comparison to the results after simulation of the schematic. This is due to the parasitics formed after layout design of the circuit. They lead to extra power losses, which are not included in efficiency results in schematic simulations. The results given in Table 3 when $V_{out,avg}$=1.8 V, are graphically presented in Fig. 10.

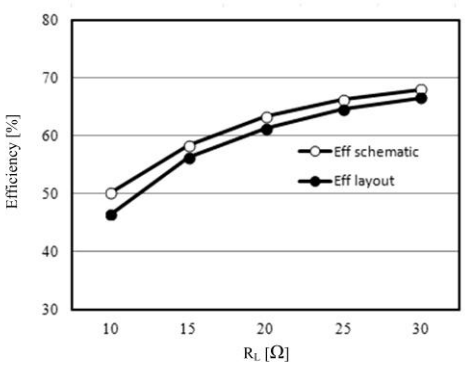

Fig. 10. Efficiency of the switching-mode amplifier as a function of the load R_L, *when* $V_{out,avg}$*=1.8 V.*

The total estimated parasitic capacitance formed by overlapping of the metal layers is equal to 1 pF. The main contributor is power buck stage. In this stage four metal layers in parallel are used in the layout design, to ensure the highest output current of the switching-mode amplifier.

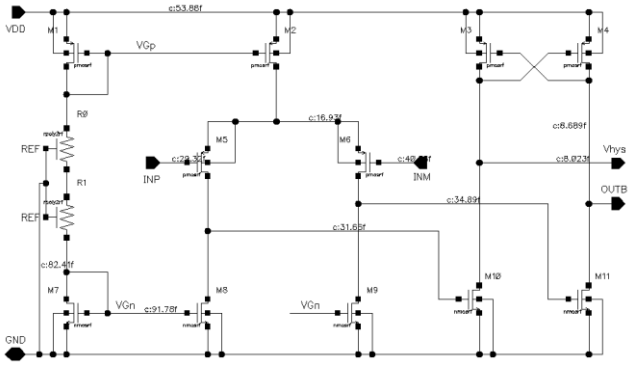

Fig. 11. Schematic of net's capacitive load of comparator with hysteresis.

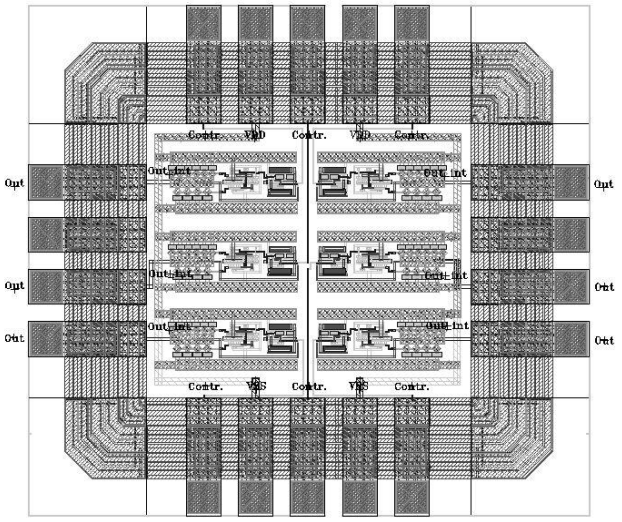

Fig. 12. Layout top view of switching-mode amplifier system.

The parasitic capacitance can be reduced by using fewer metal layers, but then occupied silicon will be larger. The parasitic capacitance formed in the power buck stage is 85% of total parasitic capacitance. Nevertheless, the simulation results show that the designed circuit works properly after layout design. The schematic of net's capacitive load of comparator with hysteresis is shown in Fig. 11. The layout including pad rings of the designed hysteresis controlled switching-mode amplifier is presented in Fig. 12.

IV. CONCLUSION

In this paper the layout design of hysteresis controlled switching-mode amplifier for wireless communication applications is presented, performed with Cadence on AMS CMOS 4-metal 0.35 μm technology. The re-simulation of the layout with extracted parasitics proves the proper work of the circuit. The parasitics decrease the overall efficiency of the system between 1.2 % and 3.5 %.

ACKNOWLEDGEMENT

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