Design of Power Supply Circuit for Measurements of Geomagnetically Induced Currents in Power Networks

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Abstract – **In this paper is presented power supply circuit designed to deliver desire energy to magnetometers, used for measurements of geomagnetically induced currents (GICs) in a high voltage (HV) networks. The buck-boost dc-dc converter's topology is investigated with software Cadence OrCAD. The input voltage V_{in} is expected to vary between 8 V and 15 V. The presented converter ensures stable dc output voltage V_{out} of 12 V. The power supply circuit is implemented on PCB. Efficiency as function of input voltage is investigated. The maximum achieved efficiency result of the designed circuit is equal to 85.7 %.**

Keywords – **differential magnetometer measurements; efficiency; geomagnetically induced currents; power supply circuit.**

I. INTRODUCTION

The geomagnetically induced currents (GICs) are phenomena which are generated by the interaction between the solar event and magnetic field of the earth [1]. GICs flow through HV power transmission networks, because they have low resistance. This leads to negative effects to the grounded high voltage transformers, such as saturation and heating.

During the geomagnetic storm time-varying magnetic fields are generated [2]. Respectively, those magnetic fields induce electric fields, which lead to GICs [3]. Large GICs, which can be induced during the extreme geomagnetic storm, could damage the transformers in the substations leaving large geographical and population areas without electricity [4]. In modern life such catastrophic event will lead to huge economic and security consequences.
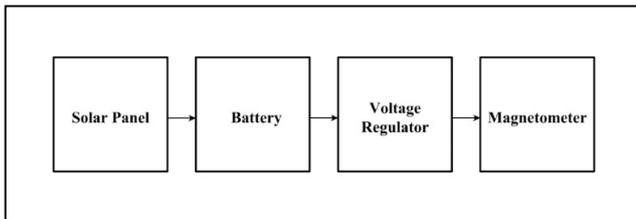
Fig. 1. The simplified block circuit of the components used in the differential magnetometer system.

The most accurate and direct method to measure GICs is by using Hall effect probe clamped to earth of the transformer [1]. The limitation of this approach is that Hall effect probes are very expensive. Using indirect measurements GICs can be modeled and evaluated [5]. Differential magnetometer method (DMM) is cheaper and widespread used method to estimate the effect of space weather over the HV network [5].

In DMM two magnetometers at different points are used to estimate values of GICs. The measurement systems in DMM method are powered by batteries, which are recharged by solar panels [2]. The simplified block circuit diagram of the components used in the differential magnetometer system is illustrated in Fig. 1 [2], [6]. The measurement system consists of a solar panel, battery, voltage regulator and magnetometer. The high efficient switching-mode dc-dc converter can save battery energy.

In this paper, power supply circuit design is presented, to ensure the desired energy of the magnetometers used in DMM method. The variation of the input voltage is expected to be in the interval between 8 V and 15 V. The dc-dc converter delivers stable output voltage to the load, which is equal to 12 V [7]. The power supply circuit is modeled using software Cadence OrCAD. The layout design of the investigated dc-dc converter is realized. The circuit is implemented on PCB board with dimensions 130mm X 80mm, respectively.

The short theory is discussed in Section II. The DMM method using to estimate GICs is described in Section II*A*. The basic theory of the analyzed converter is discussed in Section II*B*. In the Section III are presented power supply circuit investigated with Cadence OrCAD, the layout design of the converter implemented on PCB and the measurement results respectively. The maximum efficiency value of the presented circuit is 85.7 % at output power P_{out} equal to 3 W.

II. THEORY

In this section of the paper is discussed differential magnetometer method used for measurements of GICs and the theory of the standard buck-boost dc-dc converter. The GICs are quasi-DC currents.

A. Differential magnetometer method

In the DMM two magnetometers are employed. One of the magnetometers is positioned below the HV line, while the second one is located around 200 m away [2]. The first one records the quasi-DC current, which exist due to the

geomagnetic activity, plus background magnetic field. The second magnetometer detects the natural magnetic field. Their positions are shown in Fig. 2 [6].

The GICs can be calculated using the difference between the two measurement instruments. They are flowing in power networks through the neutral to ground connection of the transformers [8]. The frequency of GICs is between 0.01 Hz to 0.05 Hz [9].
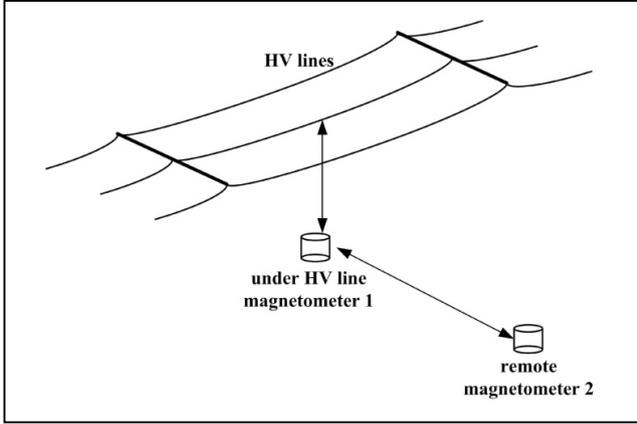
Fig. 2. The positions of the magnetometers in DMM method [6].

When GICs are measured it is assumed that they are distributed equally to the three parallel conductors in the HV high voltage power transmission networks (common mode) [8].

B. Buck-boost dc-dc converter

The basic buck-boost dc-dc converter's schematic is illustrated in Fig. 3.
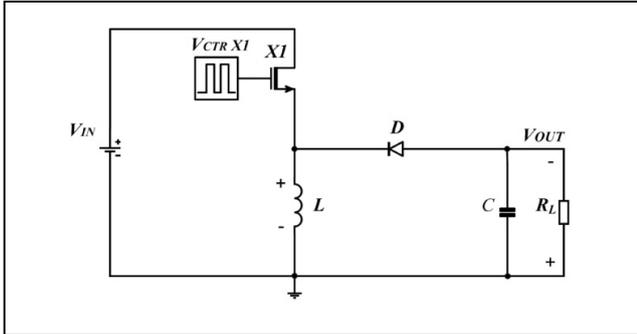
Fig. 3. Schematic of buck-boost dc-dc converter.

That dc-dc converter's topology is used when input voltage V_{in} could be smaller or higher than regulated output voltage V_{out}. When the main power NMOS transistor $X1$ is switched-on the input power is delivered to the filter inductor L. In this case the diode is reverse biased. If the transistor $X1$ is switched-off the stored energy of the filter inductor is distributed to the circuit's load.

The of duty cycle's value D determines the output voltage compared to input voltage level. The output to the input voltage ratio can be expressed by formula [10]:

$$\frac{V_{out}}{V_{in}} = D\frac{1}{1-D}.$$

(1)

The value of V_{out}, of the circuit shown in Fig. 3, has negative polarity compared to voltage V_{in}.

III. DESIGN AND INVESTIGATIONS OF BUCK-BOOST DC-DC CONVERTER

The block diagram, of power supply circuit for measurements of GICs designed with software Cadence OrCAD, is presented in Fig. 4.
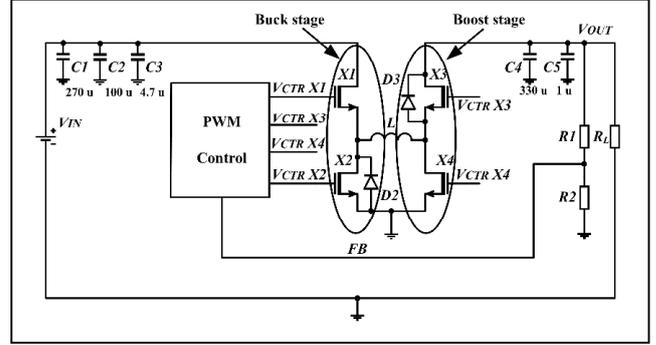
Fig. 4. The block diagram of the designed buck-boost dc-dc converter.

The dc-dc converter's power stage consists of: NMOS transistors $X1$, $X2$, $X3$ and $X4$; filter inductor L and output filter capacitors $C4$ and $C5$. The input voltage V_{in} of the circuit can be changed between 8 and 15 V, while output voltage V_{out} is 12 V.

According to the level of input voltage the power supply circuit works in buck or in boost mode of operation. The PWM control stage forms the signals, which control the power NMOS transistors.

The dc-dc converter has to deliver the desire energy to magnetometers, used for measurements of GICs, which is up to 3 W [11]. The simplified circuit model investigated with Cadence OrCAD [12], when the designed converter works in buck mode of operation, is shown in Fig. 5.
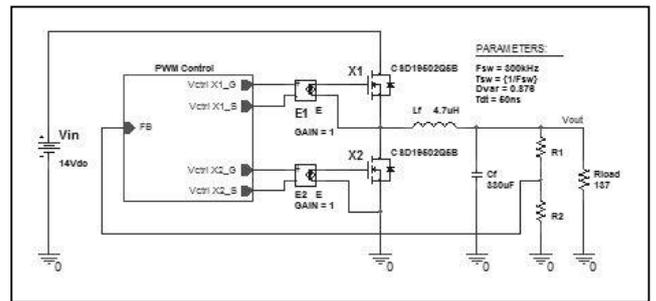
Fig. 5. The simplified circuit's model, when the dc-dc converter works in buck mode of operation, investigated with Cadence OrCAD.

In this particular case the input voltage of the modeled circuit is equal to 14 V. The PSpice models of the MOSFET transistor "*CSD19502Q5B*" of the company Texas Instruments are used in the investigations for power transistors $X1$ and $X2$. Those electronic components are chosen for presented design due to their low drain-to-source on resistance $R_{DS(on)}$.

The power losses in the MOSFET transistors $X1$ and $X2$ are divided into switching and conduction power losses [13]:

$$P_{loss,MOS} = P_{sw} + P_{cond} \,, \qquad (2)$$

The switching losses in transistor $X1$ in buck mode of operation are equal to [14]:

$$P_{sw(X1)} = \frac{1}{2} \cdot V_{in} \cdot I_{out} \cdot \left(t_r + t_f \right) \cdot f_s \,, \qquad (3)$$

where t_r and t_f are the rise and the fall times of the MOSFET transistor respectively, while f_s is the switching frequency of the dc-dc converter.

The conduction power losses P_{cond} of the MOSFET transistor are proportional to $R_{DS(on)}$ [13]. Therefore, using output transistors with low drain-to-source on resistance, the total power losses in dc-dc converters could be decreased. As a result, the overall efficiency of the whole system can be increased.
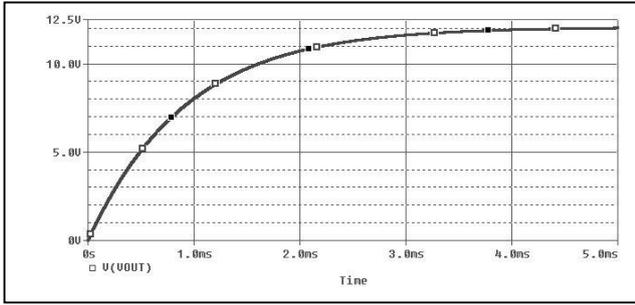
Fig. 6. The waveform of the output voltage V_{out} of the simulated dc-dc converter.

The output current I_{out} of the modeled dc-dc converter shown in Fig. 5, in this particular case of the investigation, is equal to 87 mA. The value of the load resistor R_L is chosen in such a way that the average output power is equal to approximately 1 W. Using the resistors $R1$ and $R2$, which are equal to 280 kΩ and 20 kΩ respectively, is set the output voltage of the circuit. The switching frequency of the power supply circuit is 300 kHz. The waveform of the output voltage V_{out} of the simulated converter, presented in Fig. 5, is shown in Fig. 6.
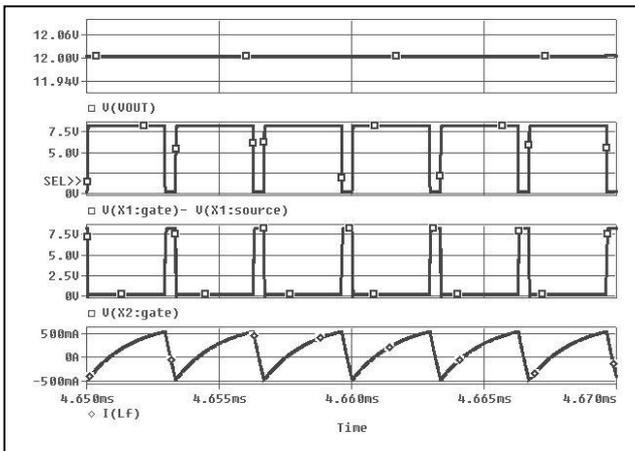
Fig. 7. The waveforms of the dc-dc converter's voltage V_{OUT}, V_{GS1}, V_{GS2}, and the inductor current I_L.

The results presented in Fig. 6 shows that, the output voltage of V_{out} of the modeled dc-dc converter, which work

in the buck mode of operation, is stabilized at 12 V after 4 ms.

The waveforms of the output voltage V_{out}, the drain-source voltages V_{GS1} and V_{GS2}, which regulate the mode of operation of the transistors $X1$ and $X2$ respectively, and the inductor current I_L are shown in Fig. 7.

The PCB layout of the power supply circuit is designed with software Cadence OrCAD. The "TOP" layer of the dc-dc converter's topology is shown in Fig. 8. The physical sizes of the power supply circuit are 130mm X 80mm.
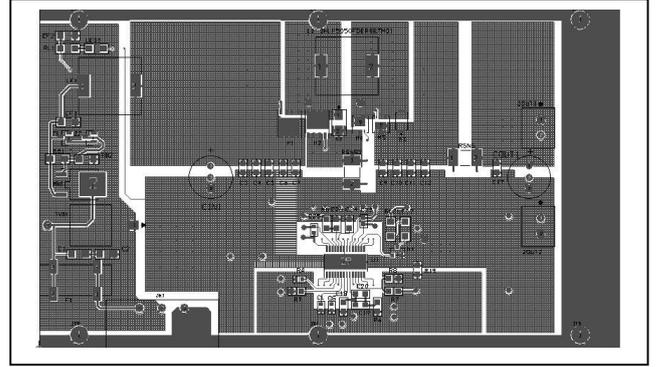
Fig. 8. The PCB layout of the power supply circuit.

The zoomed layout view of the "TOP" layer, which includes the power stage of the designed dc-dc converter, is shown in Fig. 9.
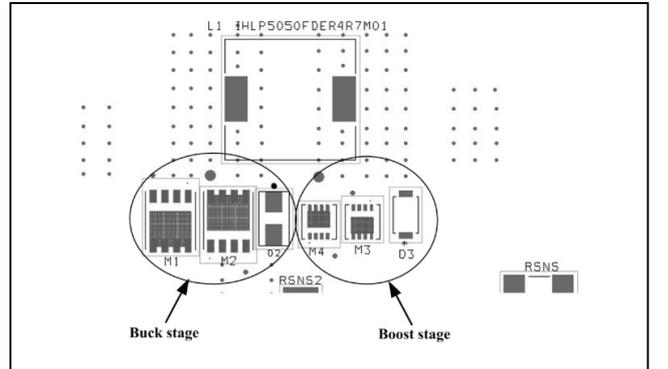
Fig. 9. The zoomed layout view of the power stage of the designed dc-dc converter.

The filter inductor L together with the MOSFET transistors and diodes, which form the buck and boost stage of the dc-dc converter respectively, can be seen in the picture presented in Fig. 9.

The power supply circuit presented in this paper is implemented on PCB. The efficiency η of the buck-boost dc-dc converter is evaluated as a function of input voltage. The received results, at output power P_{out} equal to 1 W, are given in Table 1.

The efficiency of the circuit is calculated by formula [10]:

$$\eta = \frac{P_{out(avg)}}{P_{in(avg)}} = \frac{V_{out(avg)} \cdot I_{out(avg)}}{V_{in(avg)} \cdot I_{in(avg)}} \,, \qquad (4)$$

where $P_{out(avg)}$ and $P_{in(avg)}$ are the average values of the output and the input power of the circuit. The results presented in

Table 1 show that, the maximum efficiency η at P_{out}=1 W is equal to 82.6 %.

V_{IN} [V]	Efficiency [%]
8	78
9	81.5
10	79.6
11	80.8
12	82.6
13	81.7
14	82
15	76.3

The received results shown in Table 1, are graphically presented in Fig. 10, together with the case when the output power of buck-boost dc-dc converter is equal to 3 W. The illustrated graphs show that the efficiency of the power supply circuit is about 3 % higher when P_{out}=3 W, compared with the results when P_{out}=1 W.
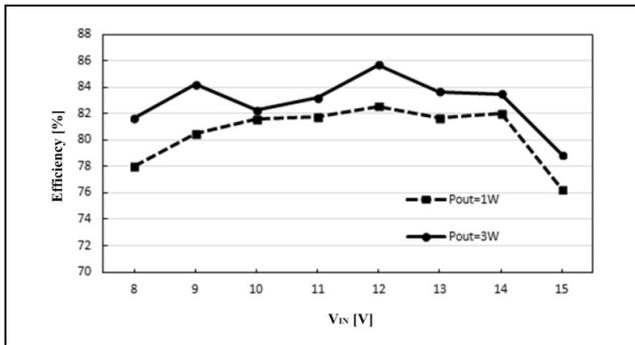
Fig. 10. Efficiency as a function of V_{in} at P_{out}=1 W and P_{out}=3 W.

The measurement results show that, maximum efficiency of the dc-dc converter implemented on PCB is equal to 85.7 %, when P_{out}=3 W.

IV. CONCLUSION

A power supply circuit designed with software Cadence OrCAD is presented in this paper. The output voltage V_{out} of the buck-boost dc-dc converter is equal to 12 V, while the input voltage V_{in} is in the range between 8 and 15 V. The PSpice models of MOSFET transistors "$CSD19502Q5B$" of the company Texas Instruments are used in the investigations. The circuit is suitable for measurements of GICs in power networks. The designed dc-dc converter is implemented on PCB. Efficiency as a function of input voltage of the circuit is investigated. The measurement results show that, maximum efficiency of the dc-dc converter implemented on PCB is equal to 85.7 %, when P_{out}=3 W.

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