Power Losses in High Frequency Switching-Mode Regulator for Integrated Circuit Applications

Tihomir Brusev

Abstract – **In this paper an integrated buck switching-mode regulator for modern communication portable devices is presented. The switching frequency f_s of the circuit, designed on AMS 0.35 µm technology with Cadence, is equal to 200 MHz. Power losses sources in CMOS IC are discussed and evaluated as a function of circuit's parameter. The energy dissipations and efficiency of the designed converter are investigated as a function of the load current I_L.**

Keywords – **Power losses, CMOS technology, Switching-mode regulator, Cadence.**

I. INTRODUCTION

Today the increasing of the time between two consecutive battery charges of the modern telecommunication portable devices such as smartphones, is a challenge for the designers. The key is the minimization of power losses of the mobile system's building blocks. The traditional CMOS (Complementary Metal–Oxide–Semiconductor) technology is good choice for low power integrated circuit (IC) design, because energy dissipation could be decreased compare to the other integrated circuit technologies [1]. In the new Fifth-Generation (5G) wireless communications standard, the transmitter's power amplifier (PA) have to work with high peak to average power ratio (PAPR), such as the previous Long-Term Evolution (4G LTE) standard [2], [3]. The PA is the most energy consuming block of the transmitter.

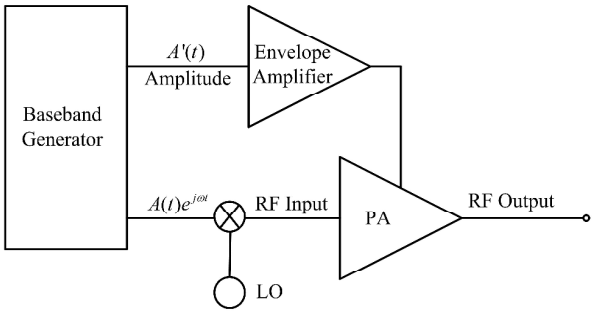

Fig. 1. Block diagram of envelope tracking power amplifier system (ET PA).

The envelope tracking (ET) technique is used to increase power amplifier efficiency. The design of high efficient envelope amplifier, which is part of envelope tracking power amplifier (ET PA) system, can increase the battery lifetime in the portable electronic devices [4].

Most of the energy, which is delivered to the transmitter's (PA) from envelope amplifier, is ensured by switching-mode regulator [5]. The power losses in the whole converter's system are necessary to be minimized. The block diagram of envelope tracking power amplifier system is shown in Fig. 1 [2].

This paper considers the energy dissipations in high frequency monolithic switching-mode regulator, which are suitable for modern communication standards. The power losses sources of CMOS IC are discussed in Section II. They are investigated with Cadence on AMS 0.35 µm technology as a function of power supply voltage and operating frequency. The switching-mode regulator for IC application using Pulse-Width Modulation (PWM) control is designed and presented in Section III. The switching frequency of the converter f_s is equal to 200 MHz in order to cover the large bandwidth of the transmitted RF signal.

II. INVESTIGATION OF POWER LOSSES IN AMS CMOS 0.35 µM TECHNOLOGY

The energy dissipations of the all building blocks of portable electronic devices have to be minimized in order to save battery energy. Here in this chapter the power losses sources in CMOS integrated circuit are discussed. They are analyzed and investigated for AMS CMOS 0.35 µm technology. The total losses are equal to sum of for different power dissipation sources and can be expressed by formula [6]:

$$P_{total\ power\ losses} = P_{dynamic} + P_{leakage} + P_{short-circuit} + P_{DC}\,, \qquad (1)$$

where $P_{dynamic}$ are dynamic switching power losses which which are due to charging and discharging of parasitic capacitance; $P_{leakage}$ are leakage power losses; $P_{short\text{-}circuit}$ are short-circuit losses which represent power dissipation when pull-up and pull-down CMOS networks are simultaneously switched-on; P_{DC} is DC power which CMOS circuit consume.

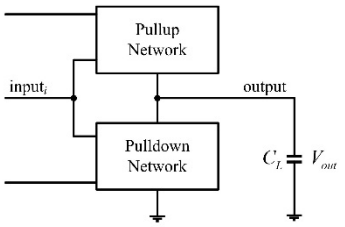

Fig. 2. Block diagram of CMOS circuit.

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The equivalent block diagram of CMOS circuit used to analyze the dynamic switching power losses is shown in Fig. 2. The major part of the total power dissipation in the CMOS integrated circuit is dynamic switching power losses. They are proportional respectively to supply voltage, the equivalent capacitance of the nodes, the switching frequency and the voltage swing of the control signal. The average value of total dynamic switching power losses in the CMOS integrated circuit is equal to [7]:

$$P_{dynamic} = f_s V_{DD} \sum_{i=1}^{N} \alpha_i C_{Li} V_{swing} , \quad (2)$$

where N is a number of nodes in CMOS circuit, f_s is the switching frequency, V_{DD} is power supply voltage, α_i is coefficient which express the average activity factor of the nodes, C_{Li} is the equivalent parasitic of the node i, V_{swing} is the voltage swing in the node i. Usually V_{swing} in CMOS IC is difference between power supply voltage and ground and dynamic switching power losses are equal to:

$$P_{dynamic} = \alpha_i f_s C_{Li} V_{DD}^2 , \quad (3)$$

The leakage current is the current which is conducted in the real CMOS integrated circuit even when the transistor is switched-off, because the transistor is not ideal component. The main sources of the leakage current in IC are weak inversion, drain-induced barrier lowering and gate oxide tunneling [8]. When the MOSFET transistor works in weak inversion the value of gate-source voltage V_{GS} is smaller than threshold voltage of the transistor. The current which is flowing in this mode of operation is called subthreshold current [9].

The drain current characteristic I_D as function gate-source voltage V_{GS} is investigated using Cadence on AMS CMOS 0.35 μm process and presented in Fig. 3.

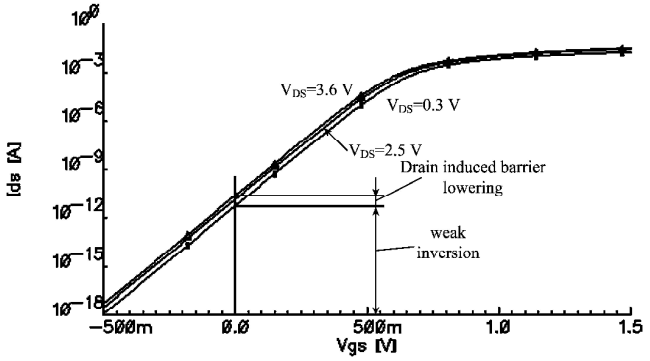

Fig. 3. Drain current I_D as a function of V_{GS}, for three different values of V_{DS}, when "*nmosrf*" transistor work in weak inversion.

For the simulation is used NMOS transistor type "*nmosrf*", respectively with sizes W/L equal to 200/0.35 [μm]. The goal of this investigation is analysis of transistor's power losses when they work in the weak inversion mode of operation. With the development of new IC technologies, the reduction of the supply voltages of circuit's building electronic blocks is growing at a faster rate than the decrease of the threshold voltages of the transistors. This leads to increased leakage currents and the power losses caused by them cannot be ignored. The characteristic of drain current I_D as a function of V_{GS}, which is illustrated in Fig. 3, is simulated respectively for three different drain-source voltage: V_{DS}=0.3 V, V_{DS}=2.5 V and V_{DS}=3.6 V. As can be seen from the presented results, with decreasing of V_{DS} subthreshold leakage current goes down. The effect of the drain voltage over the threshold of the MOS transistor is called drain induced barrier lowering [8]. A significant part of the subthreshold leakage current in submicron MOSFETs could be due to the drain induced barrier lowering, which leads to increasing of power losses in CMOS IC.

The short-circuit power losses is another source of energy dissipation in CMOS IC. There is a small time interval when both pull-up and pull-down networks, which are illustrated in Fig. 2, are switched-on simultaneously. Therefore short-circuit current flows between power supply and ground. The reason is that the rise and the fall time of the input signal are not zero. The significant short-circuit power losses can be received if the rise and fall time of the input signal are larger compare to the rise and fall time of the output signal.

TABLE I
THE TOTAL POWER LOSSES IN AMS CMOS 0.35 μM TECHNOLOGY AS A FUNCTION OF SUPPLY VOLTAGE V_{DD} AT DIFFERENT VALUES OF OPERATING FREQUENCY

f [MHz]	P_{losses} [mW]	P_{losses} [mW]	P_{losses} [mW]	P_{losses} [mW]
	V_{DD}=1V	V_{DD}=2V	V_{DD}=2.5V	V_{DD}=3.6V
50	0.7	3.13	5.13	31.6
100	1.4	6.3	10.25	37
150	2.1	9.4	15.4	46.07
200	2.8	12.5	20.5	108
250	3.5	15.7	25.63	134

In the new 5G wireless communications standard the RF signal bandwidth is increased [10]. On the other hand envelope tracking bandwidth has to be at least twice higher compare to the RF signal bandwidth [2].

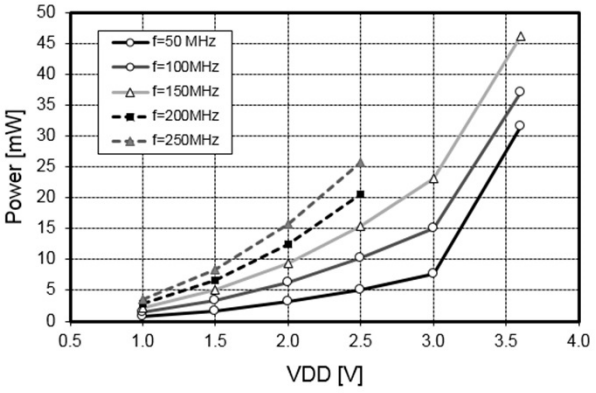

Fig. 4. The total power losses in CMOS IC circuit as a function of V_{DD} at different operating frequencies.

All those requirements lead to high switching frequency f_s of the switching-mode regulator [11]. As can be seen from formula (3), with increasing of f_s the dynamic switching

power losses will go up. Respectively the result is efficiency degradation of switching-mode regulator. Therefore it is important to estimate the total power losses in CMOS IC for high operating frequencies.

The Cadence software on AMS CMOS 0.35 μm process is used for analysis. The total power losses in CMOS integrated circuit are evaluated as a function of power supply voltage V_{DD} at different operating frequencies. The received simulation results are presented in Table 1. The operating frequencies used in the investigation are in the range from 50 MHz to 250 MHz.

The simulation results shown in Table 1 are graphically presented in Fig. 4. As can be seen from the picture, when the power supply voltage is decreased the total energy dissipations go down. This is explained by the quadratic relationship that exists between the dynamic switching losses and the supply voltage. The dynamic switching losses are a dominant part of total power losses when circuits operate in active mode. The simulation results presented in Fig. 4 prove that energy dissipations in CMOS IC are increased at higher operating frequencies.

III. High Frequency Switching-Mode Regulator Designed on AMS CMOS 0.35 μm Technology

Switching-mode buck regulator for modern communication standards is designed with Cadence on AMS CMOS 0.35 μm technology.

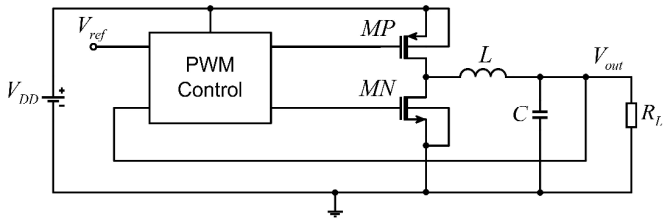

Fig. 5. The block diagram of switching-mode buck regulator.

The simplified block diagram is presented in Fig. 5. The switching-mode buck regulator used PWM control.

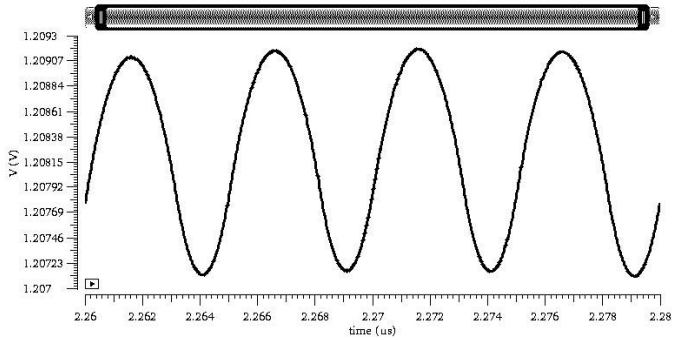

Fig. 6. The waveform of the output voltage V_{out} of the switching-mode buck regulator.

The resistance R_L represents the current load of RF power amplifier in ET PA system shown in Fig. 1. The control circuit is formed by bandgap voltage reference, error amplifier, ramp generator and buffer. The power supply voltage is equal to 3.6 V.

The waveform of the output voltage of the converter V_{out} is shown in Fig. 6. In this particular case the average value of V_{out} is equal to 1.2 V, while the load current is equal to 48 mA. The schematic of error amplifier is presented in Fig. 7.

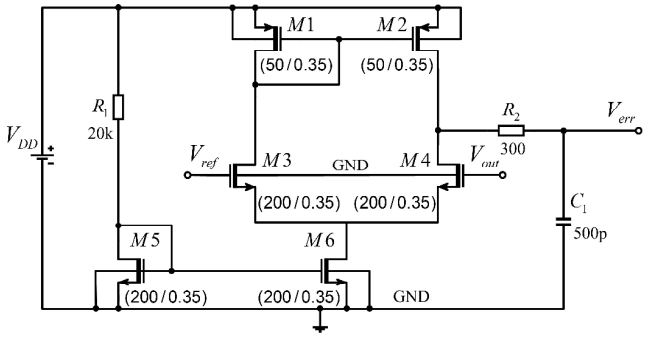

Fig. 7. The schematic of error amplifier.

The simulation results received in Cadence Analog Design Environment tool are presented in Fig. 8. The switching frequency f_s of the buck regulator is equal to 200 MHz. The high value of f_s is chosen, because the bandwidth of the RF transmitted signal in the new communication standards is large.

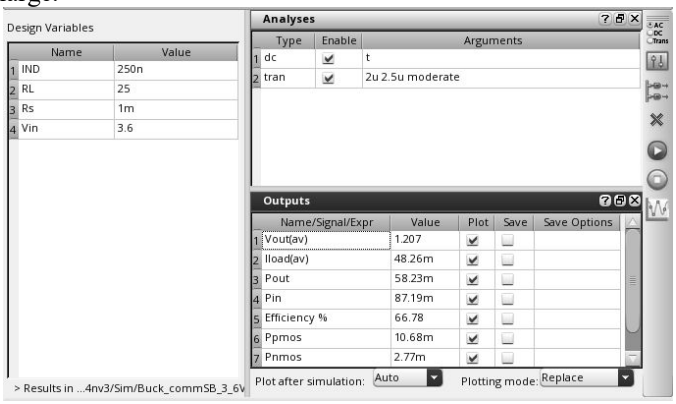

Fig. 8. Simulation results received in Cadence Analog Design Environment when the load current is equal to 48 mA.

As can be seen from Fig. 8 the efficiency of the switching-mode regulator, when load current is 48 mA, is equal to 66.78%. The efficiency of the whole buck converter system is calculated as a ratio between average values of the output P_{out} and the input P_{in} power.

$$\eta = \frac{P_{out}}{P_{in}}, \tag{4}$$

The total energy dissipation in the both MOS transistors, which are part of the power stage of the buck switching-regulator, is 13.45 mW. The power losses in PMOS transistor *MP* are respectively 10.68 mW, while in NMOS transistor *MN* they are equal to 2.77 mW. This is 46.44% of the total power losses in the whole converter system.

The obtained results of energy dissipation in power MOS transistors and efficiency of the buck switching-mode regulator as function of load current I_L, are presented in

Table II. The maximum efficiency of the buck switching-mode regulator is equal to 67.34%. The biggest parts of the energy dissipation in the switching-mode regulator system are respectively in power PMOS (*MP*) and NMOS (*MN*) transistors.

TABLE II
POWER LOSSES OF MOS TRANSISTORS AND EFFICIENCY OF BUCK SWITCHING-MODE REGULATOR AS A FUNCTION OF I_L

	I_L=40 [mA]	I_L=48 [mA]	I_L=60 [mA]	I_L=80 [mA]	I_L=120 [mA]
P_{out} [mW]	48.65	58.23	72.6	96.49	143.9
P_{in} [mW]	74.85	87.19	107.8	145.3	233.6
P_{NMOS} [mW]	2.09	2.77	4.25	7.28	17.29
P_{PMOS} [mW]	8.352	10.68	15.07	24.94	56.36
$P_{MOS,tot}$ [mW]	10.44	13.45	19.57	32.22	73.65
Eff. [%]	65	66.78	67.34	66.43	61.59

In Fig. 9 are graphically presented simulation results of the power losses in PMOS (*MP*) and NMOS (*MN*) transistors as a function of the load current I_L. At higher load currents is increased the impact of the losses in the power MOS transistors over the total energy dissipations of the converter's system.

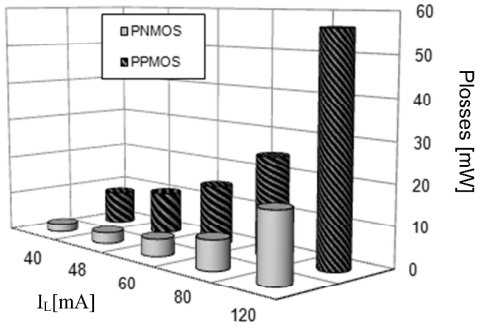

Fig. 9. Power losses in PMOS (*MP*) and NMOS (*MN*) transistors of the switching-mode regulator, as a function of load current I_L.

The investigation shows that power losses in the both MOS transistor (*MP* and *MN*) vary between 40% and 82% of the total power losses in the whole converter system. Those results are achieved when the load current I_L of the buck switching-mode regulator is changed from 40 mA to 120 mA.

IV. CONCLUSION

In this paper a buck switching-mode regulator suitable for modern communication portable devices, designed with Cadence on AMS 0.35 µm technology is presented. The switching frequency f_s of the converter, which is equal to 200 MHz, is high in order to cover the large bandwidth of the transmitted RF signal. The power losses sources in CMOS IC are discussed and evaluated as a function of circuit's parameter. The energy dissipations and efficiency of the designed buck converter are investigated and analyzed. When the load current of switching-mode regulator is changed from 40 mA to 120 mA, the losses in power MOS transistors vary between 40% and 82% of the total power losses in the whole system.

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