IC Implementation of Subthreshold Current Temperature Independent Power-on-Reset Circuit

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***Abstract**: Power-on-reset (POR) circuit with low current consumption, temperature independent has been developed. The circuit contains several sub-circuits such as self-biased current generator, analog comparator with hysteresis, Schmitt trigger and supply filter. Two nano amp currents with positive temperature coefficients (PTAT), generated from self-bias current generator – one applied on resistor, and one applied on two diode string connected to the supply, are compared at the two inputs of analog comparator. By controlling the resistance value and the multiplier of the current bias, the low-to-high threshold is precisely settled. This also allows to control the temperature behavior of the voltage on the inputs of the comparator and make POR threshold levels less temperature dependent. A hysteresis has been added in the analog comparator, which is used to set the high-to-low POR threshold and to prevent the circuit from wrong triggering and oscillations. This circuit is designed in TSMC 0.18 μm technology kit. The simulations are performed at schematic level only, with 5V supply voltage*

Keywords: Power-on-Reset (POR), temperature independent, self-bias current generator.

1. INTRODUCTION

POR circuits are always part of both analog and digital power management circuit. The main function is to detect supply voltage, which takes time to settle, whether it has reached its steady-state value. During this settling time of the supply, the behavior of the supplied circuits cannot be predicted, so reset signal is needed for enable [1].

The primary requirement for such circuit is that the output signal of the POR block should hold all circuits in reset state, until the supply voltage reaches safe operation level for those circuits. This implies that threshold levels for turning on and off the POR circuit should be accurately set and weakly dependent from process and mismatch and temperature variations. Power consumption and size of the circuit are also an enormous concern.

There are various ways to realize POR circuits. One simple circuit can be made by comparing two voltages in analog comparator – one from stable band-gap reference and one from the target in ratio of the suppling voltage. The main disadvantage in such structure is the higher current consumption and area.

In some chip applications nowadays, there are low current modes, or modes in which the chip has to sleep (hibernate), but the digital has to store some data, while not making reset.

2. CIRCUIT DESIGN

In this paper we propose a Power on reset circuit, which has current consumption in range of nano amps and small temperature dependence of the threshold levels. The circuit provides precise control of the low-to high and high-to-low threshold levels. This circuit is relatively independent from the technology of the die, in which it is going to be implemented, because all the biases required for the correct operation of the POR circuit, are created in the internal self-biased circuit and current mirrored.

Figure 1 depicts the block diagram of the proposed POR circuit. It consists of self-bias current mirror with start-up circuit, analog comparator with hysteresis, Schmitt trigger, and supply voltage filter. All devices used in the circuit design are 5 V devices in 0.18 μm TSMC CMOS technology, except for one pmos 2 V device used as resistor.

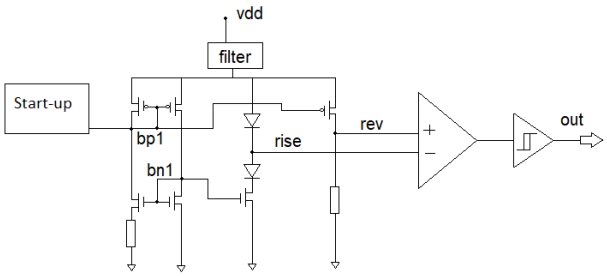


Fig. 1. Power on reset circuit block level view.

The self-biased circuit in Figure 1 generates currents in the order of couple of nano Ampers. It equips with its own start-up unit.

The analog comparator in Figure 1 compares two node voltages "rev" and "rise" – "rise" is voltage defined by the voltage drop across two diodes and the current from the self-bias generator, while "rev" is defined by the resistor R1 and the current flowing through it. The type of the resistor is chosen so that the slope of the temperature behavior of the node "rev" is control compensated.

The two voltages are compared in analog comparator. The hysteresis is realized in the analog comparator. The output of the comparator is applied at the input of Schmitt trigger circuit, which forms rapid fronts of the output signal of the POR.

In Figure 2 it is shown the schematic view of the proposed Power on Reset circuit drawn in Cadence environment.

The operating principle is given in Figure 1. Self-biased circuit is generating the bias currents needed for the whole circuit. The currents value is the order of couple of nano amperes. The resistor is P+ poly type. Start-up circuit generates start-up pulse node "st" in Figure 2. as shown in Figure 4. and is securing that the self-biased current mirror is starting up properly in all corners and conditions. Then comparator is comparing two node voltages "rise" and "rev".

The "rise" node is following the supply voltage, with voltage drop, formed by one diode connected 5v pmos device (its gate is shorted to their drain), and the current flowing through the diodes is from the self-bias. During start-up this node is following the supply ramp minus one diode threshold voltages.

The voltage on "rev" node is formed by current from self-bias flowing through resistors string, made by two pmos transistors used as resistors (their gate is connected to ground through protection resistor),

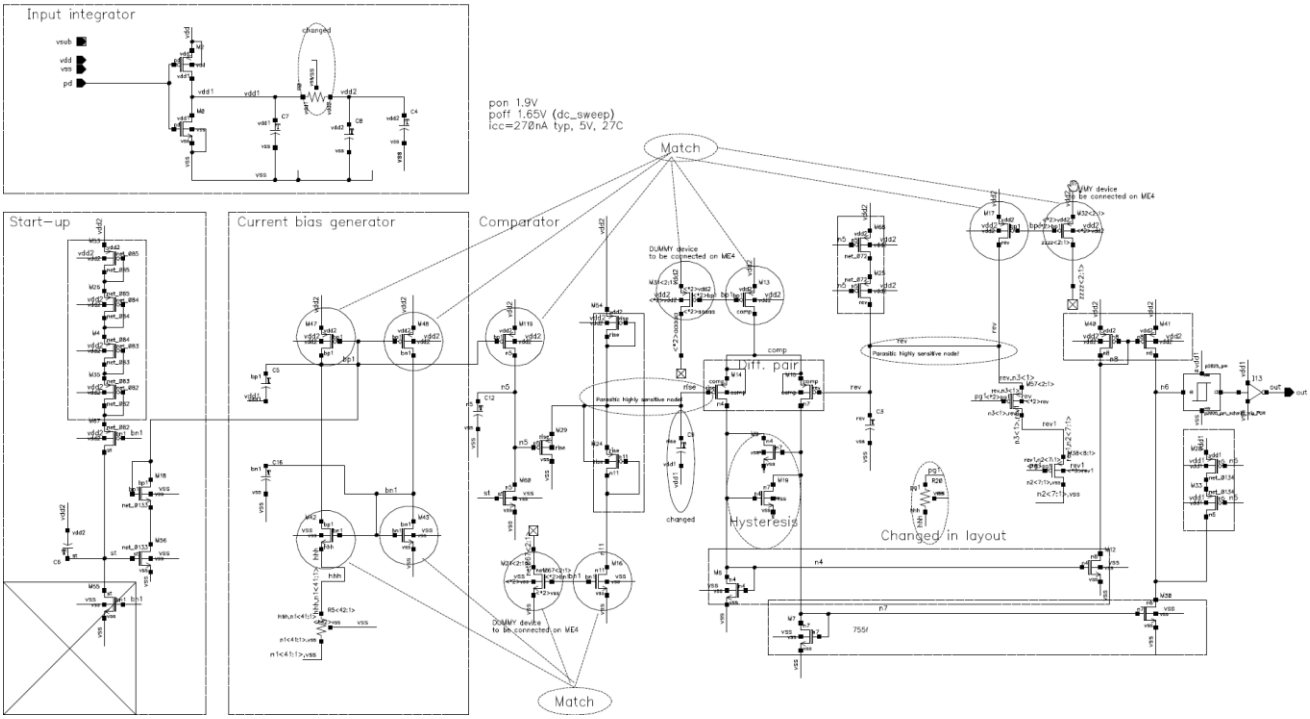


Fig. 2. Full schematic view of proposed Power-on-reset circuit.

so that the voltage is proportional to the current and the resistor value. In Figure 2 the first one M57 is with 5 V type and the second one M38 is 2 V type. All the devices used in the proposed circuit are at 5 V with one device at 2 V; all of them are in TSMC 0.18 µm technology.

The calculations for the sizes of the resistors and the multiplier of the bias, are made for the desired Low-to-High threshold level. The current value is chosen to be 1000 nA. For the proposed POR circuit it is the desired threshold level is 1.9 V typical. The formula for the threshold is:

$$Vth = \left(\frac{I}{\mathrm{R}}\right) 1.9\mathrm{V} = \left(\frac{100nA}{\mathrm{R}}\right) \qquad (1)$$
$$\mathrm{R} = 19\mathrm{M}\Omega$$

It should be noted that the voltage on the 2 V device should be below 2 V in every corner, so the sizing for the two pmos transistors used as resistors should be carefully done.

By defining the hysteresis of the circuit (Figure 2 transistors M9, M19) the high-to-low threshold level is defined. For this POR the hysteresis is set 250 mV typical, so high-to-low level is

$$1.9\ \mathrm{V} - 0.25\ \mathrm{V} = 1.65\ \mathrm{V}.$$

The idea with the temperature compensation in the two nodes is the following: both "rev" and "rise" node voltages have positive temperature coefficients, due to the same type of self-bias currents used. When temperature is raising the voltage on the "rev" node is raising as well, so as the "rise" voltage. Because "rise" voltage is following the supply with voltage drop, it will start faster at hotter temperatures. The voltage on "rev" will increase at hot temperatures. This will allow "rise" to cross earlier over time "rev" node, and this will compensate the increased voltage of the "rev" node like shown in Figure 3. At cold temperatures the effect will be the opposite – "rise" will start slower, due to the increased threshold of the pmos diode and the voltage on "rev" will be less.

Note that the resistors in the "rev" node are pmos transistors connected as resistors and depending on their characteristic are used also to adjust the slope of the temperature behavior of the voltage.

During start-up, when "rise" voltage crosses "rev" voltage the comparator output is pulled down by transistor M30 (Figure 2). Then the Schmitt trigger output follows and goes down. There is inverter at the output to form the POR output logic level.

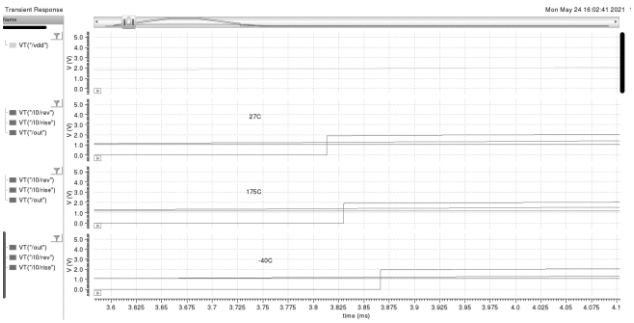


Fig. 3. Transient start-up behavior over temperature

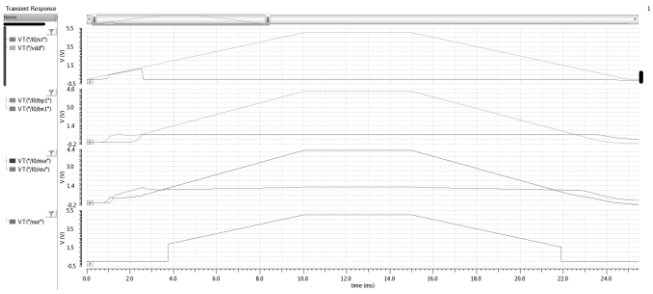


Fig. 4. Nominal transient start-up – 10 ms ramp up time and 10ms ramp down time

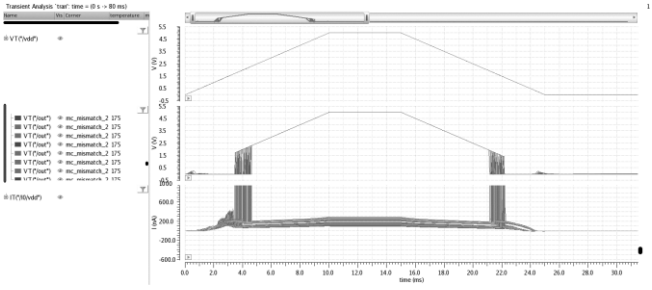
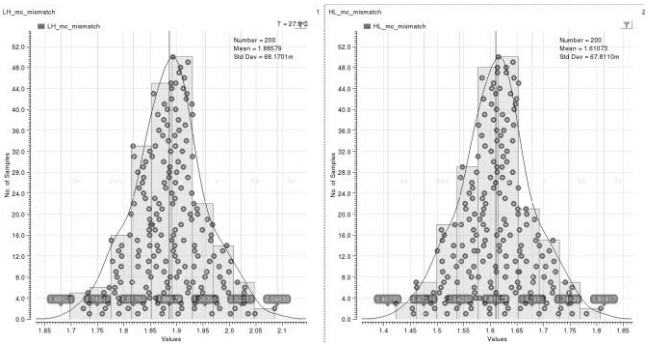


Fig. 5. Transient start-up over Monte Carlo process and mismatch for tree temperatures -40, 27, 175 C



a) b)

Fig. 6. Monte Carlo analysis at 175 C for the Low-to-high a) and High-to-low b) threshold levels

3. SIMULATION AND EXPERIMENTAL RESULTS

Figures 5 and 6 show Transient Monte Carlo process and mismatch simulation results, when the supply voltage ramps from 0 to vdd (5 V). The summarized data is in Table 1. It is shown that the achieved total deviation from the typical values is around 200 mV up and 200 mV down. The current consumption is maximum 290 nA worst case, which is quite small compared to other POR architectures. The major drawback of this architecture is that the POR circuit has delay, which if there is specification for fast start-up of the chip (less than 100 μs until the POR release), could potentially be a problem.

Table 1. Monte Carlo Process and mismatch transient simulation results for treshold levels, hysteresis and current consumption

Name	Description	Min.	Typ.	Max.	Unit
LH	Low to high threshold voltage	1.7	1.9	2.23	V
HL	High to low threshold voltage	1.42	1.65	1.89	V
hyst	Output hysteresis	150	250	350	mV
Ivdd	Current consumption	200	270	390	nA

In Figure 7 it is shown the block layout view of the proposed POR circuit. The length on the X axis is 145 μm, while on the Y axis is 190 μm. This is the total area occupied by the proposed POR circuit with the input filter and the resistors.

4. CONCLUSION

In this paper a temperature independent power on reset circuit with subthreshold current is presented. Achieved is a total deviation of ± 200 mV with small current consumption of less than 290 nA. With little modifications of the technology the architecture could be transferred and developed on different technology as well.

On schematic level the circuit shows promising simulation results, which prove it to be with very minor temperature dependence and very little current consumption. The developed POR structure is independent from other electrical blocks in the die, in which it is implemented, because all the voltages needed for the circuit to work properly are generated in inside the block.

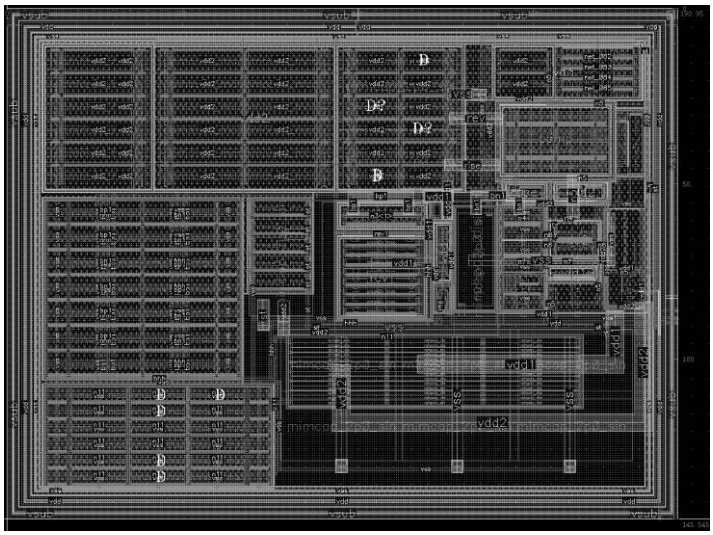


Fig. 7. Block layout view of the POR circuit.

The proposed structure is appropriate for low current consumption applications or low current working modes.

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