A Neural Network with HfO_2 Memristors

Stoyan Kirilov, Ivan Zaykov

***Abstract* — In the last twenty years, the neural networks are under intensive analyses. One of the main ideas of the scientists is to partially replace some of their CMOS-based elements by memristors. Memristors are preferred for application due to their memory effect, low power consumption and nano-size dimensions. The purpose of this paper is to propose an analysis of a feed-forward neural network with HfO_2 memristor-based synapses for XOR logic function emulation. The considered network uses synaptic devices with a memristor, resistor and a differential amplifier. The proposed synaptic scheme can ensure positive, zero and negative synaptic weights. For the neural network analysis several classical and modified HfO_2 memristor models are used. The network is successfully tested in LTSPICE. The occurrence of convergence problems is reduced by replacing the standard step function in the models by its smooth and differentiable analogue. The capability of the modified models for operation in complex schemes is proven.**

***Index Terms* — neural network, memristor synapse, hafnium dioxide, memristor model, step-like logistic function**

I. Introduction

The artificial neural networks are under intensive analysis in the recent fifteen years owing to their widespread applications in pattern recognition, signal processing, object classification and many others [1], [2], [3]. Both software and hardware realizations are used in many technical and scientific fields [2], [4]. The main constructive elements of the neural networks – synapses, neurons, and axons, are realized in hardware based on the present Complementary Metal Oxide Semiconductor (CMOS) technology [5], [6]. One of the main trends existing in the last several years is to replace some of the CMOS-based elements in the neural networks by memristors [6]. The memristor is a two-terminal passive nonlinear element with a memory effect. It retains its instantaneous resistance after turning the power sources off [7], [8]. It is predicted by Chua in 1971 [9] and its first physical prototype is realized by Williams in the Hewlett-Packard research labs [8]. Memristors are mainly based on transition metal oxides as titanium dioxide [8], hafnium dioxide [10], [11], [12], tantalum oxide and others [13], [14]. The memristors have many promising properties – memory effect, non-volatility, low power consumption, energy efficiency, nano-scale dimensions, and a sound compatibility with the present CMOS integrated circuits technology [15], [16], [17], [18]. In the scientific literature several variants of memristor-based synapses exist [5], [17], [19], [20], [21].

The research, the results of which are presented in this publication, are funded by NIS of TU - Sofia, a funding research project in support of doctoral students Number 212ПД0021-08, session 2021 - 2022.

S. M. Kirilov is with the Department of Theoretical Electrical Engineering, Faculty of Automatics, Technical University of Sofia, 1000 Sofia, Bulgaria (e-mail: s_kirilov@tu-sofia.bg).

I. D. Zaykov is with the Department of Theoretical Electrical Engineering, Faculty of Automatics, Technical University of Sofia, 1000 Sofia, Bulgaria (e-mail: ivanzaykov@tu-sofia.bg).

There are synaptic circuits with one, two and four memristors realized using bridge topology [21], [22], [23], [24]. An advantage of the bridge schemes is their possibility for realization of positive, zero and negative synaptic weights. Another solution is a single-memristor synapse, and a scheme based on anti-series memristor circuit with two memristors [22], [23]. A synaptic circuit with two memristors and operational amplifier is also existing [24], [25]. The main purpose of the present paper is to propose a single memristor synaptic scheme having the possibility to realize positive, zero and negative synaptic weights [26]. In this sense a schematic with a memristor and resistor based on a current divider and a comparator with operational amplifier in LTSPICE is proposed in the present paper. The considered memristor-based synapse is successfully applied in a simple neural network for XOR function emulation.

The rest of the paper is organized as follows. In the next section a description of several commonly used standard and modified hafnium dioxide memristor models is made. Section 3 represents the proposed memristor-based synaptic circuit. The analysis of the considered neural network for XOR emulation is presented in Section 4. The final Section 5 concludes the paper.

II. Hafnium Dioxide Memristor Models – a Review

The hafnium dioxide memristor nanostructure is presented in Fig. 1. It has two terminals – top electrode and bottom electrode, respectively [10], [15]. The length of the memristor is denoted by *D*. The top region is doped by oxygen vacancies, and it has a length denoted by *w*.

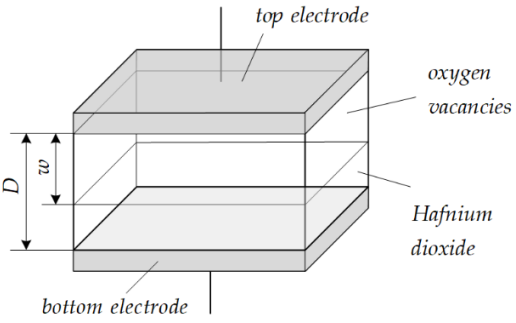

Fig. 1. Hafnium dioxide based memristor nanostructure.

The state variable *x* of the memristor element is defined as a ratio between *w* and *D* [10]:

$$x = \frac{w}{D}. \tag{1}$$

The equivalent resistance of the memristor *M* is a state-dependent one and it is expressed as follows [10], [15]:

$$M(x) = R_{ON}x + R_{OFF}(1-x). \tag{2}$$

https://doi.org/10.47978/TUS.2021.71.01.006

where R_{ON} is the ON resistance state and R_{OFF} is the OFF-resistance state of the memristor, respectively.

The state differentiable equation of the memristor relates the time derivative of the state variable x and the current i (or the voltage v). A constant dependent on the memristor physical parameters and a window function for limitation the state variable in the range (0,1) are usually applied in the right-hand side of the state equation [10]. Follows the basic hafnium dioxide memristor models and their description.

A. *Standard Hafnium Dioxide Memristor Model with activation thresholds [10]*

According to this model [10] the state differential equation of the hafnium dioxide memristor is [10]:

$$\begin{cases} \dfrac{dx}{dt} = \dfrac{v}{v_{tp} \cdot t_{swp}}, \ v \geq v_{tp} \\ \dfrac{dx}{dt} = -\dfrac{v}{v_{tn} \cdot t_{swn}}, \ v \leq v_{tn} \\ \dfrac{dx}{dt} = 0, \ v_{tn} < v < v_{tp} \\ v = \left(R_{ON} x + R_{OFF}(1-x)\right) i \end{cases} . \quad (3)$$

where v_{tp} and v_{tn} are the positive and the negative activation thresholds, respectively, t_{swp} and t_{swn} are the OFF to ON and the ON to OFF switching times of the memristor. System (3) completely describes the considered model. This memristor model is simple for realization. An advantage of this model is the lack of window function which sometimes leads to jumping the state variable outside the previously defined physical interval (0, 1).

B. *Standard Hafnium Dioxide Memristor Model with a highly nonlinear window function [10]*

This memristor model [10] contains a nonlinear window function for limitation the state variable. It is completely represented by the next system (4) [10]:

$$\begin{cases} \dfrac{dx}{dt} = \dfrac{C_{LRS}}{\Delta r}\left(\dfrac{v - v_{tp}}{v_{tp}}\right)^{P_{LRS}} \dfrac{1}{1+\exp\left(\dfrac{\Theta_{LRS} R_{ON} - M}{\beta_{LRS} \Delta r}\right)}, \ v > v_{tp} \\ \dfrac{dx}{dt} = \dfrac{C_{HRS}}{\Delta r}\left(\dfrac{v - v_{tn}}{v_{tn}}\right)^{P_{HRS}} \dfrac{-1}{1+\exp\left(\dfrac{M - \Theta_{HRS} R_{OFF}}{\beta_{HRS} \Delta r}\right)}, v < v_{tn} \\ \dfrac{dx}{dt} = 0, \quad v_{tn} \leq v \leq v_{tp} \end{cases} \quad (4)$$

where $\Delta r = Roff - Ron$, $C_{LRS} = (R_{OFF} - R_{ON})/t_{swp}$, $C_{HRS} = (R_{OFF} - R_{ON})/t_{swn}$, t_{swp}=0.1 s, t_{swn} = 0.1 s, P_{HRS} = 1.71, P_{LRS} = 1.73, β_{HRS} = 1.3, β_{LRS} = 1.3, Θ_{HRS} = 1.2, Θ_{LRS} = 1.2, v_{tp} = 0.5 V, v_{tn} = -0.5 V are parameters for adjustment the memristor model according to experimentally recorded current-voltage relationships [10]. The memristor model has a good adjustability. It could incompletely represent the nonlinear relationship between the ionic dopant drift and the applied memristor voltage. A drawback of this memristor model is its higher complexity owing to the large number of the used elementary mathematical operations.

C. *The proposed modified memristor model*

This hafnium dioxide memristor model is mainly based on the Lehtonen-Laiho memristor model [22]. The applied window function is based on a combination of two exponential logistic functions. The derived window function is a smooth and differentiable one. The proposed hafnium dioxide memristor model is completely represented by the next set of equations:

$$\begin{cases} \dfrac{dx}{dt} = a \cdot u^m \cdot \left[\dfrac{1}{1+\exp(-k \cdot x)} \cdot \dfrac{1}{1+\exp\left[k \cdot (x-1)\right]}\right] \\ i = \beta x^n \sinh(\alpha u) + \chi\left[\exp(\gamma u) - 1\right] \end{cases} . \quad (5)$$

where a, m, k, β, n, α, χ, γ are parameters for tuning the model according to experimental current-voltage relationships. The tuning procedure is realized in MATLAB environment using Simulink model of (5) and applying a procedure for parameters estimation [27], [28], [29], [30]. A methodology for minimizing the root mean square error between the experimental and simulated current-voltage characteristics is also applied for the extraction of the optimal values of the parameters [30], [31], [32], [33]. This methodology is based on altering the parameters of the memristor model in broad ranges and on a search of a global minimum of the cost function which in this case is the root mean square error between the i-v relationships. The derived values of these parameters are: β=150 μA, α=3.55 V^{-1}, χ=50 μA, γ=0.07 V^{-1}, a=3.34, k=100, m=5, n=5. The proposed memristor model with the optimal values of its parameters is analyzed in MATLAB [30] and LTSPICE environment and compared to several existing and modified models [30], [31]. A good agreement between the state-flux and current-voltage relationships is derived. Follows the derived basic characteristics for a state near to a hard-switching operating mode of the considered memristor. The time diagrams of the memristor voltage v and current i are presented in Fig. 2 for visualization the nonlinearity of the flowing current corresponding to the applied sinusoidal voltage signal.

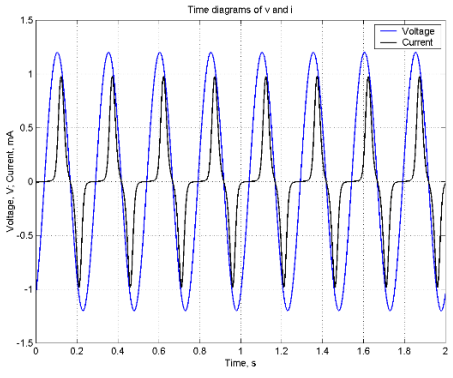

Fig. 2 Time diagrams of the memristor voltage v and current i

The time diagrams of the state variable x and the voltage are presented in Fig. 3 for visualization the range of altering of x and establishing the operating mode of the memristor. In the present case the element operates in a soft-switching mode because x is altering between 0.3 and 0.9.

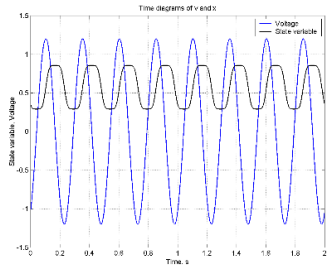

Fig. 3 Time diagrams of the state variable *x* and voltage *v*

The corresponding current-voltage relationship of the memristor is presented in Fig. 4. It is a symmetrical according to the origin curve. Additional experiments confirm that with increasing the operating frequency the *i-v* curve shrinks to a single-valued straight line which prove the correct behavior of the proposed memristor model.

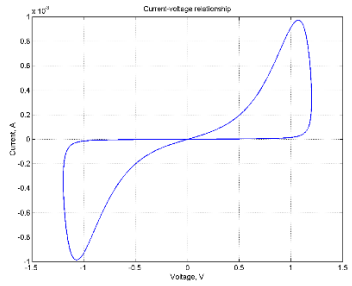

Fig. 4. Current-voltage relationship of the considered memristor

The corresponding state-flux relationship is presented in Fig. 5 for confirmation the established operating mode. In the present case the state-flux relationship is a single-valued monotonically increasing curve [28], [29].

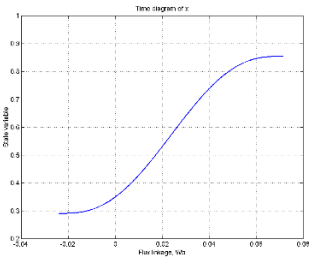

Fig. 5 State-flux relationship of the memristor element

III. A Description of the Proposed Memristor-Based Synaptic Scheme

The schematic of the proposed synapse is presented in Fig. 6 for explanation of its operation. It is based on a current divider and an operational amplifier. The current divider has two branches. The first branch contains a memristor element *M* and a resistor – R_3, and the second branch contains two resistors connected in a series - R_1 and R_2. The related currents are denoted by i_1 and i_2, correspondingly. The input voltage signal is denoted by v_{in}. The voltages across the resistors R_2 and R_3 are:

$$v_1 = \frac{v_{in}}{M + R_3} R_3 \tag{6}$$

$$v_2 = \frac{v_{in}}{R_1 + R_2} R_2 \tag{7}$$

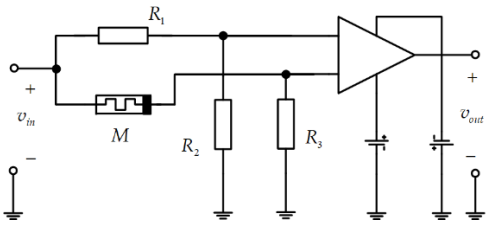

Fig. 6 A schematic of the proposed memristor-based synaptic circuit.

The output voltage of the synapse v_{out} is:

$$v_{out} = k_v \cdot (v_1 - v_2) = k_v \cdot v_{in} \cdot \left(\frac{R_2}{R_1 + R_2} - \frac{R_3}{M + R_3} \right) \tag{8}$$

where k_v is the transfer coefficient of the operational amplifier. The values of the resistors are: R_1 = 500 Ω, $R_2 = R_3$ = 1.5 kΩ. The synaptic weight of the discussed circuit *w* is dependent on the memristance *M*:

$$w(M) = \frac{v_{out}}{v_{in}} = k_v \cdot \left(\frac{R_2}{R_1 + R_2} - \frac{R_2}{M + R_2} \right) \tag{9}$$

The memristance *M* and the corresponding synaptic weight *w* are altered by external pulses affecting the memristor state variable *x*. After a simple transformation of (9) and paying attention on the fact that $R_2 = R_3$ it is obtained that if $R_1 = M$ then $w = 0$. Positive synaptic weights are derived when $M > R_1$. If $M < R_1$ then $w < 0$. By the change of the transfer coefficient of the operational amplifier, scaling of the synaptic weights is realized. The described synaptic device is successfully applied in a simple neural network for XOR logic function emulation.

IV. Analysis of the Considered Neural Network

A simple neural network for XOR logical function emulation is presented in Fig. 7. It contains two hidden layers. The first hidden layer contains four neurons and the second one is made of three neurons. The neurons in the hidden layer are with a sigmoidal activation function while the neuron in the output layer is with a linear activation function. The synaptic bonds between the neurons are memristor-based and their detailed diagram is presented in Fig. 6. The input signals are with level of one and they are previously sampled. The artificial neural network has been trained for 103 epochs with all the possible combinations of the input signals corresponding to the logical levels of zero and unity till reaching a global minimum of the root mean square error between the desired and the actual output signal.

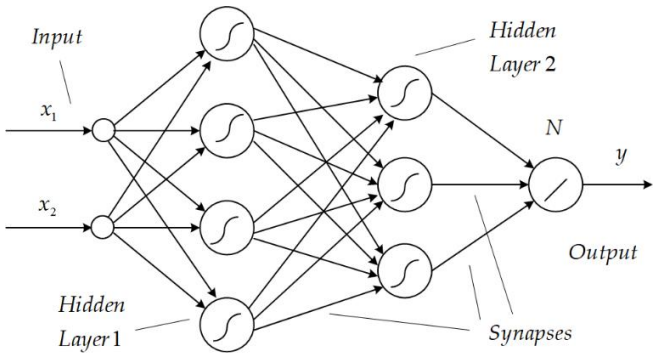

Fig. 7 A simple neural network for XOR logic function emulation

The error signal derived during the testing stage is about ten thousand times lower than the level of the input and the output signals. Finally, it was concluded that the presented neural network with memristor-based synapses correctly emulates the logical function XOR.

V. Conclusions

In this work a modified synaptic scheme based on memristor is presented and analyzed. It is based on a current divider and an operational amplifier. The current divider is made of a hafnium dioxide memristor element and a resistor. The operation of the considered synaptic scheme is founded on a comparison of the currents flowing through the memristor and the resistor. The memristor current is dependent not only on the applied input voltage but also on the memristor state variable. An advantage of the proposed circuit is its capability to produce positive, zero and negative synaptic weights. The synaptic circuit has minimal number of memristors per synapse which is it's another advantage according to several existing synaptic circuits with increased number of memristors per synapse. The considered synapse is successfully analyzed using a modified model of hafnium dioxide memristor. It is successfully applied and tested in a neural network for XOR logic function representation in LTSPICE environment. A comparison to several other memristor models is conducted as well. The applied modified memristor model is simple and appropriate for analysis of electronic circuits. Finally, it could be concluded that the analyzed memristor-based synaptic schemes successfully operate in the artificial neural network for XOR logical function representation and the modified hafnium dioxide memristor model applied in this work is suitable for analysis of complex memristor-based schemes.

References

[1] Fausett L., "Fundamentals of Neural Networks," *Prentice Hall*, 1994, ISBN 0130422509.

[2] Choi S., Sheridan P., Lu Wei D., "Data Clustering using Memristor Networks," 2015, *Nature, Scientific Reports* | 5:10492 | DOI: 10.1038/srep10492, pp. 1 – 10.

[3] La Maire B.F., Mladenov V.M. "Comparison of neural networks for solving the travelling salesman problem", *In 11th IEEE Symposium on Neural Network Applications in Electrical Engineering* 2012 Sep 20, pp. 21-24, DOI:10.1109/NEUREL.2012.6419953

[4] Sah M., Kim H. and Chua L., "Brains Are Made of Memristors", *IEEE Circuits and Systems Magazine* (2014) 14 (1) 12–36, DOI: 10.1109/MCAS.2013.2296414.

[5] Sah M., Yang C., Kim H., Roska T. and Chua L., "Memristor Bridge Circuit for Neural Synaptic Weighting", *In: Proc. 13th CNNA, IEEE*, Italy, 2012, pp. 1–5, DOI:10.1109/CNNA.2012.6331434.

[6] Ebong I. and Mazumder P., "CMOS and Memristor-Based Neural Network Design for Position Detection", *Proc. IEEE (2012)* 100 (6) pp. 2050–2060, DOI: 10.1109/JPROC.2011.2173089.

[7] Tsakoumis A.C., Vladov S.S., Mladenov V.M. "Electric load forecasting with multilayer perceptron and Elman neural network", In *6th IEEE Seminar on Neural Network Applications in Electrical Engineering* 2002 Sep 26, pp. 87-90.

[8] Strukov D., Snider G., Stewart D., Williams R. S., "The missing memristor found," *Nature Letters*, Vol 453, 2008, DOI:10.1038/nature06932, pp. 80 – 83.

[9] Chua L., "Memristor — The Missing Circuit Element", *IEEE Transactions on Circuit Theory* (1971) 18 pp. 507–519, DOI: 10.1109/TCT.1971.1083337.

[10] Amer S, Sayyaparaju S, Rose G.S, Beckmann K, Cady N.C., "A practical hafnium-oxide memristor model suitable for circuit design and simulation", *In 2017 IEEE International Symposium on Circuits and Systems (ISCAS)* 2017 May 28, pp. 1-4, DOI: 10.1109/TCT.1971.1083337

[11] Mladenov V., "A New Simplified Model for HfO_2-Based Memristor", in: *IEEE Proceedings of 8th MOCAST*, 2019, 1–4, DOI: 10.1109/MOCAST.2019.8741953.

[12] Abunahla H, Mohammad B, Jaoude Abi M, Al-Qutayri M., "Novel hafnium oxide memristor device: Switching behaviour and size effect", In 2017 IEEE International Symposium on Circuits and Systems (ISCAS) 2017 May 28, pp. 1-4, DOI: 10.1109/ISCAS.2017.8050791

[13] Strachan J.P., Torrezan A.C., Miao F., Pickett M.D, Yang J.J., Yi W, Medeiros-Ribeiro G, Williams R.S., "State dynamics and modeling of tantalum oxide memristors", *IEEE Transactions on Electron Devices*. 2013 Jun 17;60(7), pp. 2194-202, DOI: 10.1109/TED.2013.2264476

[14] Ascoli A, Tetzlaff R, Chua L., "Robust simulation of a TaO memristor model", Radioengineering, 2015 Jun 1;24(2):3, pp. 84-92, DOI: 10.13164/re.2015.0384

[15] Mladenov V. Analysis of memory matrices with HfO_2 memristors in a PSpice environment. *Electronics*. 2019 Apr;8(4), DOI: 10.3390/electronics8040383

[16] Torrezan A.C., Strachan J.P., Medeiros-Ribeiro G, Williams R.S. Sub-nanosecond switching of a tantalum oxide memristor. *Nanotechnology*. 2011 Nov 9; DOI: 10.1088/0957-4484/22/48/485203

[17] Mladenov V., A Modified Tantalum Oxide Memristor Model for Neural Networks with Memristor-Based Synapses. In 2020 9th International Conference on Modern Circuits and Systems Technologies (MOCAST) 2020 Sep 7 (pp. 1-4). IEEE, DOI: 10.1109/MOCAST49295.2020.9200238

[18] A. Ascoli, R. Tetzlaff, Z. Biolek, Z. Kolka, V. Biolkovà, D. Biolek, "The Art of Finding Accurate Memristor Model Solutions," IEEE J. Emerg. Sel. Top. Circuits Syst., 5, 2015, pp. 133–142, DOI: 10.1109/JETCAS.2015.2426493

[19] C. Yakopcic, T. Taha, G. Subramanyam, R. Pino, "Memristor SPICE Modeling," Advances in Neuromorphic Memristor Science and Applications, DOI 10.1007/978-94-007-4491-2_12, pp. 211 – 244.

[20] V. Mladenov, "Advanced Memristor Modeling - Memristor Circuits and Networks," MDPI Basel, Switzerland, ISBN 978-3-03897-104-7 (Hbk), https://doi.org/10.3390/books978-3-03897-103-0, 2019.

[21] Y. Zhang, X. Wang and E. G. Friedman, "Memristor-Based Circuit Design for Multilayer Neural Networks," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 2, pp. 677-686, Feb. 2018, doi: 10.1109/TCSI.2017.2729787.

[22] E. Lehtonen, M. Laiho, "CNN using memristors for neighborhood connections," *12th International Workshop on Cellular Nanoscale Networks and their Applications (CNNA 2010*), 2010, pp. 1-4, doi: 10.1109/CNNA.2010.5430304.

[23] Mladenov V., "Synthesis and Analysis of a Memristor-Based Artificial Neuron," *IEEE, VDE Proceedings of CNNA* 2018, The *16th International Workshop on Cellular Nanoscale Networks and their Applications*, Print ISBN: 978-3-8007-4766-5, pp. 1 – 4.

[24] Choi, S., Ham, S. and Wang, G., 2019. Memristor synapses for neuromorphic computing, In Memristors-Circuits and Applications of Memristor Devices, InTechOpen, pp.1-14, DOI: 10.5772/intechopen.85301

[25] Linn E., Siemon A, Waser R. and Menzel S., "Applicability of Well-Established Memristive Models for Simulations of Resistive Switching Devices", *IEEE Trans. Circ. Syst.* (2014) 2402–2410, DOI: 10.1109/TCSI.2014.2332261.

[26] Mladenov V., Kirilov S., "Learning of an Artificial Neuron with Resistor-Memristor Synapses", *ANNA'18, IEEE, VDE* (2018), Print ISBN: 978-3-8007-4756-6.

[27] Chen S., Billings S., Luo W., "Orthogonal least squares methods and their application to non-linear system identification", *International Journal of Control, Taylor & Francis*, 1989, https://doi.org/10.1080/00207178908953472, pp. 1873 - 1896.

[28] Aggarwal, C., "Neural Networks and Deep Learning"., *Springer International Publishing AG*, eBook ISBN 978-3-319-94463-0, 2018.

[29] Mladenov V, Kirilov S., "A memristor model with a modified window function and activation thresholds", *In 2018 IEEE International Symposium on Circuits and Systems (ISCAS)* 2018 May 27, pp. 1-5, DOI: 10.1109/ISCAS.2018.8351429

[30] Y. Yang, Seung C. Lee., "Circuit Systems with MATLAB and PSpice," John Wiley & Sons, 2008, ISBN 978-04-7082-240-1, 532.

[31] Mladenov, V., "A Unified and Open LTSPICE Memristor Model Library" *MDPI Electronics*, 2021, Vol. 10, no. 13: 1594. https://doi.org/10.3390/electronics10131594.

[32] Qiangfei X., Robinett W., Cumbie M., Banerjee N., Cardinali T. J., J. Yang J., Wei W., Xuema Li, William M. Tong, Strukov D. B., Snider G. S., Medeiros-Ribeiro G., and Williams R. S., "Memristor−CMOS Hybrid Integrated Circuits for Reconfigurable Logic"., *Nano Letters* 2009 9 (10), pp. 3640-3645, DOI: 10.1021/nl901874j.

[33] Pedretti, G., Ielmini, D., "In-Memory Computing with Resistive Memory Circuits: Status and Outlook", *MDPI Electronics* 2021, 10, 1063. https://doi.org/10.3390/electronics10091063